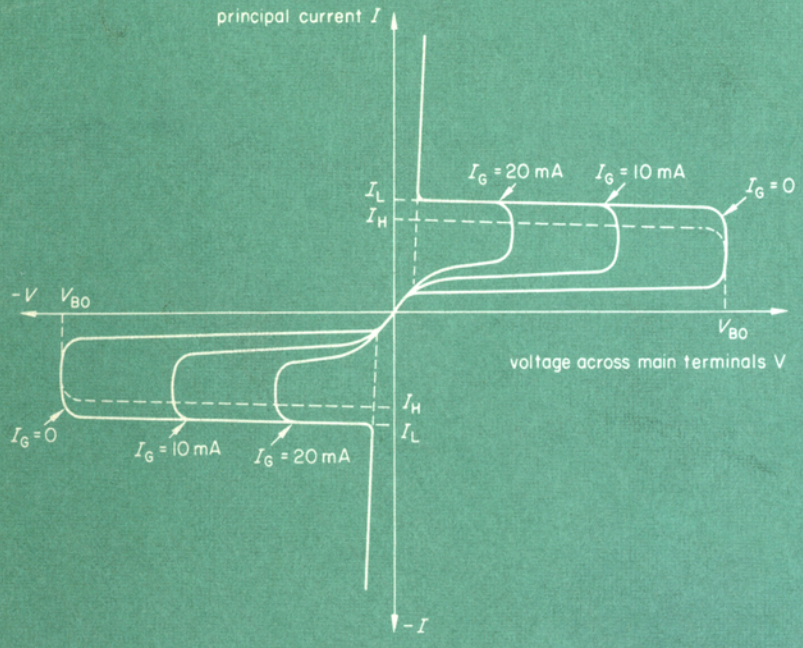

F. Brogan

semiconductor electronics by worked example

SEMICONDUCTOR ELECTRONICS
by Worked Example

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SEMICONDUCTOR ELECTRONICS by Worked Example

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Macmillan Education

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Preface

The stimulus for this book was provided by two annual requests from students, the first being to recommend a suitable textbook to cover the contents of a given electronics syllabus, and the second to provide tutorial periods which in their opinion provided a successful way of teaching electronic theory and circuits.

As most modern electronics syllabuses cover mainly semiconductor devices, I have attempted to meet both these requests by devoting the contents of this book entirely to the treatment of semiconductor devices and their associated circuitry by means of worked examples, the majority of which are taken from past papers of various examining bodies. Wherever possible, the examples in each chapter have been graded to lead the student through the simpler to the more difficult questions. Both qualitative and quantitative examples are solved and further questions are posed at the end of each chapter for the student to attempt.

The majority of the questions are taken from past examination papers of the City and Guilds of London Institute Electronic Technician Course No. 281, and Telecommunication Technician Course No. 271, the rest being from past examination papers of the Institution of Electrical Engineers, the Institution of Electronic and Radio Engineers, the Union of Lancashire and Cheshire Institutes and Wigan and District Mining and Technical College. In this respect, I would like to thank the boards of the above bodies and the Principal of Wigan and District Mining and Technical College for permitting me to reproduce these problems; the responsibility for the accuracy of the solutions is entirely mine.

Finally, I would like to thank my wife for her encouragement during my preparation of the manuscript and for her subsequent typing of it.

Wigan 1974 F. BROGAN

Key to source of examination questions

ET3	City and Guilds of London Institute Industrial Electronics 1 paper
ET4	City and Guilds of London Institute Industrial Electronics II paper
ET5	City and Guilds of London Institute Industrial Electronics III paper
TT3	City and Guilds of London Institute Telecommunications course third year
TT4	City and Guilds of London Institute Telecommunications course fourth year
TT5	City and Guilds of London Institute Telecommunications course fifth year
U.L.C.I	Higher National Certificate papers of the Union of Lancashire and Cheshire Institutes
H.N.C.	Higher National Certificate
I.E.E.	Part Three Applied Electronics paper of the Institution of Electrical Engineers
I.E.R.E.	Electronics and Communication papers of the Institution of Electronic and Radio Engineers

1 Semiconductor diodes, rectifiers and stabilisers

1.1 Current conduction in a semiconductor

Explain the differences between intrinsic p-type and n-type conduction in a semiconductor such as germanium.

(ET3)

Every atom contains a nucleus of neutrons and positively charged protons. This is surrounded by electrons, which are negatively charged, moving in orbits or shells around the nucleus. Each shell is at a fixed radius from the nucleus and can contain only a fixed number of electrons. The number of electrons in the outer shell of the atom determines whether the atom is a *conductor* or an *insulator*: for if the outer shell contains only a few electrons, these are easily attracted from the atom and the material is therefore a conductor; but if the outer shell is full of electrons, these will not easily be attracted from it, and the material is therefore an insulator. To see what constitutes a *semiconductor*, however, consider the germanium atom, which is a positive nucleus surrounded by 32 electrons.

For any atom

Shell 1 contains 2 electrons
Shell 2 contains 8 electrons
Shell 3 contains 18 electrons
Shell 4 contains 18 electrons

The germanium atom will therefore have only 4 electrons in shell 4, and these are termed *valence electrons.*

Figure 1.1a shows that a crystal of germanium is built up by an atom sharing each of its four valence electrons with one valence electron from each of the four neighbouring atoms, so that the central atom now has effectively eight valence electrons. This sharing of two electrons is called a *covalent bond*, and the crystal of germanium is built up from these atoms. In this state the germanium crystal would be an insulator as there are no free electrons. However, the covalent bonds are weak, and the thermal energy that electrons receive at room temperature is sufficient to enable some of them to break free from the bonds and to become free electrons. When such an electron leaves the shell it leaves a gap into which another electron can move, and such a gap is termed a *positive hole*. This explains why the resistance of a semiconductor decreases with increase in temperature, that is as temperature increases more covalent bonds break down and more free electrons are provided thereby causing resistance to decrease.

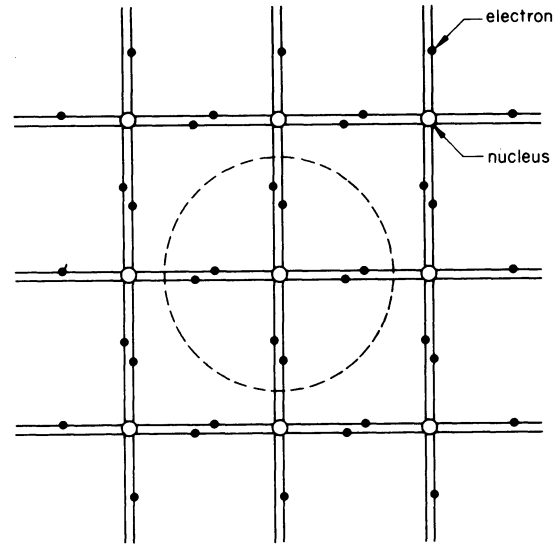


Figure 1.1a

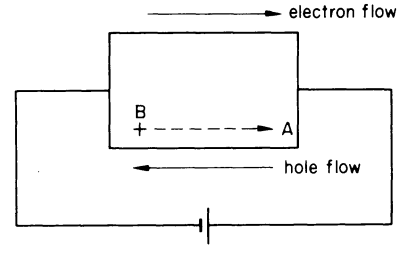


Figure 1.1b

In a semiconductor material the current flow consists of both a movement of electrons and a movement of holes. Electrons can flow towards the positive terminal of the battery, as they normally do in metals, without moving into any positive holes; this is known as *electron motion* or *electron flow*. Some electrons, however, move towards the positive holes. For example in figure 1.1b an electron moving from an atom at B into a hole at A leaves a positive hole at B; so that, although an electron has actually moved from B to A, it appears that the hole has moved from A to B. This is known as *hole motion* or *hole flow.*

Doping

The indium atom has only 3 electrons in its outer shell. If this atom is substituted for one of the germanium atoms in a germanium crystal (as shown in figure 1.2a) then, as it has only 3 electrons to share, a positive hole will appear at the place where the fourth

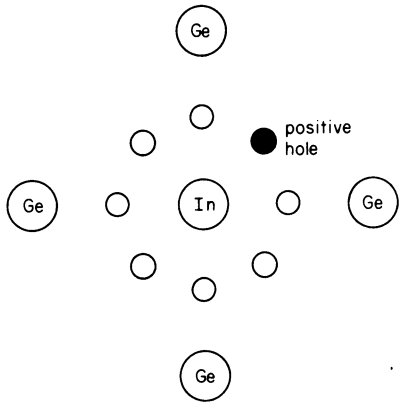


Figure 1.2a

electron should be. If this is repeated many times, the germanium is said to be *doped* positively and is known as *p-type germanium.* (In practice, there is only one impurity atom for every 10^7 germanium atoms.)

In figure 1.2b an antimony atom, which has 5 electrons in its outer shell, is substituted in place of a germanium atom. Four of

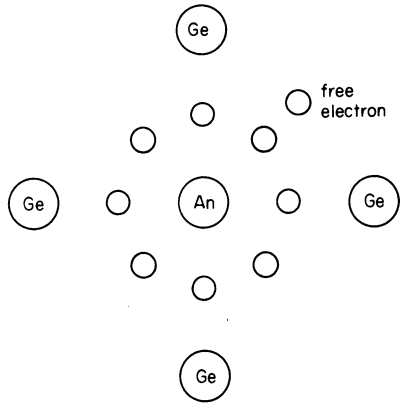


Figure 1.2b

these electrons form covalent bonds and the fifth remains free. If this process is repeated many times, the germanium is said to be doped negatively, and is known as *n-type germanium.*

In a *p*-type material the holes are referred to as *majority carriers*, because there are many more holes than electrons, while electrons are referred to as *minority carriers*. Thus, current flow in a *p*-type material can be considered to consist mainly of a flow of majority carriers which are holes.

Similarly, in *n*-type materials electrons are the majority carriers and holes are the minority carriers. Current flow in *n*-type materials can therefore be considered to consist mainly of a flow of majority carriers which are electrons.

1.2 Junction diode

Describe with a cross-sectional diagram the structure and principle of operation of a junction diode. Mention the materials used and explain why a very high degree of purity is necessary in them. State, with reasons, the effect of excess voltage on a junction diode. (TT2)

The structure of a *pn*-junction diode is shown in figure 1.3a and its corresponding circuit symbol appears in figure 1.3b.

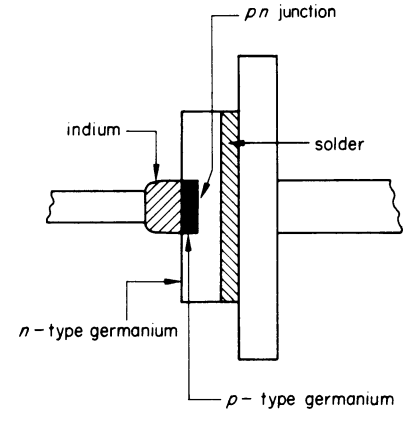


Figure 1.3a

Consider a piece of semiconductor, half of it doped *n*-type and the other half doped *p*-type; the initial situation is shown in figure 1.4 with both pieces electrically neutral. When one of the free

Figure 1.3b

electrons moves away from its associated atom, the remaining part of the atom is left relatively positively charged and is then known as a *positive ion* (note that this is fixed in the crystal and cannot move). Similarly, when a hole moves away from its atom in the *p*-type material, the remaining part is a fixed *negative ion*. The holes in the *p*-type and the electrons in the *n*-type are known as *majority carriers.*

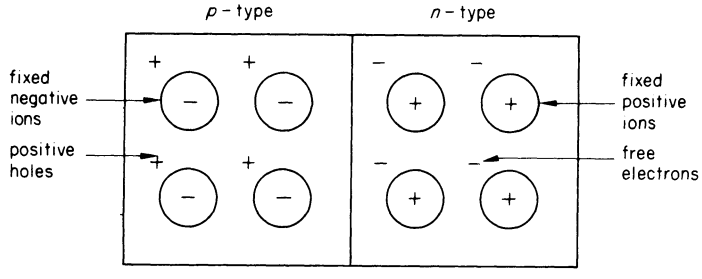


Figure 1.4

At room temperature, thermal energy causes the breakdown of some covalent bonds in both the *p*-type and *n*-type materials (as previously described), thereby causing the formation of a few hole–electron pairs in both types of material (note that these are also formed if there are any impurities in the germanium initially). In the *p*-type, the few extra holes produced will be insignificant compared with the millions of holes present already. However, the few electrons do play an important part in current conduction. These few electrons in the *p*-type and the few holes in the *n*-type are known as *minority carriers.*

Consider the semiconductor shown in figure 1.4; initially, majority holes from *p*-type diffuse into *n*-type and majority electrons from the *n*-type diffuse into the *p*-type, and these holes and electrons recombine when they meet. This flow of majority carriers across the junction eventually stops because of the force exerted by the ions near the junction, because the holes and the electrons in a very narrow layer near the junction have all recombined, leaving a row of negative ions on the *p*-side of the junction and a row of positive ions on the *n*-side of the junction (as shown in figure 1.5).

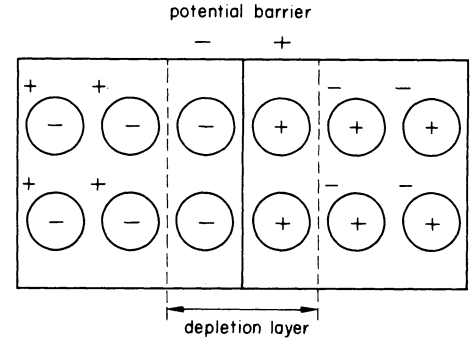


Figure 1.5

These ions form a potential barrier at the junction, known as the junction or *barrier potential*, which prevents the flow of further majority carriers. As there are no majority carriers in this region near the junction, it can be considered to be an insulator. This region is known as the *depletion layer.* (Note that although this junction potential will help the movement of the few minority carriers across the junction, this movement is balanced out by the flow of an equal number of majority carriers in the opposite directions.)

Reversed biased pn junction

When the battery is connected as in figure 1.6, it will cause holes in the *p*-type and electrons in the *n*-type to move away from the junction, thereby increasing the depletion layer and reinforcing

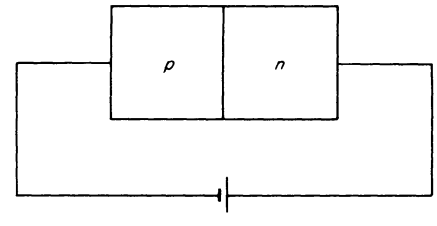


Figure 1.6

the barrier potential. Thus, no flow of majority carriers can take place across the junction, and the only current that does flow across it consists of the small movement of minority carriers which is aided by the barrier potential. Hence, to ensure that the reverse current flow in a junction diode is small (that is a few μA), the

initial semiconductor material should be extremely pure and the temperature should be as low as possible.

Forward biased pn junction

With the battery connected as in figure 1.7 it tends to overcome barrier potential, and when it is greater than the barrier potential (that is, between 0·2 and 1·0 V), a large flow of majority carriers

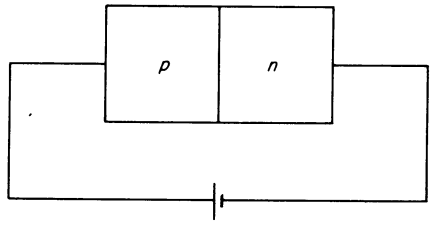


Figure 1.7

occurs. In practice, the forward voltage-drop across a diode is nearly equal to the barrier potential. As can be seen from figure 1.8, a *silicon* diode normally has a larger forward voltage drop than a *germanium* diode and can normally withstand larger forward currents.

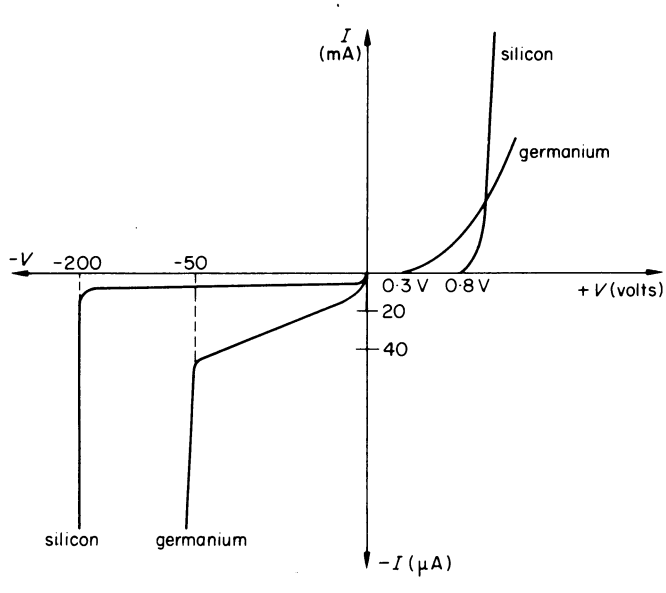


Figure 1.8

In the reverse direction however, the small current through a germanium diode tends to increase with voltage whereas the lower silicon-diode current remains fairly constant with voltage. If the reverse voltage becomes too large however, it accelerates the minority carriers to such a high speed that when they collide with other atoms in the depletion layer they dislodge electrons, thereby causing the formation of other hole–electron pairs. The effect is cumulative and is known as *avalanche breakdown*; it results in destruction of the diode unless the reverse current is limited.

1.3 Full-wave rectifier circuits

Give the meaning of the term 'peak inverse voltage' as applied to the diode in a rectifier circuit. With the aid of suitable wave and circuit diagrams, explain the differences between a full-wave rectifier which uses (a) two diodes; (b) four diodes. In particular mention the transformer required and the peak inverse voltage across the diodes, if the d.c. output voltage is the same in each case.

(ET3)

The peak inverse voltage of a diode is the maximum reverse voltage that may be applied across it without reverse breakdown occurring.

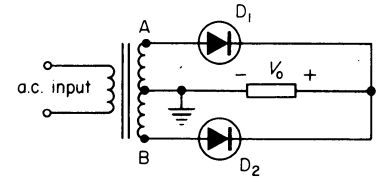


Figure 1.9a

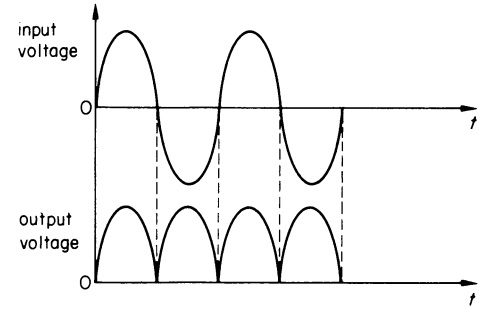


Figure 1.9b

Figure 1.9a is the circuit diagram of a full-wave bi-phase rectifier employing two diodes. This circuit uses a transformer with a centre-tapped secondary. Assuming a mains input voltage of 240 V, 240 V will be developed across each half of this secondary winding. On the first half cycle of the input voltage, point A goes positive with respect to earth and diode D_1 conducts, thereby passing current down the load. Meanwhile, voltage point B remains negative with respect to earth and D_2 is cut off. At the peak input voltage, the peak inverse voltage across D_2 will be $2 \times 240\sqrt{2}$ V; that is $240\sqrt{2}$ V across the lower half of the secondary winding, and $240\sqrt{2}$ V across the load. Also, the peak forward current through D_1 will be $240\sqrt{2}/R$ A (where R is the forward resistance of the diode) and the average current will be $240\sqrt{2}/\pi R$ A.

On the second half cycle of the input voltage, point B will go positive with respect to earth and D_2 will conduct, thereby passing current down the load (that is, in the same direction as during the first half-cycle). Meanwhile, voltage point A will go negative with respect to earth and D_1 will be cut off. Thus, though the conditions of the diodes are reversed the direction of the load current is the same, so that the output voltage is as shown in figure 1.9b.

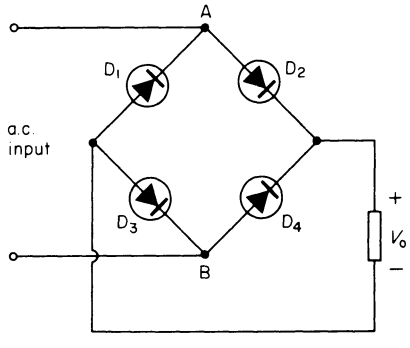


Figure 1.10

Figure 1.10 is the circuit diagram of a full-wave bridge rectifier employing four diodes. This circuit either uses a 1-to-1 input transformer or can have the mains input-voltage applied directly to its input.

On the first half-cycle, as point A goes positive with respect to earth, current flows in through diode D_2, down the load, and out through diode D_3. Meanwhile, diodes D_1 and D_4 are cut off. In this circuit, the peak inverse voltage across diodes D_1 and D_4 is only $240\sqrt{2}$ V, but the values of the peak forward-current and average current through diodes D_2 and D_3 are the same as the corresponding values in the bi-phase rectifier circuit.

On the second half cycle, as point B goes positive with respect to earth, current flows in through diode D_4, down the load, and out through diode D_1. Again, although the conditions of the diodes are reversed, the direction of the load current is the same, and the output voltage is as shown in figure 1.9b.

Thus, the advantages of the bridge rectifier circuit over the bi-phase rectifier circuit are that it does not require a centre-tapped transformer, and that the peak inverse-voltage across each diode is only half of that existing in the bi-phase rectifier circuit. When semiconductor diodes are employed the bridge rectifier is more commonly used as the cost of the two extra diodes is then not excessive.

1.4 Operation of Zener stabiliser

Briefly explain how the operation of a Zener diode differs from that of a conventional silicon diode.

Draw the circuit diagram of a simple Zener-diode stabilising-circuit and calculate suitable component values to provide a 20 V *d.c. stabilised supply to a variable load, from a 50* V *d.c. input. A 20* V, *4* W *Zener is to be used, whose voltage remains constant down to a diode current of 0·5* mA.

Explain how the circuit stabilises (a) against supply voltage variations; (b) against load current variations.

Also calculate (c) the maximum and minimum supply voltage between which stabilisation is satisfactory if the load resistance is 1·5 kΩ; *(d) the minimum value of load resistance when the supply voltage is 50* V.

In the forward direction the Zener diode has a similar characteristic to any other silicon diode, with a forward voltage drop of about 0·5 V, as shown in figure 1.11. In the reverse direction however, the Zener diode breaks down at much lower reverse voltages (from about −2 V). This is because the Zener diode is manufactured with a much narrower junction than a normal silicon diode by using an impurity content of only 1 in 10^5. Hence, at relatively small reverse voltages, the electric-field strength across the junction is sufficient to cause electrons to break away from their covalent bonds, thereby giving rise to what is known as *field* emission. Breakdown in a normal silicon diode occurs at much higher voltages, and it is caused by the minority carriers colliding with ions in the depletion layer, thereby releasing more electrons from the covalent bonds, and

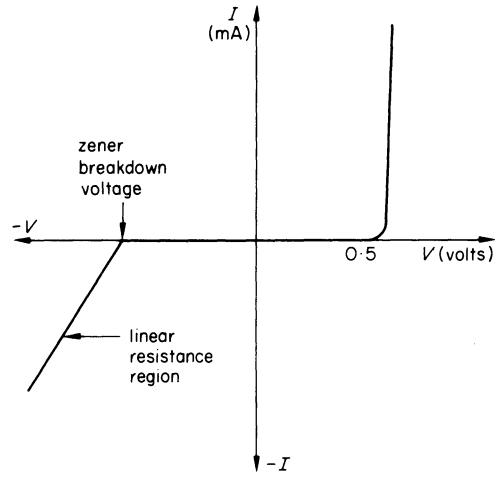


Figure 1.11

giving rise to what is termed *avalanche breakdown*. After breakdown, as the voltage across the Zener diode increases only slightly with further increase in current through it, it can subsequently be treated as a linear resistor. Therefore

$\Delta V_z / \Delta I_z = R_z$ = slope resistance of Zener

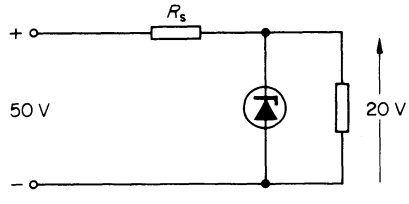


Figure 1.12

The basic Zener-diode voltage-stabiliser circuit is shown in figure 1.12. Consider an open-circuit load; the Zener will then take its maximum current, which is given by

I_{max} = Power/Voltage = 4/20 = 1/5 = 200 mA

To stabilise at 20 V from a 50 V input, 30 V must be dropped across R_s therefore

$R_s = 30/200 \times 10^{-3} = 150\ \Omega$

To understand the action of the above circuit, the Zener can be considered to be a *current reservoir* as long as it remains broken down. Its response to supply-voltage and load-current variations is as follows:

(a) When the supply voltage increases, the Zener diode takes the extra current while the increase in voltage appears across R_s. Similarly, when the supply voltage decreases, the Zener supplies the extra current required by the load and the voltage across R_s decreases.

(b) When the load current decreases because of increase in load resistance, the Zener current must increase by the same amount. Similarly, when the load current increases because of fall in load resistance, the Zener must shed an equal amount of current to the load.

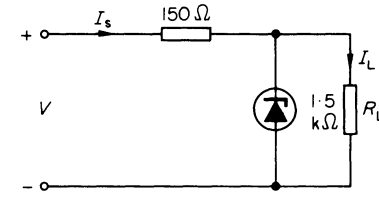


Figure 1.13

(c) For minimum value of supply voltage, the data requires that the Zener must still pass 0·5 mA. In figure 1.13

$I_L = 20/1500 = 13{\cdot}33$ mA

therefore

$I_s = 13{\cdot}83$ mA

and

$V_{min} = (13{\cdot}83 \times 10^{-3} \times 150) + 20 = 22{\cdot}07$ V

For maximum value of supply voltage, the Zener will pass its maximum current of 200 mA. Therefore

$I_s = 213{\cdot}3$ mA

and

$V_{max} = 0{\cdot}2133 \times 150 + 20 = 52$ V

(d) When $V = 50$ V, minimum value of R_L occurs when Zener current is 0·5 mA; then

$I_s = 30/150 = 200$ mA

and

$I_L = 199{\cdot}5$ mA

therefore

$$R_L = \frac{20}{199{\cdot}5 \times 10^{-3}} \approx 100\ \Omega$$

1.5 Zener-stabiliser calculations

A Zener diode has a reverse breakdown-voltage of 5·8 V and after this can be considered to be a linear resistance of 10 Ω. It is to be used in a simple voltage stabilising circuit to stabilise the load voltage at 6 V from a 12 V supply. If the load resistor is 2 kΩ, draw a suitable circuit diagram and calculate the value of the required series resistor. Also determine (a) the change in load voltage, if the supply voltage increases by 10 per cent; (b) the minimum value of load resistor for which stabilisation will still be effective, with a 12 V supply; (c) the minimum value of supply voltage for which stabilisation will still be effective, with a 2 kΩ load resistor.

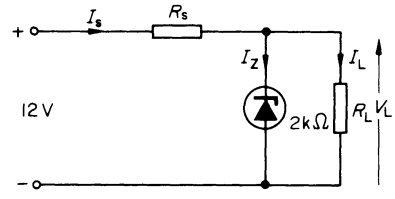


Figure 1.14

In figure 1.14, when $V_L = 6$ V

$$I_L = \frac{6}{2 \times 10^3} = 3\ \text{mA}$$

Also

$$V_L = V_B + I_z R_z$$

where

V_B = Zener breakdown-voltage

R_z = Zener slope-resistance

therefore

$$6 = 5{\cdot}8 + I_z 10$$

$$I_z = 0{\cdot}2/10 = 20\ \text{mA}$$

$$R_s = \frac{12 - 6}{(3 + 20)10^{-3}} = \frac{6000}{23} = 261\ \Omega$$

(a) When supply voltage increases by 10 per cent to 13·2 V

$$13{\cdot}2 = (I_L + I_z)261 + 2000\, I_L \qquad (1.1)$$

Also

$$V_L = 2000\, I_L = 5{\cdot}8 + 10\, I_z$$

$$I_z = 200\, I_L - 0{\cdot}58$$

Substituting for I_z in equation 1.1

$$13.2 = (I_L + 200\, I_L - 0{\cdot}58)261 + 2000\, I_L$$

$$= 52\,461\, I_L - 151{\cdot}4$$

then

$$I_L = \frac{164{\cdot}6}{52{\cdot}461} = 3{\cdot}13\ \text{mA}$$

$$V_L = 6{\cdot}26\ \text{V}$$

Change in the load voltage is 0·26 V.

(b) the minimum value of load resistance will be when Zener diode just breaks down; that is, when $V_L = 5{\cdot}8$ V and $I_z = 0$. Hence, conditions will be as shown in figure 1.15.

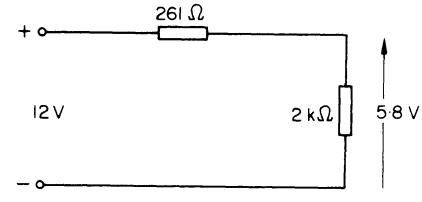


Figure 1.15

$$I_L = I_s = \frac{12 - 5{\cdot}8}{261} = 23{\cdot}8\ \text{mA}$$

$$\text{Minimum } R_L = \frac{5{\cdot}8}{(23{\cdot}8)10^{-3}} = 244\ \Omega$$

(c) Similarly, for minimum supply-voltage, Zener just breaks down and conditions are shown in figure 1.16.

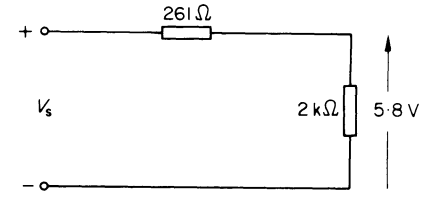


Figure 1.16

therefore

$$I_s = \frac{5{\cdot}8}{2000} = 2{\cdot}9 \text{ mA}$$

$$V_s = (261 \times 2{\cdot}9 \times 10^{-3}) + 5{\cdot}8 = 0{\cdot}757 + 5{\cdot}8 = 6{\cdot}557 \text{ V}$$

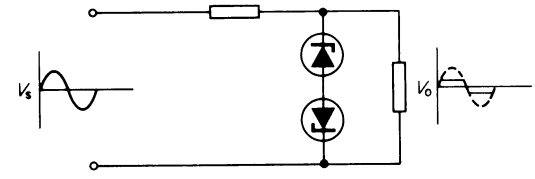


Figure 1.17

1.6 Other Zener circuits

Explain two distinct uses for a Zener diode other than as a simple stabiliser.

A Zener diode has a reverse characteristic equation V = 10 + 6I (V in volts, I in amps) for values of I greater than 5 mA. *It is used as a simple stabiliser for a load which can vary between 0 and 200* mA *from a d.c. supply of nominal voltage 36* V *which may vary by ±6* V. *Estimate the maximum value of the series resistor which may be used if the Zener-diode current is not to fall below 5* mA *for all input and load conditions. For this value of series resistor determine (a) the minimum power-rating of the Zener diode; (b) the maximum variation in output voltage.*

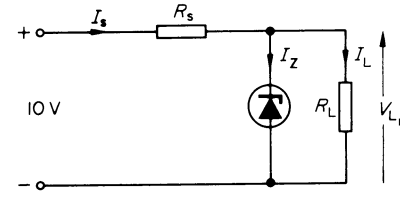


Figure 1.18

There are three common uses of the Zener diode other than in the simple stabiliser circuit

(1) as a voltage reference device in transistor stabilisers;
(2) as a protection device against overload;
(3) in a *clipper* circuit.

In (1), a sample of the output voltage is compared with the Zener voltage and the difference between the two is used as the input to a transistor amplifier which is then used to restore the output voltage to its correct level.

In (2), the Zener diode can be used to prevent overloading of sensitive meter movements without affecting meter linearity (see section 1.7).

In (3), two identical back-to-back Zener diodes can be used in the circuit configuration shown in figure 1.17 to produce an approximate square-wave from a sine-wave input.

To determine the maximum value of series resistor, the worst conditions of supply voltage and load current must be considered; that is, when the supply voltage is a minimum of 30 V and the load is taking maximum current of 200 mA, the Zener must still pass a current of 5 mA.

Considering figure 1.18

$$V_{L_1} = 10 + (6 \times 0{\cdot}005) = 10{\cdot}03 \text{ V}$$

therefore voltage drop across $R_s = 30 - 10{\cdot}03 = 19{\cdot}97$ V

$$R_s = \frac{19{\cdot}97}{(200 + 5)10^{-3}} = 97{\cdot}4\ \Omega$$

(a) to calculate the minimum power-rating of the Zener diode, the conditions when the Zener diode has maximum voltage across it and maximum current through it must be considered. This will apply when the load is open circuit and the supply voltage is a maximum of 42 V, as shown in figure 1.19.

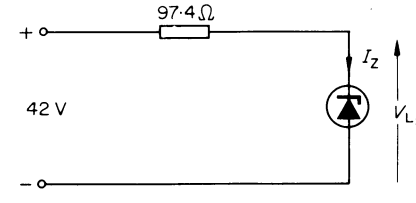


Figure 1.19

From this figure

$$42 = 97{\cdot}4\, I_z + (10 + 6\, I_z)$$

$$I_z = \frac{32}{103{\cdot}4} = 309{\cdot}5 \text{ mA}$$

when

$$V_{L_2} = 10 + (6 \times 0{\cdot}3095) = 11{\cdot}857 \text{ V}$$

therefore

minimum power rating = VI_z = 3·7 W

(b) The maximum variation in output voltage will be the change occurring between the two extreme circuit conditions; that is, between minimum supply-voltage with maximum load-current, and maximum supply-voltage with zero load-current.
Therefore

maximum variation in output voltage = $V_{L_2} - V_{L_1}$

$$= 11{\cdot}857 - 10{\cdot}03$$

$$= 1{\cdot}827 \text{ V}$$

1.7 Zener protection circuit

The circuit shown in figure 1.20 represents a d.c. voltmeter which reads 20 V full scale. The meter resistance is 560 Ω and $R_1 + R_2$ = 99·5 kΩ. If the diode is a 16 V Zener, find R_1 and R_2 so that when V = 20 V, the Zener diode conducts and the overload current is shunted away from the meter.

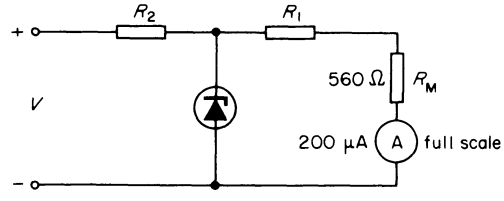


Figure 1.20

When the input voltage is 20 V, the Zener diode just breaks down; that is, the voltage across it will be 16 V but it will not be taking any current. At that time the meter must indicate full-scale deflection. The current through R_1, R_2 and the meter will therefore be 200 μA. Then

$$R_2 = \frac{20 - 16}{20 \times 10^{-6}} = 20 \text{ kΩ}$$

$$R_1 = 79{\cdot}5 \text{ kΩ}$$

(Check)

$$(R_1 + R_M) = 80 \text{ kΩ}$$

therefore

$$(R_1 + R_M) \times 200 \times 10^{-6} = 16$$

1.8 Stabilisation ratio of a Zener stabiliser

Draw and describe the current/voltage characteristic of a Zener diode. Explain the operation of the voltage-stabiliser circuit shown in figure 1.21 and calculate the value of R_s if the stabilisation ratio is to be 0·005. What would be the effect of doubling R_s? The dynamic resistance of the diode, beyond its breakdown voltage of 6 V, is 10 Ω.

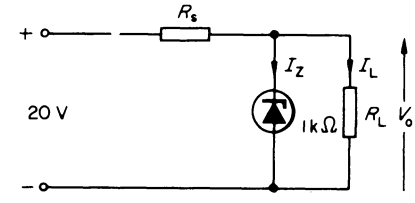


Figure 1.21

The first part of this question is answered in section 1.4. Stabilisation ratio

$$S = \frac{\text{small change in output voltage}}{\text{small change in input voltage}} = \frac{\Delta V_0}{\Delta V_1}$$

for constant value of load resistor.
From figure 1.21

$$V_1 = (I_L + I_z)R_s + V_0 \qquad (1.2)$$

Current flowing through the Zener, I_z, is given by

$$I_z = \frac{V_0 - V_z}{R_z}$$

where V_z = Zener breakdown voltage. Also, current through the load, $I_L = V_0/R_L$. Substituting these values of I_z and I_L in equation 1.2

$$V_1 = \left(V_0/R_L + \frac{V_0 - V_2}{R_z}\right)R_s + V_0$$

$$V_1 = V_0(1 + R_s/R_L + R_s/R_z) - \frac{V_z R_s}{R_z}$$

To calculate the approximate effect of a change in the input voltage, it may be assumed that V_z is constant and that $R \ll R_L$, so that R_s/R_L may be neglected compared with R_s/R_z. Then, considering small changes of voltage

$$\Delta V_1 \approx \Delta V_0(1 + R_s/R_z)$$

$$S = \Delta V_0/\Delta V_1 = \frac{R_z}{R_s + R_z} \qquad (1.3)$$

Substituting the values given

$$0{\cdot}005 = \frac{10}{R_s + 10}$$

therefore

$$0{\cdot}005\, R_s + 0{\cdot}05 = 10$$

$$R_s = \frac{9{\cdot}95}{0{\cdot}005} = 1{\cdot}99\ \text{k}\Omega$$

From equation 1·3, if R_s is doubled, as it is large compared with R_z, the stabilisation ratio S will be halved, which doubles the effectiveness of the circuit.

1.9 Voltage-doubling circuit

With the aid of a circuit diagram, describe the action of a voltage-doubler circuit using capacitors and diodes.

(ET3)

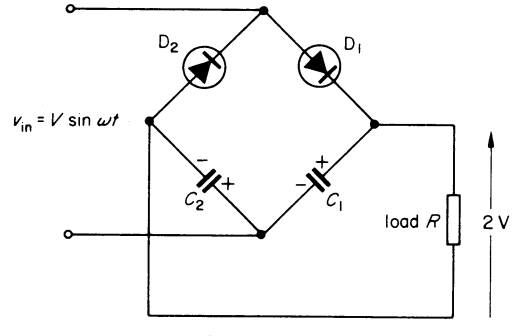


Figure 1.22

Considering figure 1.22, on the positive half-cycle of the input voltage, C_1 will charge up through D_1 to a voltage V volts, which is the maximum value of the a.c. input voltage. Similarly, on the negative half-cycle of the input voltage, C_2 charges through D_2 to a voltage V volts. After one cycle of input voltage, the voltage across the load resistor R will be 2 V volts. However, this assumes that the capacitors do not discharge through R in the time when they are not being charged. This circuit is only effective for very high load-resistor values, and its regulation deteriorates rapidly at low values of R. The peak inverse voltage across the diodes in this circuit will be 2 V volts.

1.10 Voltage-quadrupling circuit

Give a circuit diagram of a voltage-quadrupler circuit employing diodes and capacitors. Describe the action of the circuit, stating its limitations, and suggest one practical use of it.

(H.N.C.)

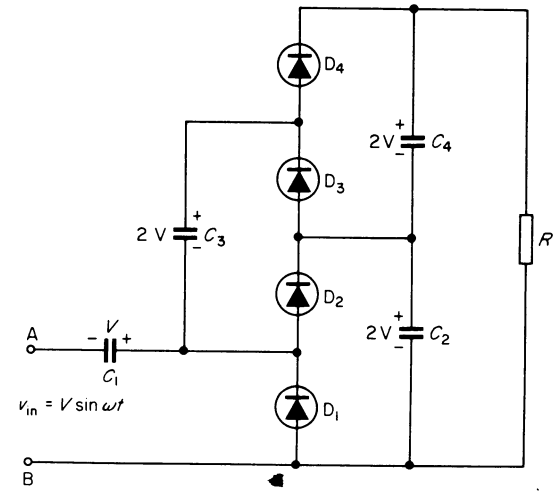


Figure 1.23

Figure 1.23 shows the circuit diagram of a voltage-quadrupler circuit. The main limitation on this circuit to ensure its effective operation, is that the load should take negligible current. To explain the operation of the circuit, it will be assumed that the load is a very high value, so that the capacitors do not discharge through it.

On the first half-cycle of supply voltage, C_1 charges through D_1 to V volts. On the second half-cycle, C_2 charges through D_2 to 2 V volts, due to supply voltage and the voltage across C_1. On the third half-cycle, C_3 charges through D_3 to 2 V volts due to supply volt-

age, voltage across C_2 minus the voltage across C_1. On the fourth half-cycle, C_4 charges through D_4 to 2 *V* volts due to supply voltage, voltage across C_1, voltage across C_3 minus the voltage across C_2. Therefore after two cycles of input voltage, the voltage across the load will be 4 *V* volts.

This circuit could be used for the E.H.T. supply in a television receiver where the current requirement is very small. In practice the circuit can be extended to give multiplication factors up to approximately 10.

1.11 Exercises

Exercise 1.1

Explain the construction of a germanium *pn*-junction diode and how it functions as a rectifier.

Show, with the aid of sketches, any differences between the current/voltage characteristics of a germanium diode and a vacuum diode valve. Comment on the shape of the characteristic.

(ET3)

Exercise 1.2

Give the circuit diagram of a rectifier bridge circuit and add wave diagrams to show how it operates. How does the transformer supplying the bridge-rectifier circuit differ from that required for a full-wave rectifier using two diodes? State what is meant by *peak inverse voltage* and calculate its value in the circuit you have drawn, if the transformer secondary voltage is 20 V r.m.s.
(Answer: 28·3 V) (ET3)

Exercise 1.3

A Zener diode has a breakdown voltage of 5 V and after this can be considered to have linear resistance of 25 Ω. It is to be used in a voltage-stabilising circuit to provide a load voltage of 5·5 V. If the supply voltage is 9 V and the load resistor is 1·1 kΩ, draw the circuit diagram and calculate the value of series resistor required. Also determine (a) the change in load voltage, if the supply voltage increases by 10 per cent; (b) the minimum value of supply voltage for which stabilisation will still be effective, with a 1·1 k Ω load; (c) the minimum value of load resistor for which stabilisation will still be effective, with a 9 V supply.
(Answers: 140 Ω, 0·13 V, 5·64 V, 175 Ω) (ET3)

Exercise 1.4

Explain, with the aid of a suitable characteristic, how the operation of a Zener diode differs from that of a rectifying diode.

The following data apply to a Zener diode

nominal voltage at 5 mA = 9 V

maximum slope-resistance at 5 mA = 10 Ω

characteristic linear above 0·5 mA.

Sketch a circuit diagram showing how this diode may be employed to supply a load of 15 mA at an almost constant voltage of 9 V from a d.c. source of 24 V (nominal).

Explain how the circuit stabilises (a) against supply-voltage variations; (b) against load-current variations.

Calculate the load voltage variation when the supply voltage varies by 2 V. What are the advantages of Zener diodes over gas stabilising-valves?
(Answer: 0·03 V) (ET5)

Exercise 1.5

A Zener diode and one resistor are joined in series to provide a 16 V stabilised output from a 20 V supply. If the load resistor is 200 Ω and the current through the stabiliser is 8 mA, determine the value of the series resistor and the power dissipated in it.

If the load is increased to 250 Ω, the output voltage rises to 16·2 V. Determine the current which then flows through the stabiliser diode, the power dissipated in it and its slope resistance, given that the Zener breakdown voltage is 15·9 V.
(Answers: 45·5 Ω, 352 mW, 20·9 mA, 338 mW, 14·3 Ω)

Exercise 1.6

Explain, with the aid of a suitable characteristic, how the operation of a Zener diode differs from that of a rectifying semiconductor-diode.

A 56 V, 8 W Zener is to be used to supply a variable load from a nominal 100 V d.c. source. Design a suitable circuit so that the Zener diode is not overloaded under any load conditions if the source voltage is 100 V. Explain how the circuit stabilises (a) against supply-voltage variations; (b) against load-current variations. If the diode can be assumed to stay constant down to a diode current of 1 mA, estimate (i) the maximum and minimum supply voltage between which stabilisation is satisfactory if the load resistance is

560 Ω; (ii) the minimum value of load resistance when the supply voltage is 100 V.
(Answers: R_s = 308 Ω, 130·8 V, 87·1 V, 395 Ω) (ET5)

Exercise 1.7

Explain two distinct uses for a Zener diode other than as a simple stabiliser.

A Zener diode has a reverse characteristic equation $V = 9{\cdot}1 + 5{\cdot}01I$ (V in volts, I in amps) for values of I greater than 0·01 A. It is used as a simple stabiliser for a load which can vary between 0 and 150 mA from a d.c. supply of nominal voltage 25 V which may vary by ±5 V.

Estimate the maximum value of the series resistor which may be used if the Zener-diode current is not to fall below 0·01 A for all input and load conditions. For this value of series resistor, determine (a) the minimum power rating of the Zener diode; (b) the maximum variation in output voltage.
(Answers: 67·8 Ω, 3 W, 1·385 V) (ET5)

Exercise 1.8

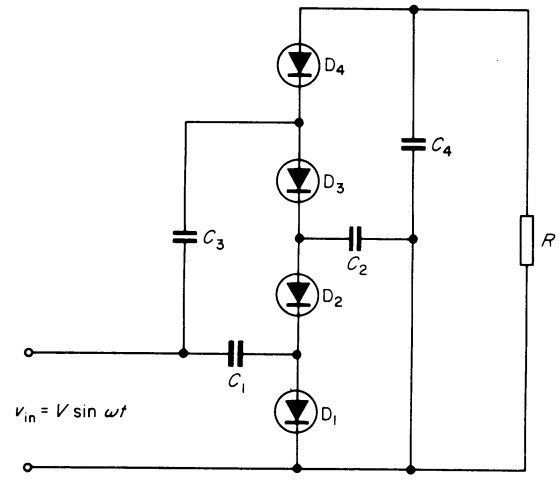


Figure 1.24

Figure 1.24 shows an alternative form of voltage-quadrupler circuit. Describe its operation.

2 Voltage and current common-emitter amplifiers

2.1 Load line; dissipation, current gain, and input resistance

The characteristics of a pnp transistor (assumed to be linear over the given range) are tabulated below. It is used in the common-emitter mode with a resistive load of 2 kΩ and a supply voltage of 10 V. Estimate, using a load line (a) the total power dissipated in the circuit under quiescent conditions when the base is biased to −50 μA; (b) the amplifier current gain; (c) the a.c. input resistance if the voltage gain is 80. Briefly state how a reduction in load resistance would affect your answers to (a) and (b).

Base current (μA)	Collector current (mA) for collector voltages of −2 V	−8 V
−20	−0·9	−1·5
−40	−1·8	−2·55
−60	−2·8	−3·85
−80	−3·9	−5·1

The load line equation is

$$V_{CC} = I_C R_L + V_C \qquad (2.1)$$

where

V_{CC} = the supply voltage

I_C = collector current

V_C = collector potential

R_L = load resistor

To fix the two points on the load line which lie on the axes of the graph, use equation 2.1 as follows
when

$$I_C = 0, \quad V_C = V_{CC} = 10 \text{ V}$$

when

$$V_C = 0, \quad I_C = \frac{V_{CC}}{R_L} = \frac{10}{2 \times 10^3} = 5 \text{ mA}$$

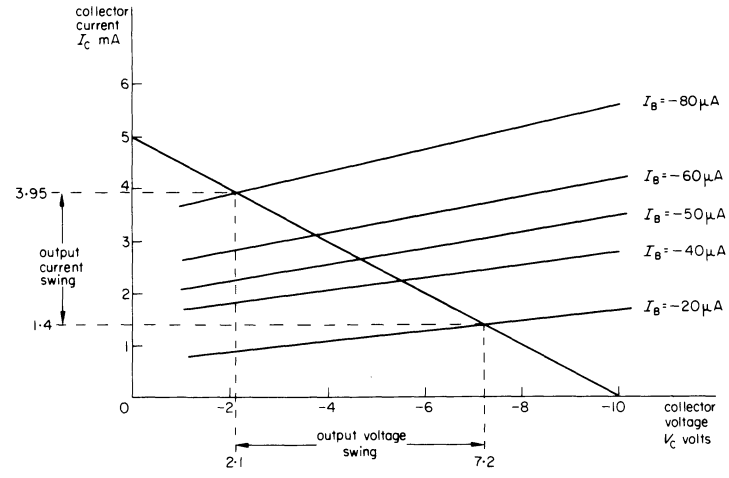


Figure 2.1

Hence the load line can be superimposed on the characteristics as shown in figure 2.1. The characteristic for a base current of −50 μA is drawn by taking the mean of those for base currents of −40 and −60 μA. At a collector voltage of −2 V the collector current will be −2·3 mA, and at a collector voltage of −10 V the collector current will be −3·5 mA.

(a) From the characteristics and the load line, the quiescent collector current I_Q is 2·7 mA. Therefore, total power dissipated in the circuit under quiescent conditions is

$$V_{CC} I_Q = 10 \times 2{\cdot}7 \times 10^{-3} = 27 \text{ mW}$$

(b) From the characteristics and load line for an input base-current swing of 60 μA, the collector current varies from 1·4 to 3·95 mA. Therefore current gain

$$A_i = i_o/i_{in} = \frac{2{\cdot}5 \times 10^3}{60 \times 10^{-6}} = \frac{2550}{60}$$

$$= 42{\cdot}5$$

(c) Voltage gain

$$A_v = v_o/v_{in} = \frac{i_o R_L}{i_{in} R_{in}}$$

where

R_{in} = input resistance of the amplifier

therefore

$$A_v = A_i \frac{R_L}{R_{in}}$$

$$80 = 42{\cdot}5 \times \frac{2000}{R_{in}}$$

$$R_{in} = \frac{42{\cdot}5 \times 2000}{80} = 1{\cdot}06\ \text{k}\Omega$$

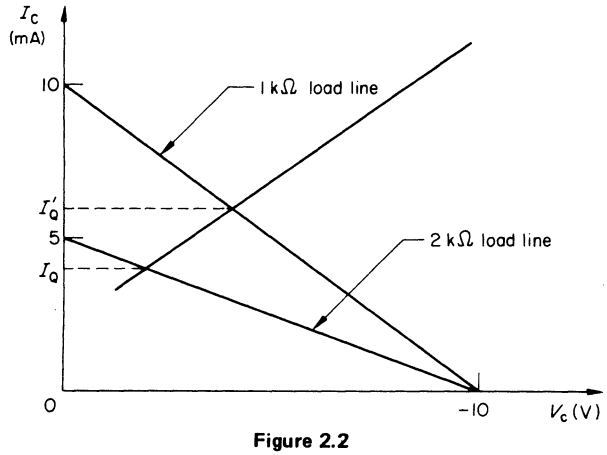


Figure 2.2

As can be seen from figure 2.2, if load was reduced to 1 kΩ, then the point on the collector-current axis would move up to 10 mA. Therefore the quiescent current in part (a) would increase and so would the power dissipation.

Similarly, the output-current swing, for the same input-current swing, would increase; and hence, in part (b), the current gain would also increase.

2.2 Load line; voltage, current, and power gains

A pnp transistor has the following characteristics which may be assumed to be linear between the values of collector voltage given

Base current (μA)	Collector current (mA) for collector voltages of −1 V	−6 V
−20	−0·9	−1·27
−40	−1·9	−2·4
−60	−3·0	−3·65
−80	−4·0	−4·79

The transistor is used as a common-emitter type amplifier with a load resistor of 1·5 kΩ and a collector supply of 7·5 V. The a.c. input resistance may be taken as 1·25 kΩ. Determine the voltage gain, current gain and power gain, when an input current of 30 μA peak varies sinusoidally about mean value of 50 μA.

If this transistor were used as a common-base type amplifier with the same load resistor and supply voltage, what values of the voltage gain, current gain, power gain and input resistance would be expected?

Hence explain why the common-base circuit is not used for multi-stage RC-coupled amplifiers.

(ET5)

The load-line equation is $V_{CC} = I_C R_L + V_C$ (as in section 2.1), which enables the points on the two axes to be determined. When

$$I_C = 0, \qquad V_C = V_{CC} = -7{\cdot}5\ \text{V}$$

when

$$V_C = 0, \qquad I_C = \frac{V_{CC}}{R_L} = \frac{7{\cdot}5}{1{\cdot}5 \times 10^3} = 5\ \text{mA}$$

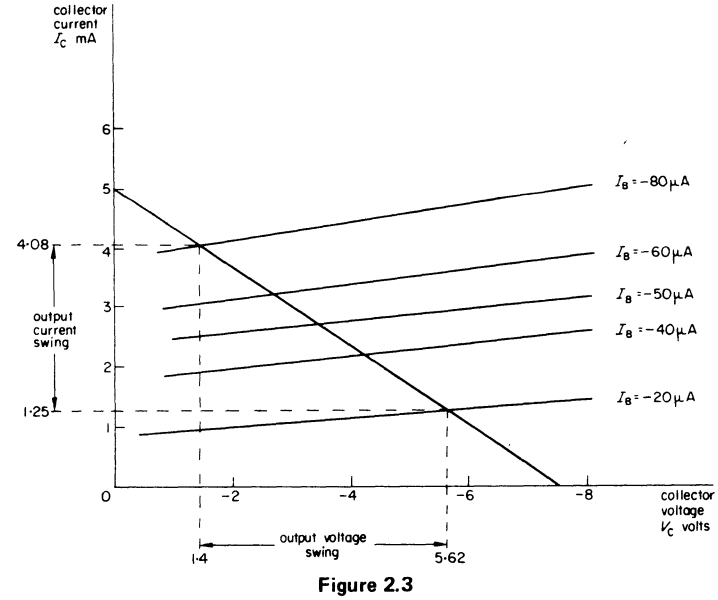


Figure 2.3

The characteristic for a base current of −50 μA can again be drawn by taking the mean of the ones corresponding to base currents of −40 and −60 μA. The load line can be superimposed

on the characteristics as shown in figure 2.3. From figure 2.3, output-voltage swing v_0 is 4·22 V. The input-voltage swing v_{in} is $i_b r_{in}$, where i_b is the base-current swing, and r_{in} is the a.c. input resistance of the amplifier.

Therefore

$$v_{in} = 60 \times 10^{-6} \times 1{\cdot}25 \times 10^{3} = 75 \text{ mV}$$

$$\text{voltage gain } A_v = \frac{v_o}{v_{in}} = \frac{4{\cdot}22}{75 \times 10^{-3}} = 56{\cdot}3$$

From figure 2.3, output-current swing i_o is 2·83 mA. Input base-current swing i_{in} is 60 μA

therefore

$$\text{current gain } A_L = \frac{i_o}{i_{in}} = \frac{2{\cdot}83 \times 10^{-3}}{60 \times 10^{-6}} = 47{\cdot}2$$

$$\text{power gain } A_p = v_o i_o / v_{in} i_{in} = A_v A_i$$

$$= 56{\cdot}3 \times 47{\cdot}2$$

$$= 2657$$

If this transistor were used in a common-base amplifier with the same load resistor and supply voltage, the voltage gain would be of similar value (that is, approximately 50). However, as the current gain of the common-base amplifier is approximately 0·95 to 0·98, the power gain would be of the order of 45. Also the input resistance is very low, at approximately 30 to 100 Ω.

Hence, the common-base circuit is unsuitable for multistage amplifiers because its current and power gains are low when compared with the corresponding common-emitter values. Also its low input resistance seriously shunts the load resistor of the previous stage, thereby reducing the output voltage from that stage and causing a corresponding fall in overall gain.

2.3 Amplifier with fixed bias

The circuit shown in figure 2.4 is that of a simple transistor amplifier. Estimate the value of the collector load-resistor R_c and the bias resistor R_B, if the mean (quiescent) d.c. collector current and voltage values are 9·2 mA *and 4·4* V *respectively. The transistor has a d.c. current gain of 115 and V_{BE} is 0·7* V.

To improve the d.c. stabilisation of the circuit the bias is to be obtained by returning the bias resistor to the collector. Draw a circuit diagram to show how this can be done without introducing unwanted a.c. feedback. Calculate suitable values for the components required and compare the relative merits of this method of d.c. stabilisation with other methods.

(ET5)

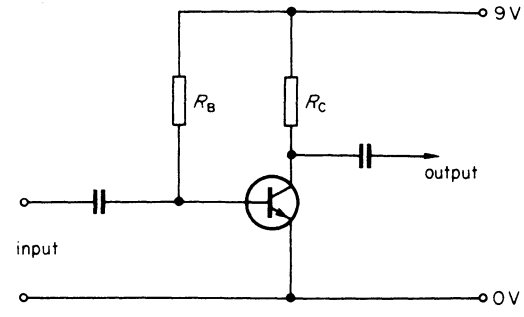


Figure 2.4

Voltage drop across R_C = 9 − 4·4 = 4·6 V

therefore

$$R_C = \frac{4{\cdot}6}{9{\cdot}2 \times 10^{-3}} = 500\ \Omega$$

Base potential = 0·7 V

therefore

voltage drop across R_B = 9 − 0·7 = 8·3 V

$$\text{Base current } I_B = I_C / h_{FE} = \frac{9{\cdot}2 \times 10^{-3}}{115} = 80\ \mu\text{A}$$

therefore

$$R_B = \frac{8{\cdot}3}{80 \times 10^{-6}} = 103{\cdot}8\ \text{k}\Omega$$

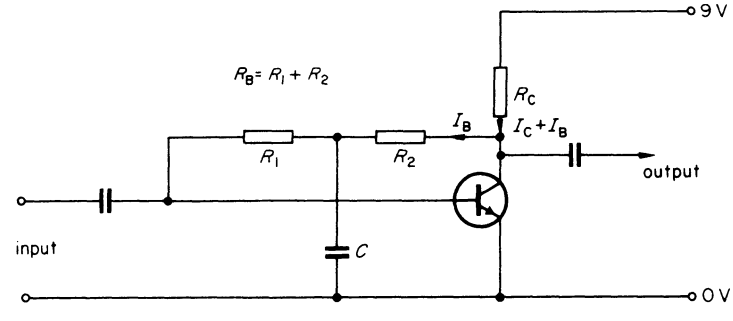


Figure 2.5

Assuming the values of base and collector currents in figure 2.5 to be the same as those in figure 2.4

collector potential $V_C = 9 - (I_C + I_B)0{\cdot}5$

$= 9 - (9{\cdot}28 \times 0{\cdot}5)$

$= 4{\cdot}36$ V

voltage drop across $R_B = 4{\cdot}36 - 0{\cdot}7$

$= 3{\cdot}66$ V

therefore

$$R_B = \frac{3{\cdot}66}{80 \times 10^{-6}} = 45{\cdot}8\ \text{k}\Omega$$

The capacitor C has to provide a low-resistance path to earth for the a.c. feedback component. If R_1 (which shunts R_L) is small, it seriously reduces the effective collector load-resistance. Similarly, a small R_2 reduces the input resistance of the amplifier. Usually therefore, R_1 and R_2 are made approximately equal, and the capacitor is chosen so that its reactance at the lowest signal-frequency is small compared with the resistance value. In this example, R_1 and R_2 would each be approximately 23 kΩ. A 4 μF capacitor could then be chosen, as it would have a reactance of approximately 800 Ω at a signal frequency of 50 Hz.

Two alternative methods of stabilisation are

(1) the use of a decoupled emitter-resistor alone (see section 2.4)

(2) the use of a decoupled emitter-resistor together with potential-divider stabilisation (see section 2.6).

Both the collector-base resistor method used in this example and the decoupled emitter-resistor method are equally effective, but the latter method involves using one extra resistor (the emitter-resistor). In both uses, the value of the bias resistor R_B is determined by the required base current. When potential-divider stabilisation is used however, a bleed current as well as the base current flows through the upper bias-resistor, and this widens the choice of resistor value. This is the best method of stabilisation and is the most used in practical amplifier circuits.

2.4 Amplifier with emitter resistor

Explain why the circuit of figure 2.6 gives better d.c. stability than one in which the emitter is connected directly to the 0 V line.

The transistor used has negligible leakage current at room temperature and a d.c. current gain (h_{FE}) of 100. Under quiescent conditions the collector current is 4 mA *and V_{BE} is 660* mV. *Determine a suitable value for R_B.*

If the amplifier a.c. current gain (A_i) is 90 and the a.c. input resistance is 800 Ω, calculate the voltage gain, assuming that all capacitors have negligible reactance at the working frequency of operation.

Explain briefly what the effect would be of removing C_E from the circuit.

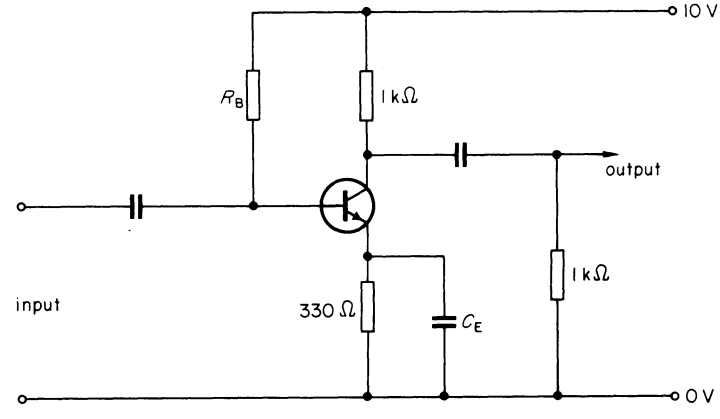


Figure 2.6

In the circuit of figure 2.4, in which the emitter is connected directly to the 0 V line, the quiescent point is fixed by the base current flowing through R_B. If the base-emitter voltage drop is negligible, then the value of the base current can be calculated from $I_B = V_{CC}/R_B$.

However, if the *temperature* of the transistor increases, the leakage current also increases, thereby changing the values of collector current, collector voltage, and base current; for d.c. collector current = $I_C + I'_{CO}$ (where I_C is the component due to the amplifying action on the base current I_B, and I'_{CO} is the leakage current), and d.c. base current = $I_B - I'_{CO}$. Hence, with increase in leakage current, the total collector current increases and the total base current decreases.

These changes cause the operating point of the amplifier to drift, and this can distort the output voltage. In power amplifiers, the increase in collector current can cause a further increase in temperature, which again increases the leakage current, thus producing a cumulative effect that can lead to the eventual destruction of the transistor, and is known as *thermal runaway*.

When the emitter resistor is employed, as shown in figure 2.6, any increase in collector current produces an increase in emitter current, which thereby causes a larger voltage drop across the emitter resistor R_E. This reduces the forward bias voltage V_{BE}, reducing the collector current and restoring it very nearly to its original value. This reasoning applies equally well to variations in collector current caused either by supply voltage changes or by changes in the d.c. current gain of the transistor. Thus, the circuit of figure 2.6 gives better d.c. stability than the one in which R_E is connected directly to the 0 V line.

In the circuit of figure 2.6, the emitter current I_E is given by

$$I_E = \frac{(h_{FE} + 1)I_C}{h_{FE}}$$

$$= \frac{101 \times 4 \times 10^{-3}}{100} = 4{\cdot}04 \text{ mA}$$

emitter voltage $= 4{\cdot}04 \times 10^{-3} \times 330$

$= 1{\cdot}33$ V

base voltage $= 1{\cdot}33 + 0{\cdot}66$

≈ 2 V

therefore voltage drop across R_B is 8 V

$$\text{base current } I_B = I_C/h_{FE} = \frac{4 \times 10^{-3}}{100} = 40\,\mu\text{A}$$

therefore

$$R_B = \frac{8}{40 \times 10^{-6}} = 200 \text{ k}\Omega$$

output voltage $v_o = i_c R_L$

input voltage $v_{in} = i_b R_{in}$

where

R_L = load resistor

R_{in} = a.c. input resistance of the amplifier

i_c = a.c. collector current

i_b = a.c. base current

therefore

$$\text{voltage gain } A_V = v_o/v_{in} = \frac{i_c R_L}{i_b R_{in}}$$

$$= \frac{A_i R_L}{R_{in}} = \frac{90 \times 500}{800}$$

$$= 56{\cdot}25$$

(*Note*: R_L comprises the 1 kΩ load resistor and the parallel output resistor of 1 kΩ; that is, 500 Ω.)

If C_E were removed, an a.c. voltage would be developed across R_E and this would oppose the a.c. input voltage to the transistor. Therefore the net a.c. base-emitter voltage would fall and so would the a.c. output voltage, thereby effectively reducing the voltage gain of the amplifier. This effect is known as *negative feedback.*

2.5 Amplifier with collector-base resistor

What is meant by the expression 'stabilisation of the operating point' when used in conjunction with a common-emitter connected transistor amplifier? Explain how d.c. stability is obtained in the amplifier circuit shown in figure 2.7.

The circuit is modified by connecting a resistor in series with the emitter and increasing the supply voltage so that the value of quiescent base current is unchanged. State how the following amplifier properties will alter (i) d.c. stability; (ii) voltage gain; (iii) input and output a.c. resistances.

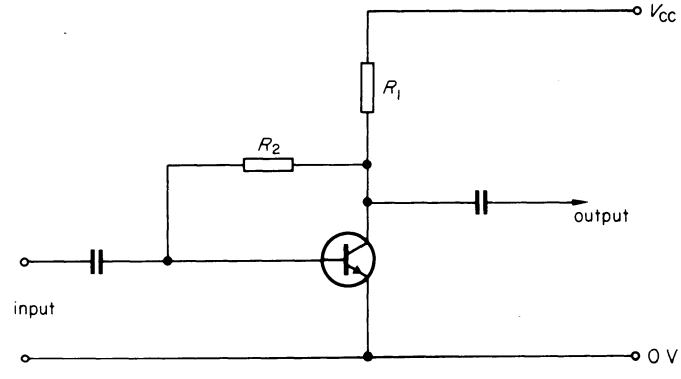


Figure 2.7

Stabilisation of the operating point implies maintaining the d.c. conditions in the amplifier as constant as possible, when supply voltage, temperature, transistor d.c. current gain, or any other parameter, varies.

In figure 2.7, if the collector current increases because of change in any of the above mentioned parameters, the collector voltage V_C will fall. Therefore, the d.c. base current I_B will fall (as $I_B = V_C/R_2$; neglecting the base-emitter voltage V_{BE}). Hence, the collector current I_C (that is, $h_{FE}I_B$) will also fall towards its original value. Similarly, if I_C decreases, V_C and I_B will rise, so that I_C then

rises to offset the original decrease. Thus, the operating point has been stabilised.

If a resistor is connected in series with the emitter

(i) d.c. stability will be improved because of the d.c. negative feedback;

(ii) voltage gain will be decreased because of the a.c. negative feedback;

(iii) input and output a.c. resistances will both decrease.

2.6 Amplifier with potential-divider stabilisation

Explain why stabilisation of the operating point is necessary in a transistor amplifier and how it is achieved in the circuit shown in figure 2.8.

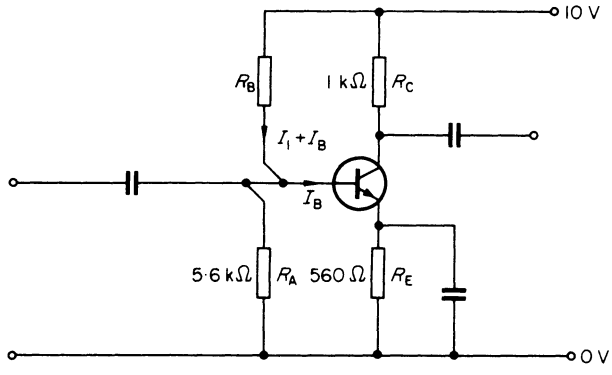


Figure 2.8

The input characteristics of the silicon transistor used in the circuit of figure 2.8 are shown in the graph of figure 2.9. Under quiescent operating conditions, the d.c. voltage across R_E is 3·5 V and the base current is 30 μA. Assuming zero leakage current, estimate the value of R_B. Calculate the voltage gain of the stage, assuming that it is coupled to an identical stage via a capacitor of negligible impedance, that R_E is adequately decoupled, and that the a.c. and d.c. current gains are the same.

(ET5)

The necessity for stabilisation of the operating point in a transistor amplifier has been dealt with in the first part of section 2.4.

In the amplifier shown in figure 2.8, which employs potential-divider and emitter-resistor stabilisation, the values of R_B and R_A are chosen such that the total current flowing through them is very much larger than the d.c. base current of the transistor (usually by a factor of 10). Thus variations in d.c. base current arising from change in leakage current have little effect on the d.c. conditions.

The effect of the emitter resistor R_E is to compensate for any change in d.c. collector current (that results from leakage current change, supply voltage variations, etc.) by producing a change in transistor drive-voltage V_{BE}, and thereby restoring the collector current towards its original value (as discussed in section 2.4).

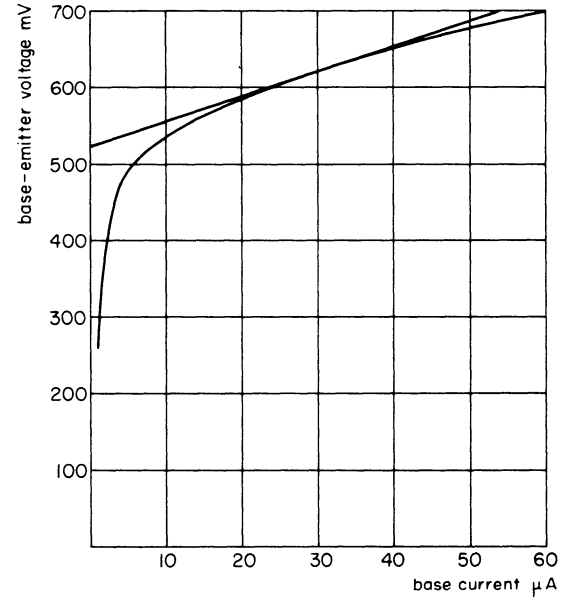


Figure 2.9

From figure 2.9, when $I_B = 30\,\mu A$, $V_{BE} = 625$ mV
therefore

voltage at the junction of R_A and $R_B = 3{\cdot}5 + 0{\cdot}625$
$= 4{\cdot}125$ V

current through R_A $\quad I = \dfrac{4{\cdot}125}{5{\cdot}6 \times 10^3} = 0{\cdot}737$ mA

therefore

$$R_B = \frac{10 - 4{\cdot}125}{I + I_B} = \frac{5{\cdot}875}{767 \times 10^{-6}}$$

$= 7{\cdot}7\ k\Omega$

The transistor d.c. current gain

$$h_{FE} = I_C/I_B \approx I_E/I_B$$

$$I_E = 3{\cdot}5/560 = 6{\cdot}25 \text{ mA}$$

therefore

$$h_{FE} = 6250/30 = 208$$

To determine the transistor a.c. input resistance h_{ie}, a tangent is drawn on figure 2.9 at the point corresponding to a d.c. base current of 30 μA.

$$h_{ie} = \frac{\text{change in base-emitter voltage } V_{BE} \text{ (in mV)}}{\text{corresponding change in base current } I_B \text{ (in } \mu\text{A)}}$$

$$= \frac{(700 - 525)\,10^{-3}}{(53 - 0)\,10^{-6}} = 3{\cdot}3 \text{ k}\Omega$$

For the amplifier, the effective a.c. input circuit is shown in figure 2.10.

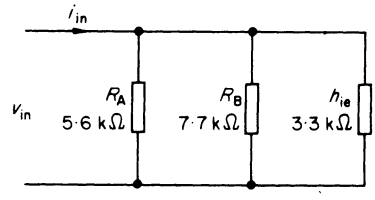


Figure 2.10

The amplifier a.c. input resistance r_{in} is given by

$$\frac{1}{r_{in}} = \frac{1}{5{\cdot}6} + \frac{1}{7{\cdot}7} + \frac{1}{3{\cdot}3}$$

$$= 0{\cdot}179 + 0{\cdot}130 + 0{\cdot}303$$

$$= 0{\cdot}612 \text{ mS}$$

$$r_{in} = 1{\cdot}6 \text{ k}\Omega$$

When this amplifier is loaded by an identical stage, the input resistance of the second stage will shunt the load resistor of the first stage, thereby reducing the net resistance to R'_L, where

$$\frac{1}{R'_L} = \frac{1}{R_L} + \frac{1}{r_{in}} = \frac{1}{1} + \frac{1}{1{\cdot}6}$$

$$= 2{\cdot}6/1{\cdot}6$$

therefore

$$R'_L = 615\ \Omega$$

Consider an r.m.s. input voltage V_{in} of 33 mV, then r.m.s. base current

$$I_b = V_{in}/h_{ie} = \frac{33 \times 10^{-3}}{3{\cdot}3 \times 10^{3}} = 10\,\mu\text{A}$$

As a.c. current gain h_{fe} = d.c. current gain h_{FE} = 208, r.m.s. collector current

$$I_c = 2{\cdot}08 \text{ mA}$$

therefore r.m.s. output voltage

$$V_o = I_c R'_L$$

$$= 2{\cdot}08 \times 10^{-3} \times 615$$

$$= 1{\cdot}28 \text{ V}$$

$$\text{Amplifier voltage gain } A_v = V_o/V_{in} = \frac{1{\cdot}28}{33 \times 10^{-3}}$$

$$= 38{\cdot}8$$

2.7 Design of practical amplifier

In the common-emitter amplifier shown in figure 2.11, the collector current of the transistor is 5 mA *and its d.c. current gain* $h_{FE} = 50$. *If the voltage drop across* R_E *is 2* V, *and the collector-emitter and base-emitter voltages of the transistor are 4* V *and 0·5* V *respectively, determine the values of all the labelled components if the lowest signal frequency is 50* Hz.

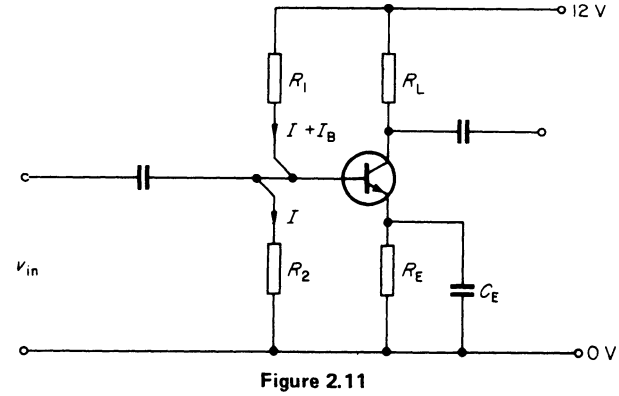


Figure 2.11

Voltage drop across load resistor = 12 − 4 − 2

= 6 V

therefore

$$R_L = \frac{6}{5 \times 10^{-3}} = 1{\cdot}2\ \text{k}\Omega$$

Transistor base current

$$I_B = I_C/h_{FE} = \frac{5 \times 10^{-3}}{50}$$

$$= 100\,\mu\text{A}$$

Emitter current

$$I_E = I_B + I_C = 5{\cdot}1\ \text{mA}$$

therefore

$$R_E = \frac{2}{5{\cdot}1 \times 10^{-3}} = 392\ \Omega$$

At the lowest signal frequency of 50 Hz, the reactance of C_E should be approximately one tenth of R_E.
Therefore

$$39{\cdot}2 = \frac{1}{2\pi \times 50\, C_E}$$

$$C_E = 81\,\mu\text{F}$$

In practice, C_E would be a 100 μF capacitor.

Let the bleed current $I = 10I_B = 1$ mA

Voltage on the base $V_B = 2 + V_{BE} = 2{\cdot}5$ V

therefore

$$R_2 = \frac{2{\cdot}5}{1 \times 10^{-3}} = 2{\cdot}5\ \text{k}\Omega$$

voltage drop across R_1 is (12 − 2·5) = 9·5 V
therefore

$$R_1 = \frac{9{\cdot}5}{1{\cdot}1 \times 10^{-3}} = 8{\cdot}6\ \text{k}\Omega$$

In a practical circuit, the nearest *preferred* values of each resistor would be used (that is, the nearest values contained in the standard 'list of preferred values' would be selected).

2.8 Voltage, current, and power gains

In a common-emitter amplifier, an a.c. input voltage of 10 mV *produces an output current of 2* mA *in the 500* Ω *load resistor. If the a.c. input resistance of the amplifier is 900* Ω*, determine the voltage gain, current gain, and power gain of the amplifier in* dB.

Amplifier output voltage

$$v_o = 2 \times 10^{-3} \times 500 = 1\ \text{V}$$

therefore

$$\text{voltage gain } A_v = v_o/v_{in} = \frac{1}{10 \times 10^{-3}} = 100$$

voltage gain A_v in dB = 20 log 100 = 40 dB

Input current

$$i_{in} = v_{in}/r_{in} = \frac{10 \times 10^{-3}}{900} = 11{\cdot}1\,\mu\text{A}$$

therefore

$$\text{current gain } A_i = i_o/i_{in} = \frac{2 \times 10^{-3}}{11{\cdot}1 \times 10^{-6}} = 180$$

current gain A_i in dB = 20 log 180 = 45·1 dB

Power gain $A_p = v_o i_o / v_{in} i_{in} = A_v A_i = 18\,000$

power gain A_p in dB = 10 log 18 000 = 42·55 dB

2.9 Stability factor of amplifier with collector-base resistor

A silicon transistor ($V_{BE} = 0{\cdot}6$ V) is used in the circuit of figure 2.12.

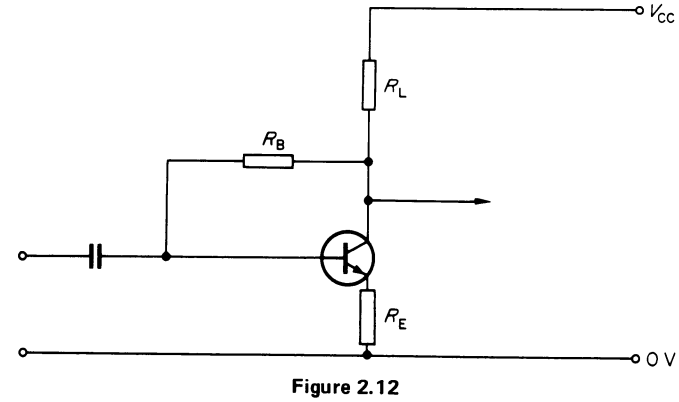


Figure 2.12

Given $V_{CC} = 24$ V, $R_L = 10$ kΩ, $R_E = 270$ Ω and $h_{FE} = 45$. If under quiescent conditions V_{CE} is 5 V, find from first principles (a) the value of the bias resistor R_B and (b) the stability factor $S = \delta I_C/\delta I_{CO}$.

(H.N.C.)

(a) In figure 2.12

$$V_{CC} = (I_C + I_B)R_L + V_{CE} + (I_C + I_B)R_E \qquad (2.2)$$

Also

$$I_C = h_{FE}I_B = 45I_B$$

therefore substituting in equation 2.2

$$24 = 46I_B \times 10 + 5 + 46I_B \times 0{\cdot}27$$

$$I_B = \frac{19}{472{\cdot}4} = 0{\cdot}04 \text{ mA}$$

Also

$$V_{CE} = I_B R_B + V_{BE}$$

$$5 = 0{\cdot}04R_B + 0{\cdot}6 \qquad (2.3)$$

$$R_B = 4{\cdot}4/0{\cdot}04 = 110 \text{ k}\Omega$$

(b) Substituting for V_{CE} from equation 2.3 into equation 2.2

$$V_{CC} = (I_C + I_B)R_L + I_B R_B + V_{BE} + (I_C + I_B)R_E$$

$$(V_{CC} - V_{BE}) = I_B(R_E + R_B + R_L) + I_C(R_E + R_L)$$

Multiply both sides by h_{FE}

$$h_{FE}(V_{CC} - V_{BE}) = h_{FE}I_B(R_E + R_B + R_L) + h_{FE}I_C(R_E + R_L) \qquad (2.4)$$

Now

collector current = d.c. component + leakage current

therefore

$$I_C = h_{FE}I_B + (h_{FE} + 1)I_{CO}$$

where I_{CO} is the value of common-base leakage current. Then

$$h_{FE}I_B = I_C - (h_{FE} + 1)I_{CO}$$

Substituting in equation 2.4 for $h_{FE}I_B$

$$h_{FE}(V_{CC} - V_{BE}) = (R_E + R_B + R_L)[I_C - (h_{FE} + 1)I_{CO}] + h_{FE}I_C(R_E + R_L)$$

$$= I_C[(R_E + R_B + R_L) + h_{FE}(R_E + R_L)] - I_{CO}(h_{FE} + 1)(R_E + R_B + R_L)$$

Considering small changes in I_C and I_{CO}, δI_C and δI_{CO}, respectively

$$0 = \delta I_C[R_B + (h_{FE} + 1)(R_E + R_L)] - \delta I_{CO}(h_{FE} + 1)(R_E + R_B + R_L)$$

therefore stability factor

$$S = \delta I_C/\delta I_{CO} = \frac{46 \times 120{\cdot}27}{110 + 46(10{\cdot}27)} = 9{\cdot}5$$

Note that the stability factor is a measure of the d.c. stability of the circuit when leakage current changes. In this example, if I_{CO} increased by 1 μA, the collector current would increase by only 9·5 μA. Therefore, a circuit should have as low a value of stability factor as possible, the minimum value being achieved in the common-base amplifier (where $S = 1$).

2.10 Stability factor of amplifier with potential-divider stabilisation

The circuit of figure 2.13 uses a silicon transistor with $h_{FE} = 60$, $V_{BE} = 0{\cdot}6$ V, $V_{CC} = 20$ V and $R_L = 4$ kΩ. It is desired to establish a quiescent point at $V_{CE} = 10$ V, $I_C = 2$ mA with a stability factor $S = 5$. Calculate the values of R_E, R_1 and R_2, proving any formula used. (H.N.C.)

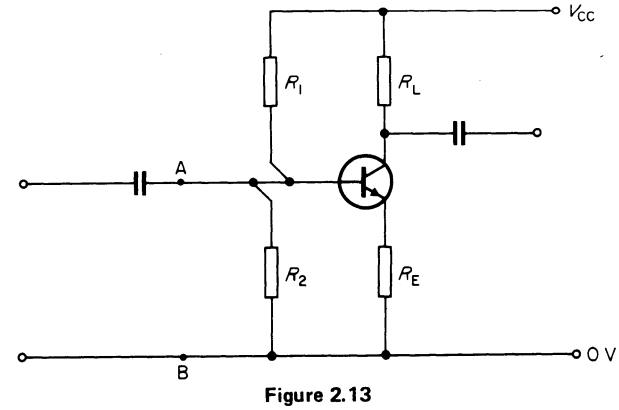


Figure 2.13

The circuit shown in figure 2.13 contains three independent loops which makes the analysis fairly complicated. Thus, it is far easier to use the Thévenin equivalent of the input circuit; that is, an active network, having two terminals A and B with a load connected across them, can be considered to be a single source of e.m.f. E with an internal resistance r. E is equal to the potential difference between A and B with the load disconnected, and r is the resistance of the network measured between A and B with the load disconnected and any sources of e.m.f. replaced by their internal resistances. In this example

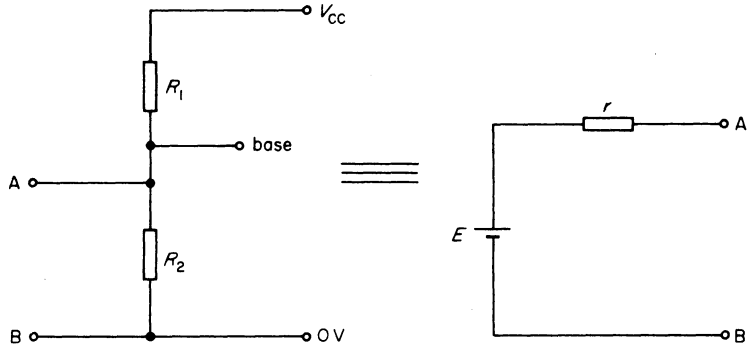


Figure 2.14

$$E = V_{CC}R_2/(R_1 + R_2)$$

and

$$r = R_1R_2/(R_1 + R_2)$$

Therefore, the circuit of figure 2.13 now becomes effectively the circuit of figure 2.15.

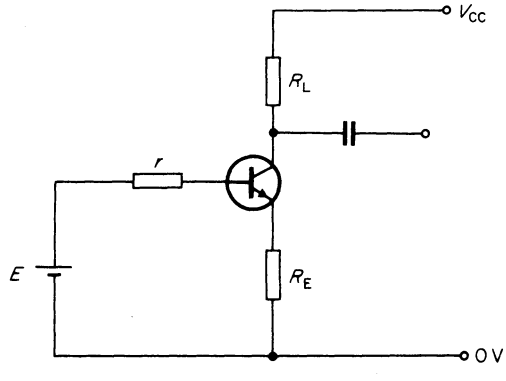


Figure 2.15

In figure 2.15 the current through R_E is $(I_C + I_B) \approx I_C = 2$ mA. Now

$$V_{CC} - V_{CE} = I_C(R_E + R_L)$$

therefore

$$R_E + R_L = \frac{10}{2 \times 10^{-3}} = 5\ \text{k}\Omega$$

$$R_E = 1\ \text{k}\Omega$$

Considering the input loop in figure 2.15

$$E - V_{BE} = (I_B + I_C)R_E + I_Br \qquad (2.5)$$
$$= I_B(R_E + r) + I_CR_E$$

Multiplying both sides by h_{FE}

$$h_{FE}(E - V_{BE}) = h_{FE}I_B(R_E + r) + h_{FE}I_CR_E \qquad (2.6)$$

Also

$$h_{FE}I_B = I_C - (h_{FE} + 1)I_{CO}$$

Substituting this value in equation 2.6

$$h_{FE}(E - V_{BE}) = [I_C - (h_{FE} + 1)I_{CO}](R_E + r) + h_{FE}I_CR_E$$
$$= I_C[r + (h_{FE} + 1)R_E] - I_{CO}(h_{FE} + 1)(R_E + r)$$

Considering small changes in I_C and I_{CO}, δI_C and δI_{CO} respectively

$$0 = \delta I_C[r + (h_{FE} + 1)R_E] - \delta I_{CO}(h_{FE} + 1)(R_E + r)$$

therefore

$$S = \frac{\delta I_C}{\delta I_{CO}}$$
$$= \frac{(h_{FE} + 1)(R_E + r)}{r + R_E(h_{FE} + 1)}$$

Substituting the values given

$$5 = \frac{61(1 + r)}{r + 61(1)}$$
$$5r + 305 = 61 + 61r$$
$$r = 244/56 = 4{\cdot}36\ \text{k}\Omega$$

Now base current $I_B = I_C/h_{FE} = 33{\cdot}3\ \mu\text{A}$
Then substituting values in equation 2.5

$$E - 0{\cdot}6 = 2{\cdot}033 \times 1 + 0{\cdot}033 \times 4{\cdot}36$$
$$E = 2{\cdot}78\ \text{V}$$

Also

$$E = V_{CC}R_2/(R_1 + R_2)$$

and

$$r = R_2R_1/(R_1 + R_2)$$

Therefore

$$R_1 = rV_{CC}/E = \frac{4{\cdot}36 \times 20}{2{\cdot}78} = 31{\cdot}4\ \text{k}\Omega$$

and

$$R_2 = \frac{ER_1}{V_{CC} - E} = \frac{2{\cdot}78 \times 31{\cdot}4}{20 - 2{\cdot}78} = 5\ \text{k}\Omega$$

2.11 Directed coupled amplifier

Explain briefly what is meant by the term 'drift' as applied to a direct-coupled transistor amplifier and state the factors upon which it depends.

In the direct-coupled amplifier shown in figure 2.16, given that the d.c. current gains h_{FE_1} and h_{FE_2} of Tr_1 and Tr_2 are 50 and 49 respectively, and that the base potential of Tr_2 is −2 V, determine the collector and emitter currents and voltages of Tr_2. The base-emitter voltage of Tr_1 can be neglected.

Explain why the d.c. stability of the second stage is superior to that of the first, and state how the first stage could be improved by using a thermistor.

(H.N.C.)

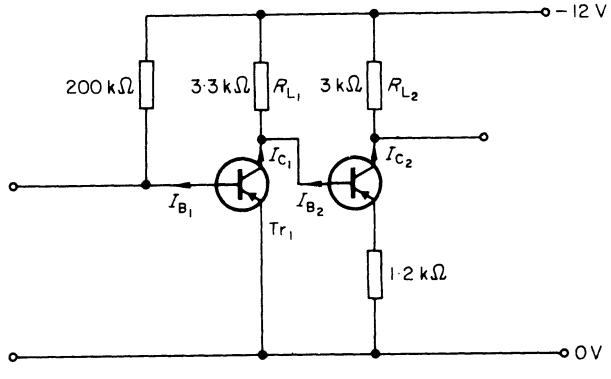


Figure 2.16

Drift is a gradual change in the output voltage or current of a d.c. amplifier when the input signal is maintained at a constant level.

In semiconductor d.c. amplifiers, drift depends upon (1) the parameters of the transistor used; (2) the collector supply-voltage. Item 1 refers to the temperature-dependent parameters of current gain, base-emitter voltage, and leakage current. The variations in item 2 are due to mains-voltage variations, and this effect can be minimised only by using a stabilised power supply. As V_{BE} of the first transistor can be neglected, the Tr_1 base current

$$I_{B_1} = \frac{12}{200 \times 10^3} = 60\ \mu\text{A}$$

therefore collector current of Tr_1

$$I_{C_1} = h_{FE_1}I_{B_1} = 50 \times 60 \times 10^{-6} = 3\ \text{mA}$$

The current flowing through R_{L_1} is $(I_{C_1} + I_{B_2})$ and the voltage drop across it is

$$(12 - 2) = 10\ \text{V}$$

therefore

$$10 = 3{\cdot}3(3 + I_{B_2})$$

$$I_{B_2} = \frac{0{\cdot}1}{3{\cdot}3} = 0{\cdot}03\ \text{mA}$$

Tr_2 collector current

$$I_{C_2} = h_{FE_2}I_{B_2} = 49 \times 0{\cdot}03 = 1{\cdot}47\ \text{mA}$$

Tr_2 emitter current

$$I_{E_2} = I_{C_2} + I_{B_2} = 1{\cdot}5\ \text{mA}$$

Tr_2 emitter voltage

$$V_{E_2} = -(1{\cdot}5 \times 1{\cdot}2) = -1{\cdot}8\ \text{V}$$

Tr_2 collector voltage

$$V_{C_2} = V_{CC} - I_{C_2}R_{L_2} = -[12 - 3(1{\cdot}47)] = 7{\cdot}59\ \text{V}$$

The d.c. stability of the second stage is superior to that of the first stage because of the effect of the 1·2 kΩ resistor, as explained in previous questions.

A thermistor has a negative *Temperature-coefficient of resistance*: that is, its resistance *decreases* with *increase* in temperature. Thus, if a thermistor is used as the collector load resistor, when leakage current increases with increase in temperature, the resistance of the thermistor will decrease; so that correct choice of thermistor temperature-coefficient will enable the collector voltage of Tr_1 to be maintained constant.

2.12 Frequency-response curve of *RC*-coupled amplifier

*Sketch a gain/frequency characteristic for a typical RC-coupled common-emitter transistor amplifier. Explain the reasons for the fall-off in the curve, label the 3-*dB *points, and briefly explain their significance.*

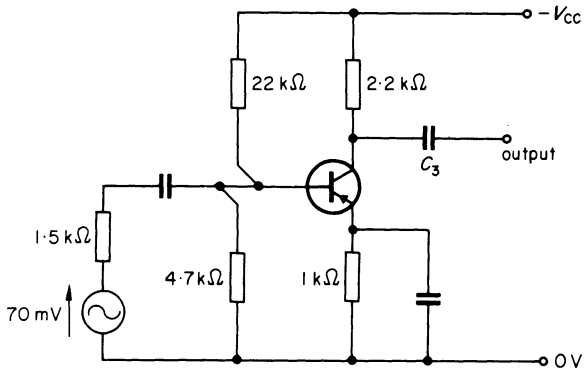


Figure 2.17

In the amplifier shown in figure 2.17, the transistor has an a.c. current gain h_{fe} *of 99 and has an a.c. input resistance of 1·1* kΩ. *It is connected via* C_3 *to another stage whose a.c. input resistance is 700* Ω. *Calculate the current flowing into the second stage, assuming that all capacitors have negligible reactance at the operating frequency. If* C_3 *is the main factor responsible for low-frequency cut-off, calculate its value such that the lower 3-*dB *point is 5* Hz.

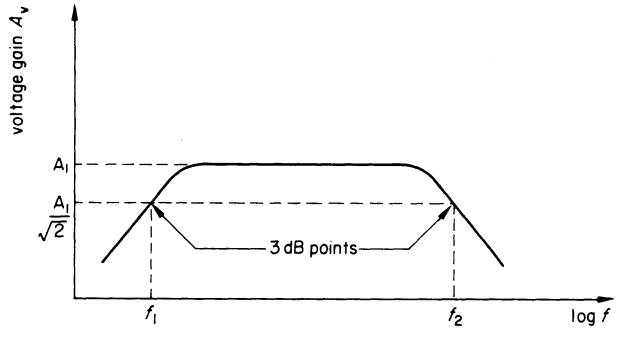


Figure 2.18

Figure 2.18 shows the *gain/frequency response* of an *RC*-coupled common-emitter amplifier. This is a graph of amplifier voltage gain A_v against frequency, where frequency has a logarithmic scale.

At *low* frequencies, the voltage gain decreases, because the reactance of the coupling capacitor increases. In consequence, more of the signal voltage is dropped across the coupling capacitor and the actual input voltage to the transistor decreases, thereby decreasing the voltage gain.

At *high* frequencies too, voltage gain falls off, because the reactances of the internal capacitances of the transistor decrease; and as these effectively shunt the load and reduce the overall load impedance, there is an inevitable decrease in output voltage and voltage gain.

Over the *medium* frequency range however, the voltage gain remains reasonably constant, as the capacitive reactances are negligible compared with the associated resistance values in the circuit.

The *3-dB points* are defined as the points at which the voltage gain falls to $1/\sqrt{2}$ of its maximum value. This fall in gain is expressed in dB as follows

$$20 \log A_1 - 20 \log \frac{A_1}{\sqrt{2}} = 20 \log \frac{A_1}{A_1/\sqrt{2}}$$

$$20 \log \sqrt{2} = 20 \times 0{\cdot}150 = 3 \text{ dB}$$

Hence, the name 3-dB points. The frequencies corresponding to these points define the *bandwidth* of the amplifier (see figure 2.18).

$$\text{bandwidth} = (f_2 - f_1) \text{ Hz}$$

The a.c. equivalent input circuit (for figure 2.17) is shown in figure 2.19.

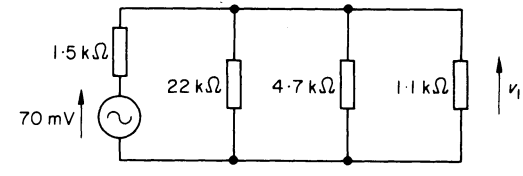


Figure 2.19

Considering the three resistors in parallel, then

$$\frac{1}{R} = \frac{1}{22} + \frac{1}{4{\cdot}7} + \frac{1}{1{\cdot}1}$$

$$= 0{\cdot}046 + 0{\cdot}213 + 0{\cdot}909 = 1{\cdot}168 \text{ mS}$$

therefore

$$R = 0{\cdot}856 \text{ k}\Omega$$

and

$$v_1 = \frac{0{\cdot}856}{1{\cdot}5 + 0{\cdot}856} \times 70 \times 10^{-3} = 25{\cdot}4 \text{ mV}$$

Then a.c. base current

$$i_b = \frac{v_1}{1{\cdot}1 \times 10^3} = 23{\cdot}1\,\mu\text{A}$$

and a.c. collector current

$$i_c = h_{fe} i_b = 99 \times 23{\cdot}1 \times 10^{-6}$$

$$= 2{\cdot}29 \text{ mA}$$

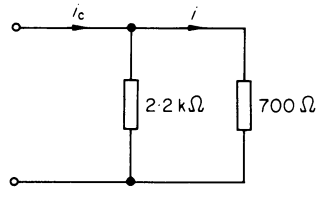


Figure 2.20

Part of the collector current is the input current i to the second stage (as shown in figure 2.20).
Therefore

$$i = 2.29 \times 10^{-3} \times \frac{2{\cdot}2}{2{\cdot}9} = 1{\cdot}74 \text{ mA}$$

At low frequencies, the output circuit is modified to that shown in figure 2.21 with its Thévenin equivalent circuit.

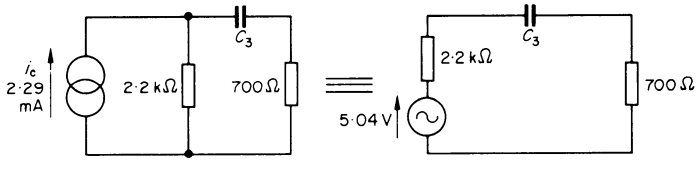


Figure 2.21

Using Thévenin's theorem, the equivalent voltage generator is given by

$$v = 2{\cdot}29 \times 2{\cdot}2 = 5{\cdot}04 \text{ V}$$

New value of current in the 700 Ω resistor is i'; and at the lower 3-dB point,

$$i' = \frac{i}{\sqrt{2}}$$

Therefore

$$\frac{5{\cdot}04}{\sqrt{(2{\cdot}9^2 + X_C^2)}} = \frac{1{\cdot}74}{\sqrt{2}}$$

which gives

$$X_C^2 = 8{\cdot}37$$

$$X_C = 2{\cdot}89 \text{ k}\Omega$$

At a frequency of 5 Hz

$$\frac{1}{2\pi \times 5C_3} = 2{\cdot}89 \times 10^3$$

$$C_3 \approx 11\,\mu\text{F}$$

2.13 Exercises

Exercise 2.1

The output characteristics of a transistor in common-emitter configuration can be regarded as straight lines between the following points

	$I_b - 20\,\mu$A		$I_b - 50\,\mu$A		$I_b - 80\,\mu$A	
V_{CE}(V)	1·0	8·0	1·0	8·0	1·0	8·0
I_C(mA)	1·1	1·3	3·3	4·1	6·0	8·0

Plot these graphs and add a load line for resistive load of 1 kΩ. The supply voltage is 9 V and the base current is 50 μA. Calculate (a) the collector current at the operating point; (b) the total variation in voltage across the 1 kΩ load, if the peak value of sinusoidal base current is 30 μA.
(Answers: 3·8 mA, 5·2 V) (ET3)

Exercise 2.2

The output characteristic of a silicon *npn* transistor consists of straight lines between the points given in the table below

I_B (μA)	70		40		10	
V_{CE}(V)	1·0	8·0	1·0	8·0	1·0	8·0
I_C (mA)	0·6	0·7	2·5	3·0	4·6	5·5

Plot the characteristics and draw a load line for a 1·6 kΩ load through an operating point at which $I_B = 40\mu A$ and $V_{CE} = 4$ V, and hence calculate (a) the quiescent value of collector current; (b) the supply voltage required; (c) the current for a sinusoidal signal input of 30μA peak.
(Answers: 2·7 mA, 8·3 V, 65) (ET3)

Exercise 2.3

A *pnp* transistor has the following (linear) characteristics

	Collector voltage		Base current
	3 V	10 V	μA
Collector current (mA)	1·0	1·6	−20
	2·1	2·9	−40
	3·2	4·2	−60
	4·3	5·4	−80

This transistor, with a load of 1 kΩ and a collector supply of 7·5 V is to be used in a simple common-emitter amplifier. Plot the characteristics given in the table and draw the load line. Give a circuit diagram and explain why the output voltage changes when a sinusoidal input signal is applied. State the phase relationship between the amplifier output and input.

Estimate the voltage gain when an input current of peak value 30μA varies sinusoidally about a mean of 50μA. The a.c. input resistance may be taken as 1·25 kΩ.
(Answer: 40·5) (ET4)

Exercise 2.4

A *pnp* power transistor has the following linear characteristics

Base current (mA)	Collector current (amps) for collector voltage of	
	−2·5 V	−17·5 V
−10	−0·67	−0·70
−30	−1·45	−1·65
−50	−2·33	−2·64

For a collector voltage of 8 V, estimate the value of common-emitter current gain β for the transistor and hence calculate the value of the common-base current gain α.

The transistor is to be used as a common-emitter amplifier having a collector load resistor of 6 Ω. If under no-signal conditions the base current is 30 mA and the collector voltage is 8 V, draw a suitable load line and estimate (a) the collector supply-voltage required; (b) the current gain of the amplifier; (c) the voltage gain of the amplifier, assuming that the input resistance is 5 Ω.
(Answers: 44, 0·98, 17·24 V, 41·1, 50) (ET4)

Exercise 2.5

In a common-emitter amplifier, the bias is provided by a single resistor R_B connected between the supply rail and the base. If the collector supply-voltage is 12 V, the base-emitter voltage of the transistor is 0·4 V and the transistor d.c. current gain h_{FE} is 40, determine the value of R_B and the load resistor required, if the d.c. base current is 50μA and the collector voltage is 6 V.
(Answers: 232 kΩ, 3 kΩ)

Exercise 2.6

If, in the amplifier of Question 2.5, an emitter resistor of 500 Ω is employed, decoupled by a capacitor C, determine the emitter current and emitter voltage. Also, determine the value of *C* if the lowest signal frequency is 50 Hz.
(Answers: 1·88 mA, 0·94 V, 64μF)

Exercise 2.7

In the circuit shown in figure 2.22, the collector voltage is 8 V and the collector current is 5 mA. Determine the value of the base current and of the d.c. current gain of the transistor. Also determine the value of R_B, stating any assumptions made.
(Answers: 60μA, 83, 133 kΩ)

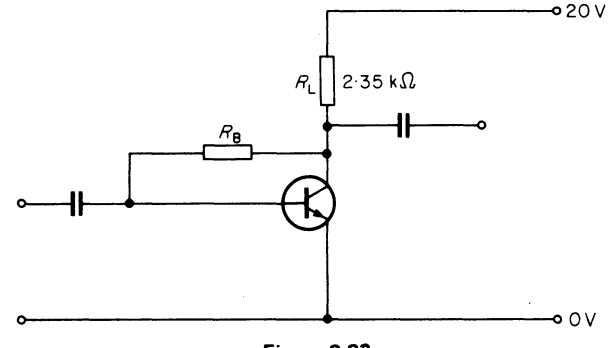


Figure 2.22

Exercise 2.8

In the common-emitter amplifier shown in figure 2.23, the collector current is 4 mA. Determine the values of R_1, R_2, and R_E, given that the transistor d.c. current gain h_{FE} is 80, V_{BE} is 0·5 V, and 1 V is dropped across R_E. Also determine the value of C_E if the lowest signal frequency is 40 Hz.
(Answers: 24·6 kΩ, 3 kΩ, 247 Ω, 162 μF)

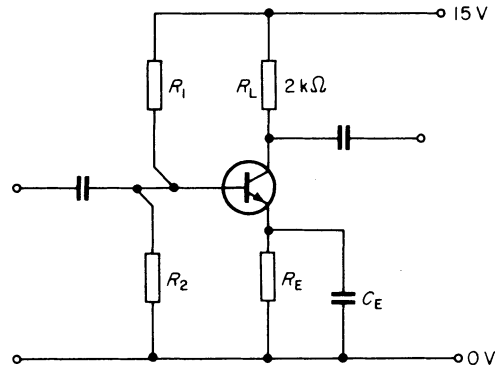


Figure 2.23

Exercise 2.9

In the amplifier of Exercise 2.8, an a.c. input voltage of 20 mV r.m.s. produces an r.m.s. base current of 25 μA. Given that the transistor a.c. current gain $h_{fe} = h_{FE}$, determine the input resistance of the amplifier and its voltage gain in dB.
(Answers: 800 Ω, 46 dB)

Exercise 2.10

(a) Explain how the circuit of figure 2.24 improves thermal stability compared with an unstabilised circuit.

(b) State the purpose of capacitor C_1.

(c) When a certain transistor is used in common-base configuration, it has a current gain of 0·99. A given change in temperature causes the leakage current to increase by 10 μA. Calculate the change in collector current for the same change in temperature when used in common-emitter configuration (i) when unstabilised; (ii) when used in the circuit shown in figure 2.24.
(Answers: 1 mA, 23·5 μA) (ET5)

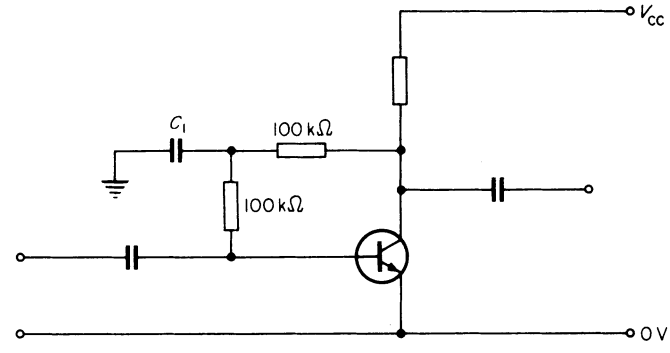


Figure 2.24

Exercise 2.11

The circuit shown in figure 2.25 is that of a basic transistor amplifier. Estimate the values of the collector load resistor R_L, and the bias resistor R_B, if the mean (quiescent) d.c. collector current and voltage values are 8·4 mA and 3·6 V, respectively. The transistor has a d.c. current gain h_{FE} of 100, and V_{BE} is 0·6 V.

To improve the d.c. stabilisation of the circuit, the bias is to be obtained by returning the bias resistor to the collector. Draw a circuit diagram to show how this can be done without introducing unwanted feedback. Calculate suitable values for the components required, given the lowest signal frequency is 40 Hz. Compare the relative merits of this method of d.c. stabilisation with other methods.
(Answers: 1 kΩ; 136 kΩ, 68 kΩ, 68 kΩ, C ≈ 3 μF) (H.N.C.)

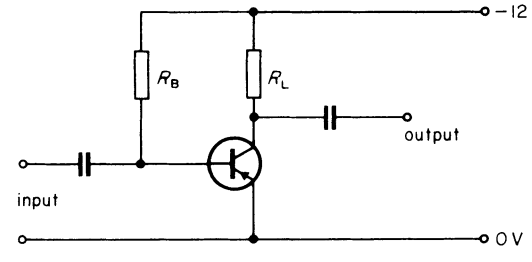


Figure 2.25

Exercise 2.12

Determine an expression for the stability factor S of a common-emitter amplifier, with a collector load resistor R_L and an emitter resistor R_E, the bias being supplied to the base through a single resistor R_B. Why is it desirable to keep this ratio small? Explain,

with the aid of circuit diagrams, two standard methods of reducing this ratio and state the effects that each has on the operation of the amplifier which conflict with their use in counteracting the effect of leakage current.

Answer: $S = \dfrac{(h_{FE} + 1)(R_E + R_B)}{R_B + R_E(h_{FE} + 1)}$ (H.N.C.)

Exercise 2.13

In the amplifier shown in figure 2.26, determine the output voltage, the current gain of the amplifier, and lower 3-dB frequency. (Answers: 4·6 V, 1450, 6·8 Hz)

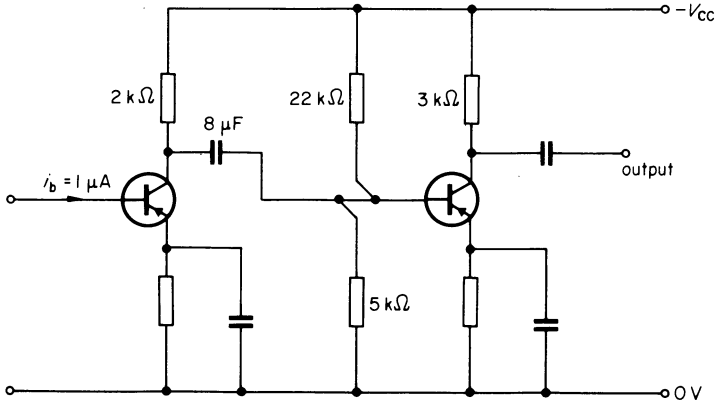


Figure 2.26

Exercise 2.14

Explain why stabilisation of the operating point is necessary in a transistor amplifier and how it is achieved in the circuit shown in figure 2.27. Discuss the factors affecting the choice of resistors R_1, R_2, and R_4.

If under no-signal conditions the transistor is to operate at $V_{CE} = -6$ V, $I_C = 10$ mA, $V_{BE} = -250$ mV, and $I_B = 0{\cdot}2$ mA, estimate suitable values for R_1 and R_3.

Estimate the lowest value of C_2 which can be used to give negligible reduction in gain at 100 Hz.
(Answers: 4·4 kΩ, 400 Ω, 80 μF) (ET5)

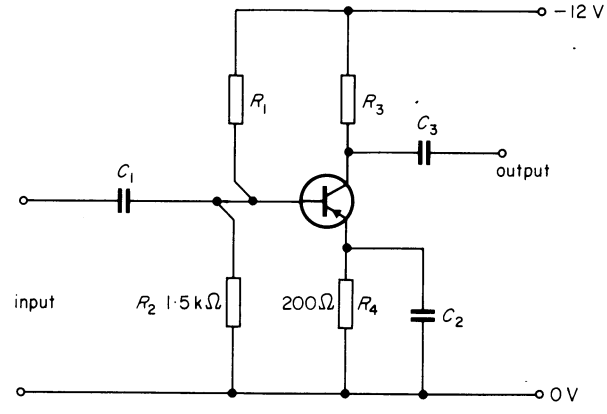


Figure 2.27

3 Equivalent circuits of small-signal, low-frequency amplifiers

3.1 Common-base equivalent-T circuit

Figure 3.1 shows the layout of the equivalent-T circuit of a transistor in its common-base configuration. Label the unmarked components and hence derive the equations for current gain and input impedance when a load R_L is connected.

Given that r_e = 20 Ω, r_b = 200 Ω, r_c = 2 MΩ and α = 0·99, find the current gain for a load resistance of 100 kΩ. Comment on the answer.

(ET3)

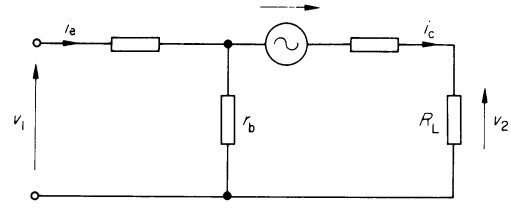


Figure 3.1

The resistor in the input circuit is r_e, which simulates the resistance of the forward-biased base-emitter diode, the one in the output circuit is r_c which simulates the resistance of the reversed-biased base-collector diode. The voltage generator has a value $\alpha r_c i_e$.

Applying Kirchhoff's law around the input and output loops

$$v_1 = i_e r_e + (i_e - i_c) r_b \tag{3.1}$$

$$0 = (i_e - i_c) r_b + \alpha i_e r_c - i_c (r_c + R_L) \tag{3.2}$$

From equation 3.2

$$i_c(r_b + r_c + R_L) = (r_b + \alpha r_c) i_e$$

then current gain

$$A_i = i_c/i_e = \frac{r_b + \alpha r_c}{r_b + r_c + R_L} \tag{3.3}$$

Substituting for i_c from equation 3.3 into equation 3.1

$$v_1 = i_e(r_e + r_b) - \frac{r_b(r_b + \alpha r_c) i_e}{r_b + r_c + R_L}$$

input resistance

$$r_{in} = v_1/i_e = r_e + r_b - \frac{r_b(r_b + \alpha r_c)}{r_b + r_c + R_L}$$

$$= r_e + \frac{r_b[R_L + r_c(1 - \alpha)]}{r_b + r_c + R_L}$$

Substituting the values given into equation 3.3, current gain

$$A_i = \frac{200 + 0{\cdot}99(2 \times 10^6)}{200 + 2(10^6) + 10^5}$$

$$\approx \frac{1{\cdot}98 \times 10^6}{2{\cdot}1 \times 10^6}$$

$$= 0{\cdot}943$$

As expected the current gain of the common-base amplifier is less than unity. (*Note* although R_L was large in this case, the actual current gain 0·943 is still very close to its short-circuit value of 0·99.)

3.2 Common-emitter equivalent-T circuit

Draw a circuit diagram of a common-emitter amplifier employing potential-divider stabilisation and a decoupled emitter resistor. If the load resistor of such a stage is 4 kΩ, the resistance of the signal source is 600 Ω and the T parameters of the transistor are r_e = 25 Ω, r_b = 400 Ω, r_c = 1 MΩ, α = 0·98, determine from first principles (a) the voltage and current gains; (b) the power gain in dB*; (c) the input and output resistances of the amplifier.*

(H.N.C.)

The circuit diagram of the common-emitter amplifier has been drawn and discussed in chapter 2; the equivalent-T circuit is shown in figure 3.2.

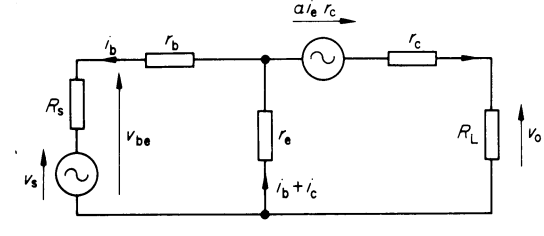


Figure 3.2

(a) Using Kirchhoff's laws around the input and output loops

$$v_s = 1000i_b + 25(i_b + i_c) \quad (3.4)$$

$$0{\cdot}98 \times 10^6 i_e - 1004 \times 10^3 i_c - 25(i_b + i_c) = 0 \quad (3.5)$$

The last term in equation 3.5 is negligible compared with the other two terms in the equation. Also, $i_e = i_c + i_b$; therefore, substituting in equation 3.5

$$980i_b - 980i_c = 1004i_c$$

therefore current gain

$$A_i = i_c/i_b = 980/24 = 40{\cdot}8$$

Substituting for i_c in equation 3.4

$$v_s = 1025i_b + 25 \times 40{\cdot}8i_b = 2045i_b$$

Also

$$v_o = 4000i_c = 163\,200i_b$$

therefore voltage gain

$$A_V = \frac{163\,200i_b}{2045i_b} = 79{\cdot}8$$

(b) Power gain

$$A_p = 10 \log A_v A_i = 10 \log 79{\cdot}8 \times 40{\cdot}8 = 35{\cdot}1 \text{ dB}$$

(c) Input resistance

$$r_{in} = v_{be}/i_b$$

$$= \frac{400i_b + 25(i_b + i_c)}{i_b}$$

$$= \frac{(425 + 25 \times 40{\cdot}8)i_b}{i_b}$$

$$= 1445\ \Omega$$

The output resistance of an amplifier is defined as the resistance of the amplifier viewed from the output terminals when all the signal sources have been replaced by their internal resistances. Hence, if the load resistor in the equivalent circuit is replaced by a voltage generator e, the output resistance can be determined by finding the ratio of e to i, where i is the current supplied by the voltage generator e as shown in figure 3.3.

Using Kirchhoff's law around loops (1) and (2)

$$1000(i - i_1) = 25i_1 \quad (3.6)$$

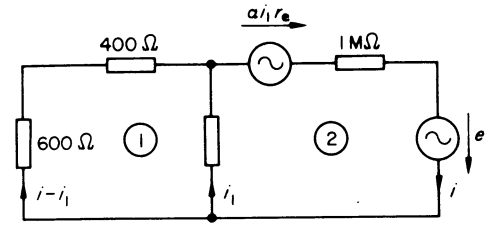


Figure 3.3

$$e + 0{\cdot}98 \times 10^6 i_1 = 25i_1 + 10^6 i \quad (3.7)$$

Again the first term on the right-hand side of equation 3.7 is negligible compared with the other terms in the equation. From equation 3.6

$$i_1 = \frac{1000i}{1025} = 0{\cdot}976i$$

Substituting for i_1 in equation 3.7

$$e = 10^6 i - 0{\cdot}98 \times 10^6 \times 0{\cdot}976i = 0{\cdot}044 \times 10^6 i$$

therefore output resistance

$$r_o = e/i = 44\ \text{k}\Omega$$

3.3 Measurement of *h*-parameters from transistor characteristics

Why are the h-parameters of a junction transistor more useful than T-parameters?

Sketch the input and output characteristics of a transistor in the common-emitter mode and clearly indicate how the following parameters may be estimated, (a) h_{ie} (b) h_{fe} (c) h_{oe}. Assign suitable units for each of these parameters and give typical values.

Explain why the a.c. input resistance of the transistor when used as an amplifier is different in value from h_{ie}.

(ET4)

There are three main disadvantages of T-parameters as compared with *h*-parameters:

(1) It is difficult to measure T-parameters directly, but *h*-parameters can be estimated directly from the static characteristics of the transistor or may be determined by simple experiment (see section 3.4).

(2) The expressions derived for current and voltage gains and input and output impedances of an amplifier from its equivalent-T circuit are cumbersome.

(3) A different equation is required for each of the three T-circuit configurations.

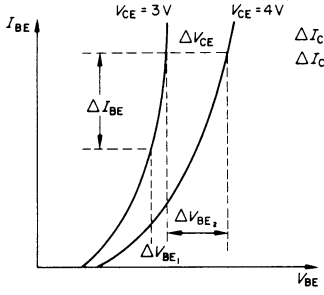


Figure 3.4a

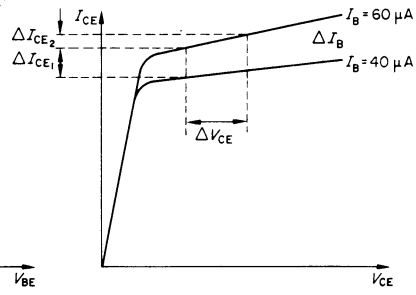


Figure 3.4b

(a) h_{ie} = the input resistance of the transistor with the output short-circuited to a.c. with constant collector voltage V_{CE}

therefore from the input characteristics shown in figure 3.4a

$$h_{ie} = \Delta V_{BE_1}/\Delta I_{BE}$$

(b) h_{fe} = the forward current gain with the output short-circuited to a.c. at constant collector voltage V_{CE}.

From the output characteristics of figure 3.4b

$$h_{fe} = \Delta I_{CE}/\Delta I_{BE}$$

(c) h_{oe} = the output admittance with the input open-circuited to a.c. at constant base current I_B

From figure 3.4b

$$h_{oe} = \Delta I_{CE_2}/\Delta V_{CE}$$

If it was required to find h_{re}

h_{re} = the reverse voltage transfer with the input open-circuited to a.c. at constant base current I_B

From figure 3.4a

$$h_{re} = \Delta V_{BE_2}/\Delta V_{CE}$$

Typical values for an a.f. transistor are

h_{ie} = 2·2 kΩ, h_{fe} = 55, h_{oe} = 12·5 μS, h_{re} = 3·6 x 10^{-4}

The a.c. input resistance of a transistor amplifier will normally be less than the h_{ie} value of the transistor because of the shunting effect of the bias resistors on h_{ie}.

3.4 *h*-parameter equations for a network

With reference to figure 3.5, write down the two equations relating V_1, V_2, I_1 and I_2 in terms of the circuit h-parameters. Hence define the h-parameters and explain how they may be obtained experimentally.

Figure 3.5

Draw the equivalent circuit of a network in terms of its h-parameters and insert typical values for a low power common-emitter transistor.

(ET5)

$$V_1 = h_{11}I_1 + h_{12}V_2 \quad (3.8)$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \quad (3.9)$$

These parameters are defined for low frequency a.c. conditions. Therefore, considering a constant value of output voltage (that is, short-circuited output terminals for a.c.), V_2 = 0.
Substituting in equations 3.8 and 3.9

$h_{11} = V_1/I_1$ = the input resistance with short-circuited output terminals

$h_{21} = I_2/I_1$ = the forward current gain with short-circuited output terminals

Similarly, considering a constant value of input current (that is, open-circuited input terminals to a.c.), I_1 = 0.
Substituting in equation 3.8 and 3.9

$h_{12} = V_1/V_2$ = reverse voltage ratio with open-circuited input

$h_{22} = I_2/V_2$ = output admittance with open-circuited input

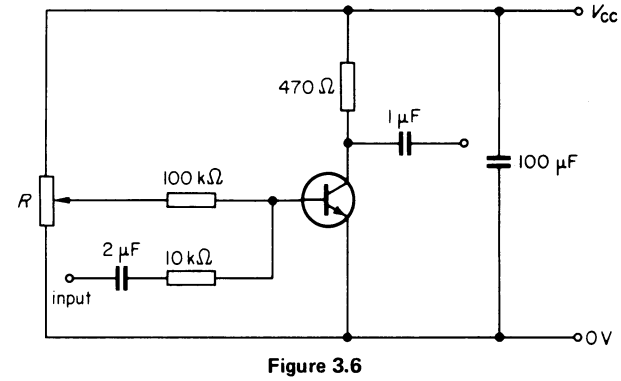


Figure 3.6

These values may be obtained experimentally from a circuit similar to the circuit shown in figure 3.6, where the low reactance of the 100 μF capacitor simulates the short-circuit output condition and the 100 kΩ resistor simulates the open-circuit input condition. The operating point is initially fixed by the potentiometer setting, then a signal generator is connected between the input and 0 V line and a signal of about 20 mV is applied at a frequency of 1 kHz. The a.c. collector and base voltages v_c and v_b are measured, from which the input base current and output collector current can then be calculated using the appropriate resistances; hence, h_{ie} and h_{fe} can be determined.

The signal generator is then reconnected in series with the 470 Ω resistor and a signal of about 800 mV is applied. The base-emitter voltage and the voltage across the 470 Ω resistor are then measured, and from these h_{re} and h_{oe} are determined.

The equivalent circuit of a low power common-emitter transistor is shown in figure 3.7; the typical *h*-values have already been given in section 3.3.

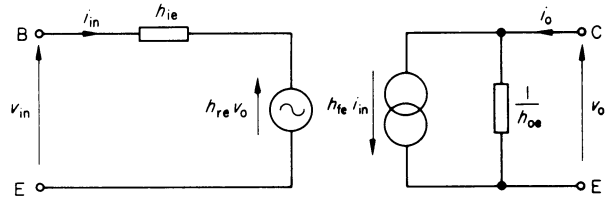


Figure 3.7

Often the voltage generator $h_{re}v_0$ is negligible compared to v_{in} and can be replaced by a short-circuit. Also the current passing through the admittance h_{oe} is small compared with the current generator $h_{fe}i_{in}$, so that the resistor $1/h_{oe}$ can be removed without appreciably affecting any results. The simplified equivalent circuit of figure 3.8 is then obtained.

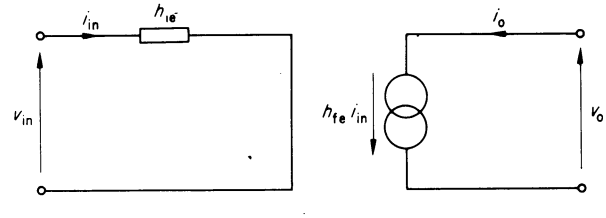


Figure 3.8

3.5 Calculation of common-emitter amplifier voltage gain and input resistance using *h*-parameters

The circuit shown in figure 3.9 is that of a single-stage amplifier. Draw an equivalent circuit in terms of the transistor h-parameters, incorporating only the labelled components (h_{oe} and h_{re} may be neglected). Using this equivalent circuit, if R_1 = 100 kΩ, R_2 = 680 Ω, h_{ie} = 1 kΩ and h_{fe} = 85 determine (a) the a.c. input resistance and (b) the voltage gain.

Explain why the input resistance will not remain constant if V_{CC} changes.

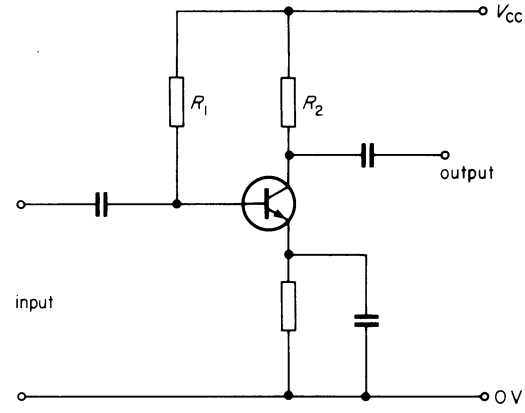


Figure 3.9

(ET4)

Figure 3.10 shows the a.c. equivalent circuit of the amplifier of figure 3.9.

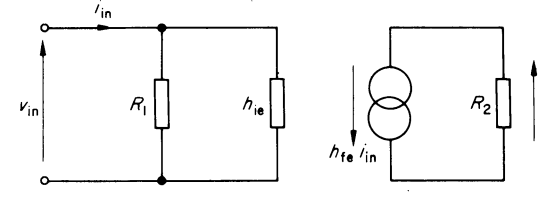


Figure 3.10

(a) Amplifier a.c. input resistance $r_{in} = v_{in}/i_{in}$ therefore

$$r_{in} = \frac{R_1 h_{ie}}{R_1 + h_{ie}} = \frac{100 \times 1}{101} = 0{\cdot}99\ \text{k}\Omega$$

(b) Input voltage $v_{in} = i_{in}r_{in} = 990i_{in}$

Output voltage $v_o = -h_{fe}i_{in}R_2 = 57\,800i_{in}$

Voltage gain $A_v = v_o/v_{in} = -57\,800/990 = -58{\cdot}4$

The minus sign in the answer for A_v indicates the 180° phase shift between input and output voltages.

If V_{CC} changes, the operating point will move to a different V_{CE} curve on the input characteristics. The slope at the new operating point will be different from the original one; hence h_{ie} will change and so will the input resistance of the amplifier.

3.6 Analysis of emitter-follower and common-emitter amplifiers using *h*-parameters

The circuit diagram of an emitter-follower is shown in figure 3.11, together with the h-parameters (table 3.1) of the transistor used.

Draw either (a) the common-emitter or (b) the common-collector equivalent circuit and determine approximately (i) the input resistance and (ii) the output resistance of the stage.

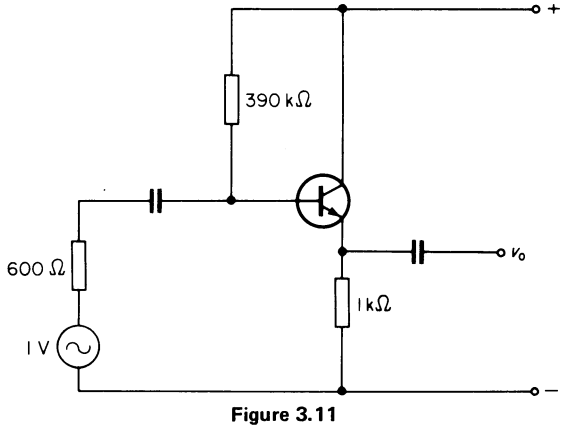


Figure 3.11

Table 3.1

Common emitter	Common collector
$h_{ie} = 600\ \Omega$	$h_{ic} = 600\ \Omega$
$h_{re} = 0$	$h_{rc} = 1$
$h_{fe} = 99$	$h_{fc} = -100$
$h_{oe} = 0$	$h_{oc} = 0$

(ET5)

The equivalent circuit of the common-emitter amplifier is shown in figure 3.12.

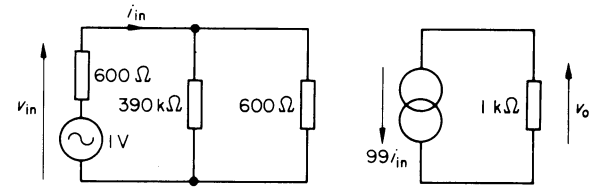


Figure 3.12

Neglecting the 390 kΩ resistor compared with h_{ie}, the input resistance

$$r_{in} = v_{in}/i_{in} = h_{ie} = 600\ \Omega$$

The input resistance viewed from the 1 V source would be 1200 Ω. To determine the output resistance, the source must be replaced by its internal resistance of 600 Ω as shown in figure 3.13.

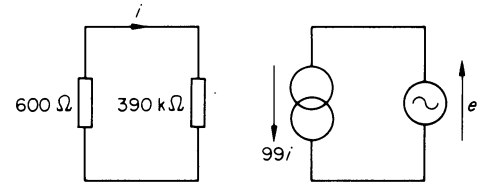


Figure 3.13

In figure 3.13, $i = 0$; therefore, the output resistance $r_o = e/99i = \infty$. That is, the output resistance is effectively infinite.

Figure 3.14 shows the equivalent circuit of the common-collector amplifier. Again, for the approximate input resistance, the 390 kΩ resistor can be neglected.

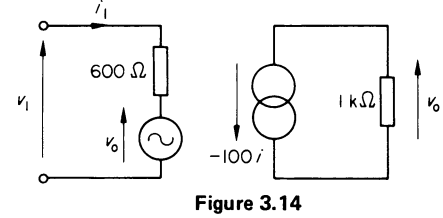


Figure 3.14

From figure 3.14

$$v_1 = v_o + 0{\cdot}6i_1 \qquad (3.10)$$

Also

$$v_o = -(-100i_1) \times 1 = 100i_1$$

Substituting for v_o in equation 3.10

$$v_1 = 100i_1 + 0{\cdot}6i_1$$

therefore input resistance

$$r_{in} = v_{in}/i_{in} = 100{\cdot}6\ \text{k}\Omega$$

To determine the output resistance, the circuit of figure 3.15 is used.

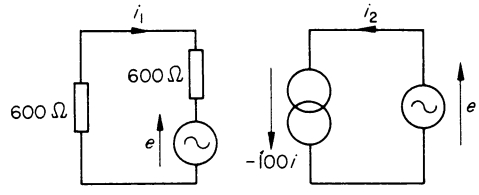


Figure 3.15

From figure 3.15

$$i_1 = -e/1200$$

and

$$i_2 = -100i_1$$

Output resistance

$$r_o = e/i_2 = -1200i_1/-100i_1 = 12\ \Omega$$

3.7 Equivalent *h*-parameter circuit of common-emitter amplifier

The h-parameters of a transistor are h_{ie} = 800 Ω, h_{fe} = 47, h_{oe} = 80 μS and h_{re} = 5 x 10^{-4}. Calculate the output voltage and output resistance of a common-emitter stage using this transistor with a load of 5 kΩ *and fed from a 10* mV *source of 500* Ω *internal resistance.*

(H.N.C.)

The equivalent circuit of the amplifier is shown in figure 3.16.

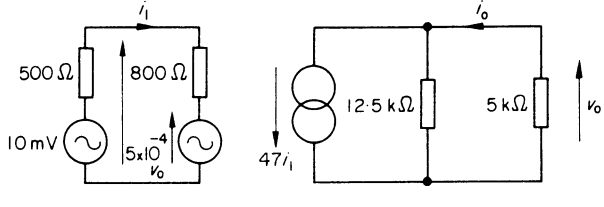


Figure 3.16

Considering the input circuit of figure 3.16

$$0{\cdot}01 = 1300i_1 + 5 \times 10^{-4}v_o \qquad (3.11)$$

The effective load resistance in the output circuit R is

$$R = \frac{12{\cdot}5 \times 5}{17{\cdot}5} = 3{\cdot}57\ \text{k}\Omega$$

therefore output voltage

$$v_o = -47 \times 3{\cdot}57 \times 10^3 i_1 = -167{\cdot}8 \times 10^3 i_1$$

Substituting for i_1 in equation 3.11

$$0{\cdot}01 = \frac{-1300v_o}{167{\cdot}8 \times 10^3} + 5 \times 10^{-4}v_o$$

$$= -77{\cdot}5 \times 10^{-4}v_o + 5 \times 10^{-4}v_o$$

$$v_o = \frac{-0{\cdot}01}{72{\cdot}5 \times 10^{-4}} = -1{\cdot}38\ \text{V}$$

The output resistance is found by replacing the 10 mV source by its internal resistance as shown in figure 3.17.

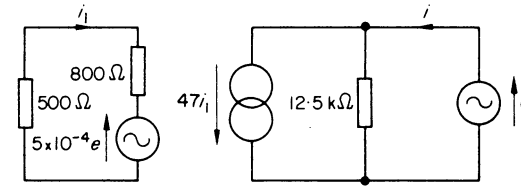


Figure 3.17

Considering figure 3.17

$$5 \times 10^{-4}e = -1{\cdot}3i_1 \qquad (3.12)$$

$$e = (i - 47i_1)12{\cdot}5$$

Substituting for i_1 from equation 3.12

$$e = 12{\cdot}5i + \frac{47 \times 5 \times 10^{-4} \times 12{\cdot}5e}{1{\cdot}3}$$

$$e = 12{\cdot}5i + 0{\cdot}226e$$

Therefore output resistance

$$r_o = e/i = 12{\cdot}5/0{\cdot}774 = 16{\cdot}1\ \text{k}\Omega$$

and the output resistance of the stage R_o is given by

$$R_o = r_o R_L/(r_o + R_L) = 16{\cdot}1 \times 5/21{\cdot}1 = 3{\cdot}8\ \text{k}\Omega$$

3.8 Voltage and current gains of common-emitter amplifier

(a) Explain what is meant by the h-parameters of a transistor.

(b) A common-emitter amplifier uses a transistor having the following h-parameters

$h_{ie} = 1{\cdot}5$ kΩ, $h_{fe} = 90$, $h_{oe} = 20\,\mu$S, $h_{re} = 5 \times 10^{-4}$

The amplifier stage is to have an input impedance of 1·3 kΩ. Find the value of load resistance to be connected in the collector circuit. Under these conditions, calculate the voltage and current gains of the amplifier. Prove any formula used.

(H.N.C.)

(a) The explanation of *h*-parameters has been covered in previous examples.

(b) Figure 3.18 shows the equivalent circuit of the amplifier.

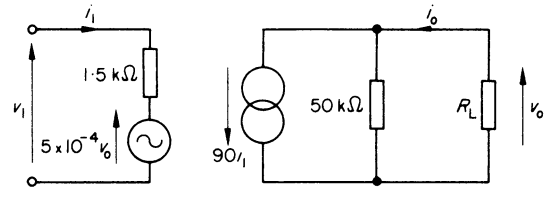


Figure 3.18

From figure 3.18

$$v_1 = 1{\cdot}5i_1 + 5 \times 10^{-4} v_o \qquad (3.13)$$

$$v_o = (i_o - 90i_1)50 \qquad (3.14)$$

Also

$$i_o = -v_o/R_L$$

Substituting for i_o in equation 3.14

$$v_o = -(v_o/R_L + 90i_1)50$$

therefore

$$v_0(R_L + 50)/R_L = -4500i_1 \qquad (3.15)$$

Substituting for v_o in equation 3.13

$$v_1 = 1{\cdot}5i_1 - \frac{2{\cdot}25R_L i_1}{R_L + 50}$$

therefore input resistance

$$r_{in} = v_1/i_1 = 1{\cdot}5 - \frac{2{\cdot}25R_L}{R_L + 50}$$

$$= 1{\cdot}3 \text{ (given)}$$

$$\frac{2{\cdot}25R_L}{(R_L + 50)} = 0{\cdot}2$$

$$R_L = 10/2{\cdot}05 = 4{\cdot}9 \text{ kΩ}$$

Substituting in equation 3.15 for R_L

$$v_o 54{\cdot}9/4{\cdot}9 = -4500i_1$$

$$v_o = -401{\cdot}6i_1 \qquad (3.16)$$

Also as

$$v_1 = 1{\cdot}3i_1$$

Voltage gain

$$A_v = v_o/v_i = -401{\cdot}6i_1/1{\cdot}3i_1 = -308{\cdot}9$$

Also

$$v_o = -i_o R_L$$

substituting in equation 3.16 for v_o

$$-i_o 4{\cdot}9 = -401{\cdot}6i_1$$

therefore current gain

$$A_i = 401{\cdot}6/4{\cdot}9 = 82$$

3.9 Equivalent *h*-parameter circuit of common-base amplifier

A transistor employed in a common-base amplifier has the following h-parameters

$h_{ib} = 42\ \Omega$, $h_{rb} = 4 \times 10^{-4}$, $h_{fb} = -0{\cdot}98$, $h_{ob} = 0{\cdot}4\,\mu$S

Determine the voltage gain, and the input and output resistances of the amplifier if the load resistance is 2 kΩ, and the signal source has an internal resistance of 400 Ω. Comment on the answers.

(H.N.C.)

The equivalent circuit of the amplifier is shown in figure 3.19.

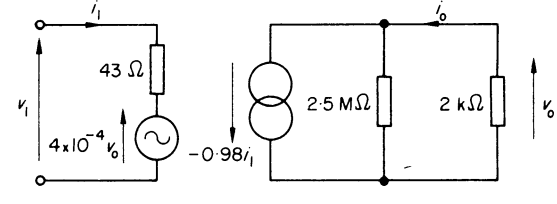


Figure 3.19

As the resistance $1/h_{ob}$ = 2·5 MΩ, it can be neglected compared with the 2 kΩ load resistor. From figure 3.19

$$v_1 = 42i_1 + 4 \times 10^{-4}v_o$$
$$v_o = -(-0{\cdot}98i_1)2000 = 1960i_1 \qquad (3.17)$$

Substituting for i_1 in equation 3.17

$$v_1 = 42v_o/1960 + 4 \times 10^{-4}v_o = 218{\cdot}3 \times 10^{-4}v_o$$

therefore voltage gain

$$A_v = v_o/v_1 = 10^4/218{\cdot}3 = 45{\cdot}8$$

Substituting for v_o in equation 3.17

$$v_1 = 42i_1 + (4 \times 10^{-4} \times 45{\cdot}8)v_1$$

therefore input resistance

$$r_{in} = v_1/i_1 \approx 43\ \Omega$$

The equivalent circuit used to determine the output resistance is shown in figure 3.20.

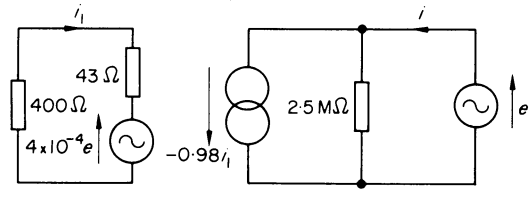


Figure 3.20

From figure 3.20

$$e = [i - (-0{\cdot}98i_1)]\,2{\cdot}5 \times 10^6 \qquad (3.18)$$
$$4 \times 10^{-4}e = -443i_1$$

Substituting for i_1 in equation 3.18

$$e = 2{\cdot}5 \times 10^6 i - 980e/443$$

therefore output resistance

$$r_o = e/i \approx 777\ \text{k}\Omega$$

Thus, although the common-base amplifier has a high voltage-gain, its low input-resistance shunts the load of the previous stage and its high output resistance is shunted by the input resistance of the following stage. Therefore, when used in a multistage amplifier, the effective voltage gain of a common-base stage is seriously reduced.

3.10 Equivalent *h*-parameter circuit of 2-stage common-emitter amplifier

Determine from first principles the overall current and voltage gains of an amplifier which has two similar common-emitter stages, both transistors having the following h-parameters

$$h_{ie} = 2\ \text{k}\Omega,\ h_{fe} = 100,\ h_{oe} = 50\ \mu\text{S},\ h_{re} = 5 \times 10^{-4}$$

The load resistance for both stages is 5 kΩ. *Neglect all other losses at the frequency considered.*

(H.N.C.)

The equivalent circuit of the two stage amplifier is shown in figure 3.21.

This reduces to the circuit shown in figure 3.22, from which

$$v_1 = 2i_1 + 5 \times 10^{-4}v_2 \qquad (3.19)$$
$$v_2 = -(i_2 + 100i_1)4 \qquad (3.20)$$
$$-(i_2 + 100i_1)4 = 5 \times 10^{-4}v_o + 2i_2 \qquad (3.21)$$
$$v_o = -400i_2$$

Substituting for i_2 in equations 3.20 and 3.21

$$v_2 = -\left(\frac{-v_o}{400} + 100i_1\right)4 = 100 \times 10^{-4}v_o - 400i_1 \qquad (3.22)$$

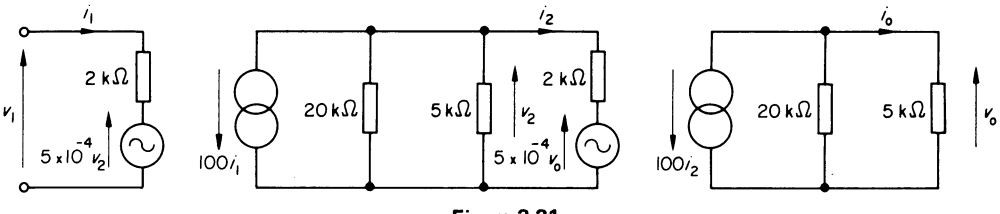


Figure 3.21

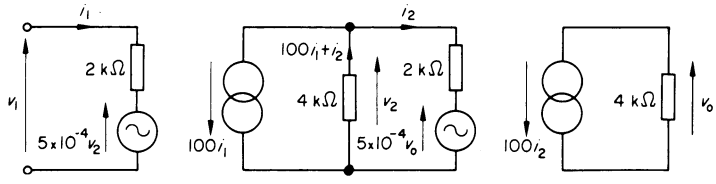


Figure 3.22

Also

$$-\left(\frac{-v_o}{400} + 100i_1\right)4 = 5 \times 10^{-4}v_0 - \frac{2v_o}{400}$$

$$100 \times 10^{-4}v_o - 400i_1 = 5 \times 10^{-4}v_o - 50 \times 10^{-4}v_o$$

$$i_1 = \frac{145 \times 10^{-4}v_o}{400}$$

$$= 3{\cdot}625 \times 10^{-5}v_0 \qquad (3.23)$$

Substituting for i_1 in equation 3.22

$$v_2 = 100 \times 10^{-4}v_o - 145 \times 10^{-4}v_o = -45 \times 10^{-4}v_o \qquad (3.24)$$

Substituting from equations 3.23 and 3.24 into equation 3.19

$$v_1 = 7{\cdot}25 \times 10^{-5}v_o - 225 \times 10^{-8}v_o$$

therefore voltage gain

$$A_v = v_o/v_1 = \frac{1}{7{\cdot}025 \times 10^{-5}} = 14\,235$$

Also from figure 3.21

$$v_o = 5i_o \qquad (3.25)$$

To determine the current gain, divide equation 3.25 by equation 3.23

$$\frac{5i_o}{i_1} = \frac{v_o}{3{\cdot}625 \times 10^{-5}v_o}$$

therefore current gain

$$A_i = i_o/i_1 = 5517$$

3.11 Exercises

Exercise 3.1

Draw a clearly labelled equivalent-T circuit for a transistor in its common-emitter mode. The transistor in a common-emitter amplifier has the following T-parameters, r_e = 40 Ω, r_b = 1 kΩ, r_c = 1.2 MΩ and α = 0·985 and uses a collector load resistance of 5 kΩ. Calculate from first principles the input impedance of the amplifier.
(Answer: 3·1 kΩ) (ET3)

Exercise 3.2

A transistor has the following T-parameters, r_e = 50 Ω, r_b = 1 kΩ, r_c = 1 MΩ, α = 0·98. If it is used in a common-emitter amplifier with a load resistor of 10 kΩ and a signal source resistance of 2685 Ω, determine the current and voltage gains of the amplifier.
(Answers: 32·6, 60·9) (ET3)

Exercise 3.3

If the transistor in Question 3.2 is used in a common-base amplifier with the same signal source resistance and load resistor, determine the current and voltage gains and the input and output resistances of the amplifier.
(Answers: 0·97, 3·6, 70 Ω, 739 kΩ)

Exercise 3.4

Give the circuit diagram of a common-collector transistor amplifier stage together with its equivalent-T circuit. State one important application of this type of amplifier.

The parameters of the equivalent-T circuit of a common-collector transistor amplifier are as follows: r_e = 40 Ω, r_b = 400 Ω, r_c = 1 MΩ, α = 0·97. If the load resistance is 3 kΩ, and the signal source resistance is 1 kΩ, show that the voltage gain is approximately unity, and find the power gain in dB. Also calculate the input and output resistance of the amplifier.
(Answers: 0·99, 14·8 dB, 91·3 kΩ, 82 Ω) (H.N.C.)

Exercise 3.5

(a) Sketch typical input and output characteristics of a transistor connected in either common-base or common-emitter configuration. Using these characteristics, show how the values of h_o and h_r may be estimated and give typical values.

(b) A 500 μF capacitor is charged to 20 V and is then connected as shown in figure 3.23. If the emitter current is adjusted to 0·505 mA before the capacitor is connected, draw an accurate graph of capacitor voltage with respect to time from the instant that the connection is made. The *h*-parameters of the transistor are h_{FB} = 0·99, $h_{ob} = h_{rb}$ = 0.

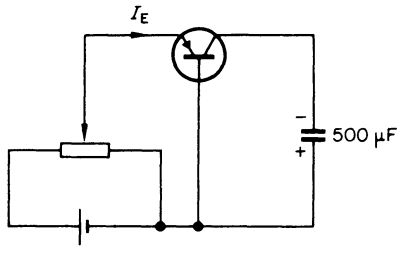


Figure 3.23

(Answers: *Note* at $t = 0$, $V_c = 20$ V; after $t = 0$, $V_c = I_c t/C$, where $I_c = h_{FB} I_E$) (ET4)

Exercise 3.6

The h-parameters for a transistor used in a common-emitter amplifier are $h_{ie} = 1{\cdot}5$ kΩ, $h_{re} = 10^{-4}$, $h_{fe} = 70$, $h_{oe} = 100$ μS. If the load resistor is 1 kΩ and the signal source resistance is 800 Ω, find the current and voltage gains and the input and output resistances of the amplifier.
(Answers: 63·6, −2·77, 1·5 kΩ, 10·3 kΩ)

Exercise 3.7

Calculate the approximate midband voltage gain of the amplifier stage shown in figure 3.24. Determine also its lower 3-dB cut-off frequency. Assume that R_1 is zero for these calculations. The transistor small-signal parameters are $h_{fe} = 50$, $h_{oe} = 10^{-5}$, $h_{ie} = 900$ Ω at the operating point given by $V_{CE} = 10$ V and $I_C = 5$ mA. The reverse gain h_{re} may be neglected.

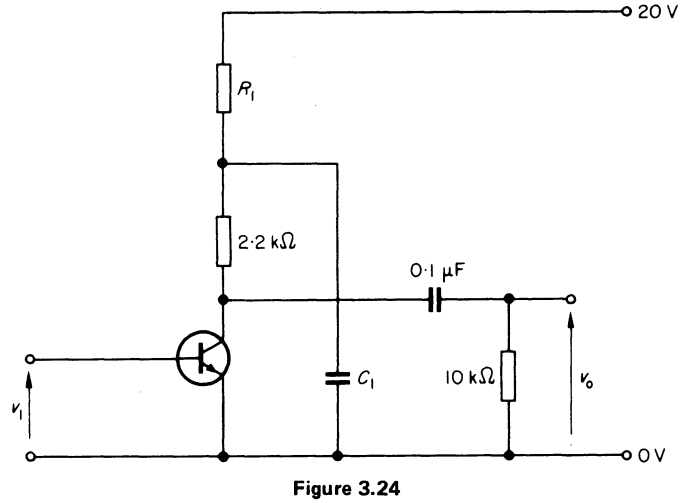


Figure 3.24

Discuss the factors which limit the low-frequency response of an RC-coupled amplifier. Describe how the components R_1 and C_1 can reduce the lower cut-off frequency. Draw a complete circuit for the stage giving suitable values for biasing components, input capacitor and supply voltage. Mention all assumptions made.
(Answers: −98·4, 131 Hz) (I.E.E.)

Exercise 3.8

The basic equations from 4-terminal network theory are

$$v_1 = h_i i_1 + h_r v_2$$

and

$$i_2 = h_f i_1 + h_o v_2$$

Using these equations, derive expressions for the input impedance and output admittance of a transistor amplifier having a load R_L and fed from a source of internal resistance R_S.

A transistor has the following h-parameters $h_{ic} = 1$ kΩ, $h_{fc} = -60$, $h_{rc} = 1$, $h_{oc} = 50$ μS. If an emitter follower using this transistor has $R_L = 600$ Ω and $R_S = 35$ kΩ, calculate the input and output impedances of this circuit. Comment on the results, giving an application of this stage.
(Answers: $r_{in} = h_i - (h_f h_r R_L/1 + h_o R_L)$, 36 kΩ, $Y_o = h_o - (h_f h_r/h_i + R_s)$, 581 Ω)

(H.N.C.)

Exercise 3.9

The common-base hybrid parameters of a transistor are $h_{ib} = 40$ Ω, $h_{ob} = 0{\cdot}4$ μS, $h_{rb} = 5 \times 10^{-4}$, $h_{fb} = -0{\cdot}98$. The transistor is connected in the common-base configuration with a load resistance of 5 kΩ. Calculate the voltage gain and input resistance of the circuit.
(Answers: 116·3, 42·5 Ω) (I.E.R.E.)

Exercise 3.10

The nominal hybrid parameters for a transistor are $h_{fe} = 50$, $h_{re} = 4 \times 10^{-4}$, $h_{oe} = 10^{-5}$ S, $h_{ie} = 800$ Ω. A 2-stage common-emitter amplifier uses this transistor with 2 kΩ collector load resistors. Calculate from the equivalent circuit the overall voltage gain and input resistance. Mention all approximations made in the calculations.
(Answers: 4592, 789 Ω)

Exercise 3.11

An amplifier consists of two transistor stages connected in the common-emitter configuration. The collector resistors of the first and second stages have values of 6 kΩ and 2 kΩ respectively. The transistor hybrid parameters at the operating point are

first stage: h_{ie} = 1 kΩ, h_{fe} = 50, h_{oe} = 20 μS

second stage: h_{ie} = 1·2 kΩ, h_{fe} = 80, h_{oe} = 60 μS

Assuming that the effect of h_{re}, biasing components, and signal source impedance can be neglected, calculate the overall current gain and power gain of the amplifier. Derive any formulae used.
(Answers: 2861, 16·4 x 10^6) (I.E.R.E.)

4 Transistor power amplifiers

4.1 Amplifier classification

With the aid of a transistor input characteristic, explain what is meant by 'class-A', 'class-B' and 'class-C' operation. In each case give a typical application of their use.

In a class-A amplifier, the input voltage causes load current to flow during the whole 360° of the input voltage cycle. This is determined by the d.c. operating point, as shown in figure 4.1a; for class A, the operating point must be on the linear part of the input characteristic such that the a.c. base-emitter voltage cycle produces a complete cycle of base current and hence of collector current.

In a true class-B amplifier, the operating point is such that base current and collector current flow on only one half-cycle of the input voltage, as shown in figure 4.1b. However, in practice the operating point is moved to Q′ on figure 4.1b, so that the nonlinear part of the input characteristic is avoided by the positive half-cycle of base current to keep it free from distortion. Thus collector current flows for more than 180° but less than 360°. This is known as class-AB operation.

In a class-C amplifier, the operating point is such that the base and collector currents flow on only part of one half-cycle of the input voltage (that is for less than 180°) as shown in figure 4.1c.

Class-A amplifiers find their main applications in small power-output devices such as record players where only one transistor is used in the power-output stage.

A single transistor working class B is rarely used in audio applications because of the inherent distortion that is introduced. Instead, two transistors are used in a 'push-pull' configuration, thereby eliminating most of the distortion and increasing the output power (as will be discussed in later questions).

Class-C amplifiers are normally used only at radio frequencies in the output stage for a transmitter or receiver. The load is normally a tuned circuit, thereby producing a sinusoidal output.

4.2 Transformer ratio for power amplifiers

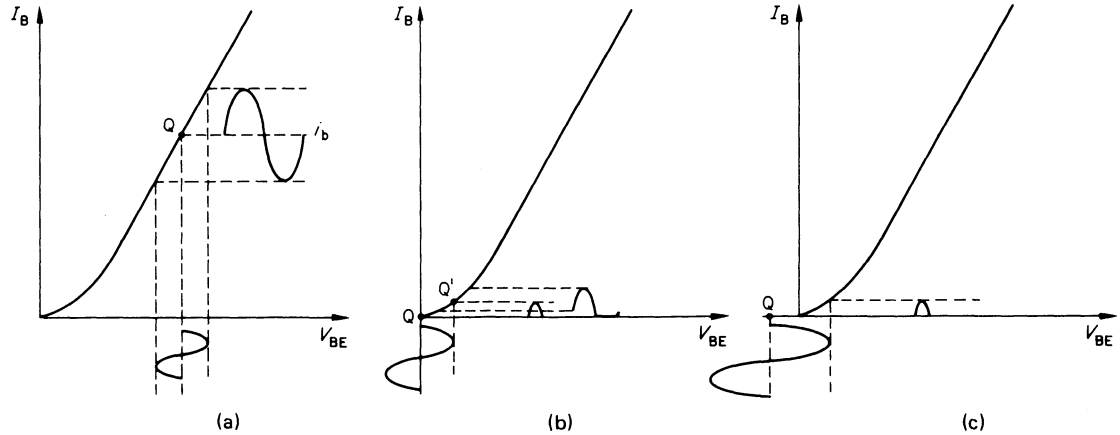
Explain why it is necessary to match a load to a transistor or valve.

Derive an expression for the effective collector load on the transistor in the circuit shown in figure 4.2, assuming an ideal transformer. Calculate a suitable turns ratio for the transformer if the effective collector load is to be 12 Ω and the load resistor R is 4 Ω.

If under the above conditions, the input resistance to the transistor is 5 Ω and an input voltage of 100 mV *r.m.s. produces a voltage across R of 2* V *r.m.s., calculate the power gain in* dB.

How may matching be achieved without the use of a transformer?

The loads used in audio power-amplifiers are usually either loudspeakers or aerial coils having impedances of between 3 and 30 Ω. If these are connected directly in the collector circuit of a class-A



(a) (b) (c)

Figure 4.1

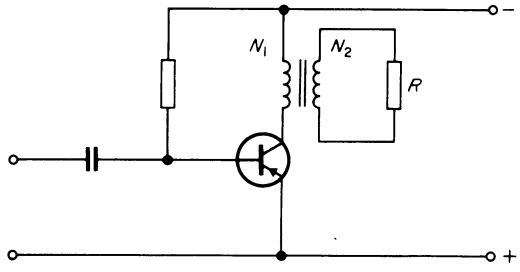


Figure 4.2

(ET4)

amplifier, the output power and power gain are not high enough for most practical applications. To obtain maximum power gain, the load must be matched to the transistor, and this is achieved when the effective load resistance is equal to the output resistance of the amplifier. The commonest method of matching is to use a transformer with a step-down turns-ratio from collector circuit to load as shown in figure 4.3.

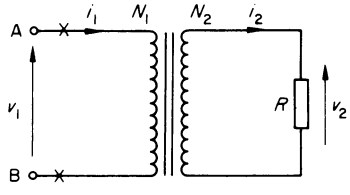


Figure 4.3

The effective resistance in the primary circuit is R_{AB}, where

$$R_{AB} = v_1/i_1 \qquad (4.1)$$

As the transformer is ideal

$$v_1/v_2 = N_1/N_2 \quad \text{and} \quad i_1/i_2 = N_2/N_1$$

Therefore substituting in equation 4.1 for v_1 and i_1

$$R_{AB} = \frac{N_1^2 v_2}{N_2^2 i_2} = \left(\frac{N_1}{N_2}\right)^2 R$$

Substituting values given

$$12 = N_1^2 4/N_2^2$$

therefore turns ratio = $\sqrt{3}$:1 = 1·73:1

Input power = $(0{\cdot}1)^2/5$ = 2 mW

Output power = $(2)^2/4$ = 1 W

therefore power gain

$$A_p = 10 \log (1/0{\cdot}002) = 27 \text{ dB}$$

In voltage amplifiers, an emitter follower can be used for matching a high output impedance to a low input impedance. In some push-pull power amplifiers, where an output transformer is not used, the load is connected into the output circuit in series with a blocking capacitor. (See later examples.)

4.3 Load-line analysis of power amplifier

An npn power transistor having the output characteristics shown in figure 4.4 is coupled to a 3 Ω load resistor through a 2:1 output transformer. The d.c. supply is 12 V and the base bias current is 30 mA. If the sinusoidal input signal has a peak value of 25 mA and the a.c. input resistance to the transistor is 8 Ω, estimate (a) the power dissipated in the load; (b) the power gain in dB; (c) the percentage efficiency. Assume negligible leakage current (I_{CEO}) and that the transformer is ideal.

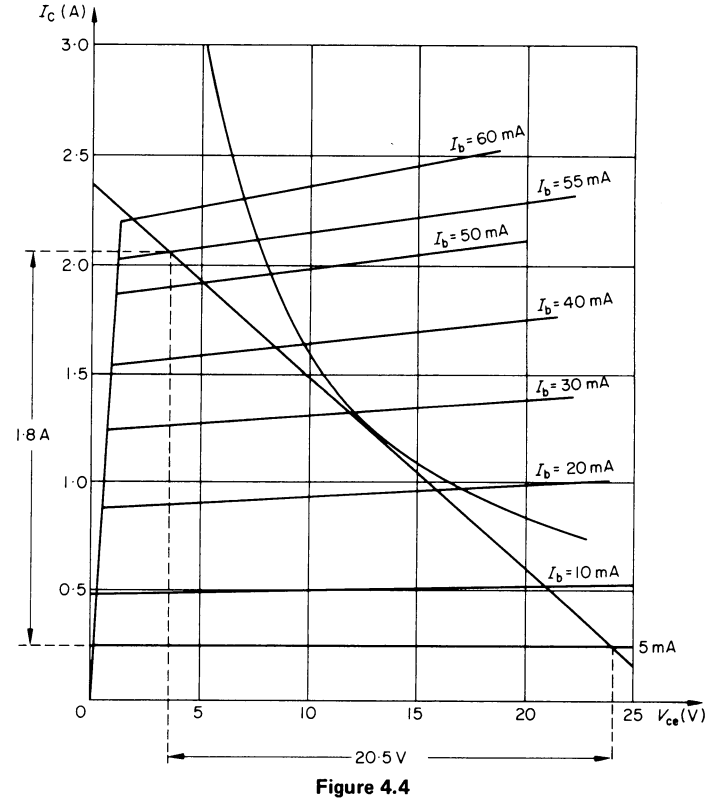


Figure 4.4

Superimpose upon the characteristics the collector dissipation curve for 16 W and thus comment on the suitability of the given d.c. operating point.

(ET4)

(a) Effective a.c. load in the collector circuit is

$R = n^2 R_L = 12\ \Omega$

Therefore the slope of the a.c. load line = $\frac{1}{12}$ siemens. Under no-signal conditions, neglecting the d.c. voltage drop across the transformer primary, the collector voltage will be 12 V. Therefore the quiescent point Q is at the intersection of the V_C = 12 V line and the characteristic for I_B = 30 mA, which gives a quiescent collector current I_Q = 1·325 A.
Therefore d.c. input power

$P_{dc} = V_{CC} I_Q = 12 \times 1{\cdot}325 = 15{\cdot}9$ W

The a.c. load line is now drawn with a slope of $\frac{1}{12}$ siemens (that is for a 1 A change in I_C, there will be a 12 V change in V_C) through the quiescent point Q as shown in figure 4.4. As the input swing of base current is 25 mA peak, the total output current and voltage swings i_o and v_o respectively, can be determined from the intersection of the load line and the characteristics for I_B = 55 mA and I_B = 5 mA, as shown in figure 4.4. (*Note* these two characteristics were not given on the original graph and must be drawn by taking the mean of the 50 and 60 mA characteristics and the mean of the 0 and 10 mA characteristics respectively.)
From figure 4.4

i_o = 1·8 mA peak-to-peak

v_o = 20·5 V peak-to-peak

therefore power dissipated in load = useful output power P_o, that is

$$P_o = v_o(\text{r.m.s.}) i_o(\text{r.m.s.}) = \frac{20{\cdot}5}{2\sqrt{2}} \times \frac{1{\cdot}8}{2\sqrt{2}} = 4{\cdot}61 \text{ W}$$

(b) a.c. input power $P_{in} = i_b^2(\text{r.m.s.}) r_{in} = \left(\frac{0{\cdot}025}{\sqrt{2}}\right)^2 \times 8$

$= 2{\cdot}5$ mW

therefore power gain

$$A_p = 10 \log \frac{P_o}{P_{in}} = 10 \log \frac{4{\cdot}61}{0{\cdot}0025}$$

$= 32{\cdot}66$ dB

(c) Percentage efficiency

$\eta = 100 P_o / P_{dc} = 461/15{\cdot}9$

$= 29$ per cent

The collector dissipation curve for 16 W is now superimposed on figure 4.4 by considering the equation

$V_c I_c = 16$

and constructing a table as shown below.

I_c(A)	0·8	1·0	1·1	1·2	1·3	1·4	1·5	2·0
V_c(V)	20	16	14·5	13·3	12·3	11·4	10·7	8

It can be seen that the load line is nearly tangential to the maximum power dissipation curve near the quiescent point. Thus, the choice of quiescent point is ideal, as the amplifier is now working near its maximum efficiency while still keeping the power dissipated in the transistor below its permissible maximum value of 16 W. Note that the difference between the d.c. input power and the a.c. output power (15·9 − 4·6 = 11·3 W) is dissipated in the transistor itself, mainly at the collector junction, and that this can cause *thermal runaway* unless a *heat sink* is used.

4.4 Efficiency of class-A power amplifier

Give a circuit diagram of a class-A power amplifier using a single transistor, indicating suitable component values. Determine the maximum theoretical efficiency of such a stage and explain why this value is not achieved in practice.

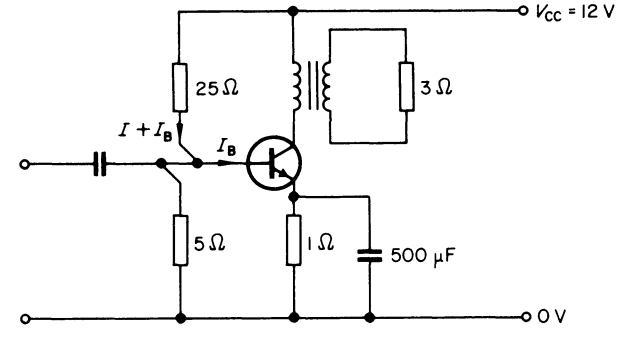


Figure 4.5

Figure 4.5 shows the circuit diagram of a class-A power amplifier. Note that the resistor values are much lower than the corresponding ones used in voltage amplifiers, because the currents flowing

in a power amplifier are much higher than those in the voltage amplifier. For example, for an emitter current of 1 A, 1 V will be dropped across the emitter resistor and the corresponding base current will be of the order of 40 mA; hence the potential-divider resistors used must pass a bleed current I of the order of 400 mA. The decoupling capacitor across the emitter resistor must be of the order of 500 μF if it is required to prevent negative feedback. However, in some amplifiers this capacitor is omitted as it decouples effectively only at frequencies above 1 kHz (in the circuit of figure 4.5), when its reactance will be less than 0·32 Ω.

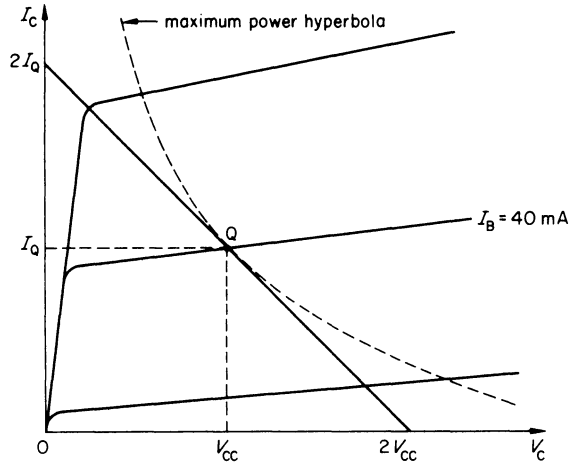


Figure 4.6

Figure 4.6 shows a typical set of characteristics for the amplifier of figure 4.6 with the maximum power dissipation curve of the transistor superimposed. Neglecting the resistance of the primary, the operating point will be at the intersection of the $V_C = V_{CC}$ line with the curve for the quiescent base current (40 mA). For maximum efficiency, the load line should be tangential to the maximum power hyperbola at the Q point, so that the transistor never dissipates more power than the maximum value quoted by the manufacturer. At the same time, the transistor must be driven to the limits of its output power: that is, corresponding to a collector-current swing of $2I_Q$, and a collector-voltage swing of $2V_{CC}$. Therefore output power

$$P_o = \frac{V_{CC}}{\sqrt{2}} \times \frac{I_Q}{\sqrt{2}}$$

$$= \frac{V_{CC}I_Q}{2}$$

d.c. input power

$$P_{in} = V_{CC}I_Q$$

therefore efficiency

$$\eta = P_o/P_{in} = 50 \text{ per cent}$$

In practice the maximum voltage swing of 2 V_{CC} cannot be achieved if distortion is to be avoided, because of the voltage drops across the primary resistance and across the emitter resistor, and also because of the 'knee' voltage of the characteristics. Also the amplitude of the a.f. input signal will vary over a wide range and the practical efficiency depends upon this factor too. Note that the power dissipated in the transistor in a class-A amplifier is maximum under no-signal conditions, for it then has a value $V_{CC}I_Q$ which is twice the maximum available output power, but that this dissipation decreases as the input signal amplitude increases.

4.5 Output power, efficiency and distortion of class-A power amplifiers

The output characteristics of the transistor used in the circuit of figure 4.7 are shown in figure 4.8. On the characteristics plot (a) the 18 W *collector dissipation curve and (b) the optimum a.c. load line.*

If a sinusoidal signal of 25 mA *peak value is applied to the input, estimate the magnitude of the power output and the efficiency of the stage. Determine also the percentage second harmonic distortion of the output current. An ideal transformer may be assumed.*

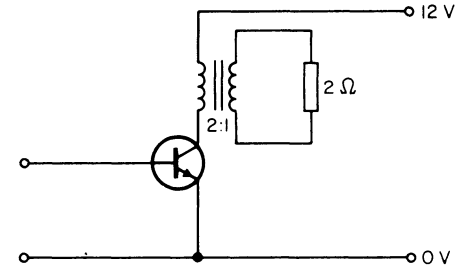


Figure 4.7

The 18 W collector dissipation curve is superimposed on the characteristics as shown in figure 4.8. The effective a.c. input resistance is n^2R = 8 Ω. The optimum a.c. load line must be tangential to the maximum power curve at the operating point of V_C = 12 V; hence

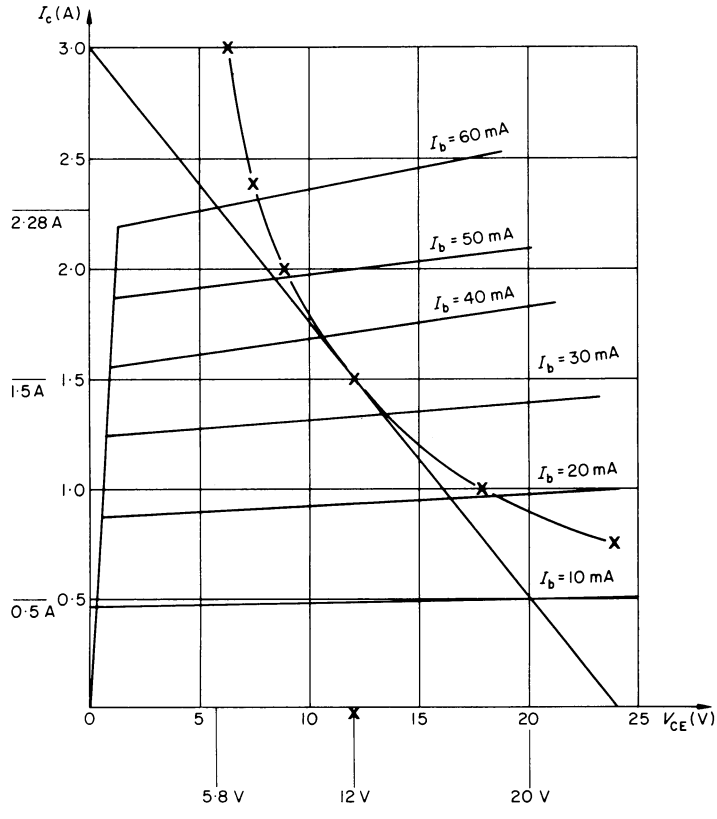


Figure 4.8 (H.N.C.)

this is superimposed on figure 4.8 with a slope of $\frac{1}{8}$ siemens. The corresponding quiescent collector current I_Q is 1·5 A. Therefore d.c. input power

$$P_{in} = 12 \times 1{\cdot}5 = 18 \text{ W}$$

From figure 4.8, the peak-to-peak collector current and voltage swings ΔI_c and ΔV_c respectively, corresponding to a 50 mA swing of input base current are

$$\Delta I_c = 2{\cdot}28 - 0{\cdot}5 = 1{\cdot}78 \text{ A}$$

$$\Delta V_c = 20 - 5{\cdot}8 = 14{\cdot}2 \text{ V}$$

therefore power output

$$P_o = \frac{1{\cdot}78}{2\sqrt{2}} \times \frac{14{\cdot}2}{2\sqrt{2}} = 3{\cdot}2 \text{ W}$$

and efficiency

$$\eta = P_o/P_{in} = \frac{3{\cdot}2 \times 100}{18} = 17{\cdot}8 \text{ per cent}$$

To determine percentage second-harmonic distortion, consider figures 4.9a, 4.9b and 4.9c.

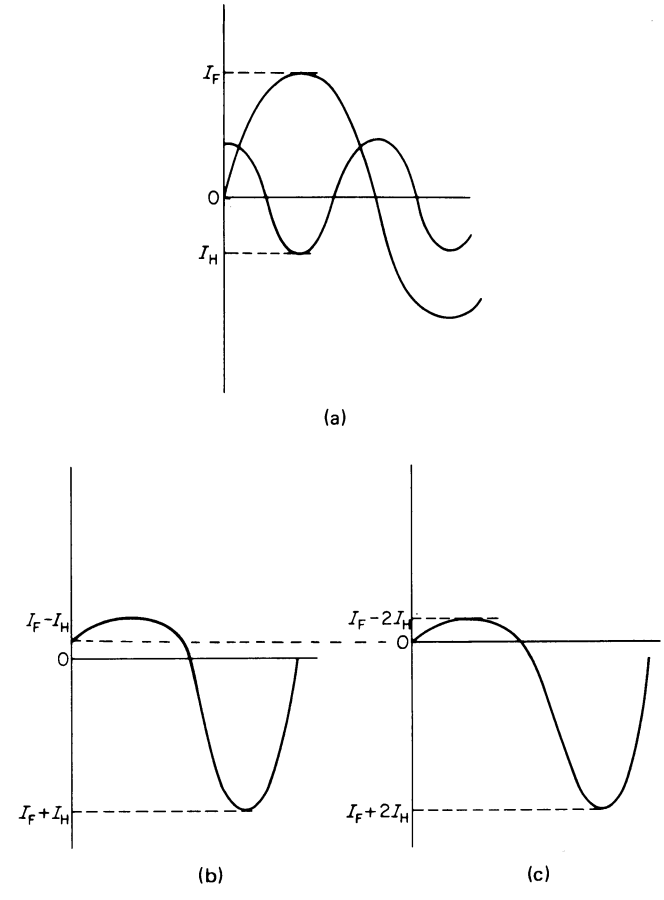


Figure 4.9

Figure 4.9a shows a sketch of a waveform at fundamental frequency together with the waveform at the second harmonic of that frequency. Figure 4.9b shows a sketch of the two added together; note that the periodic times of the positive and negative half-cycles are now unequal. The other component that also appears with second-harmonic distortion is a d.c. component of the same amplitude as the second harmonic. Figure 4.9c shows the resultant output waveform with second-harmonic distortion, from which it can be seen that

positive peak value $= I_F - 2I_H = B$

negative peak value = $I_F + 2I_H = A$

$$I_F = \frac{A + B}{2} \quad \text{and} \quad I_H = \frac{A - B}{4}$$

Thus percentage second-harmonic distortion is

$$D = \frac{I_H}{I_F} \times 100$$

$$D = 50\frac{(A - B)}{A + B} = 50\frac{(1 - 0{\cdot}78)}{1 + 0{\cdot}78} = 6{\cdot}18 \text{ per cent}$$

Note that this method assumes that no other harmonics are present.

4.6 Class-B push-pull amplifier

What are the advantages of operating an amplifier in push-pull? Draw the circuit diagram of a class-B push-pull amplifier indicating how bias is obtained. Explain with the aid of suitable waveform diagrams the operation of the circuit. Why is it necessary to have matched transistors or valves? (ET4)

The advantages of operating an amplifier in push-pull are

(1) Larger power output than a single transistor amplifier.

(2) As the two collector currents flow in opposite directions in the output transformer primary, no magnetic saturation of the core can occur.

(3) Similarly, there will be no net second-harmonic distortion as the second-harmonic components cancel each other out in the primary.

(4) The resultant a.c. current flowing from the centre of the output transformer primary, through the supply line, is zero. Therefore, as no feedback through the supply line to the pre-amplifier stages occurs, distortion is reduced.

(5) Quiescent base and collector currents are low in class-B operation.

Figure 4.10 shows the circuit diagram of a class-B push-pull amplifier. Theoretically, the quiescent base and collector currents should be zero; but the transfer characteristics of the transistors are nonlinear at the lower end thereby giving rise to crossover distortion in the output waveform (as shown in figure 4.12). By suitable choice of R_1 and R_2 however, a small d.c. base current (usually about 5 per cent of the peak collector current) is allowed to flow and this largely eliminates crossover distortion.

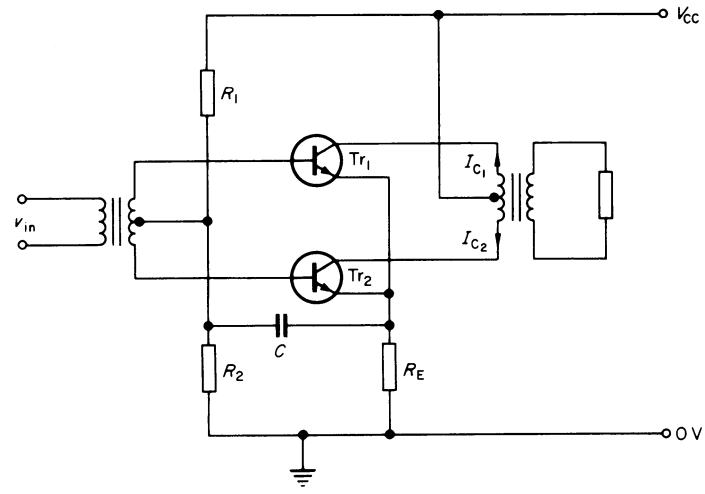


Figure 4.10

The emitter resistor R_E fixes the quiescent emitter voltage and provides a small amount of negative feedback which improves the d.c. stability of the amplifier.

The input transformer is connected in such a way that the signals applied to the transistors are in phase opposition. On the positive half-cycle of input voltage Tr_1 becomes forward biased and its collector current waveform follows the input voltage waveform; Tr_2 conducts only briefly, as the signal voltage soon overcomes the small forward bias and thus cuts off Tr_2.

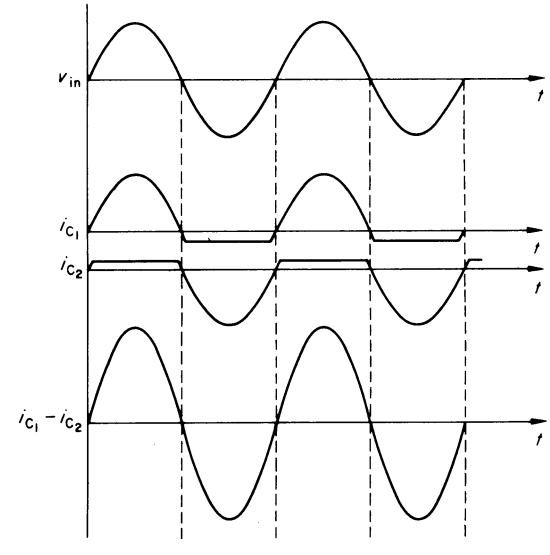


Figure 4.11

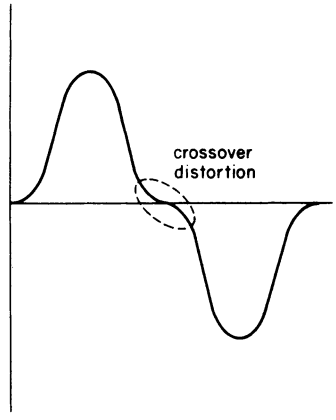


Figure 4.12

The conditions reverse on the negative half-cycle of input voltage, as shown in figure 4.11. The current in the output transformer primary is the difference between the two collector currents, and this produces a sinusoidal waveform as shown.

It is necessary to have matched transistors so that their output currents are identical, thereby giving a perfect sinusoidal output waveform and also providing cancellation of second harmonics in the output, and preventing saturation of the transformer core.

4.7 Efficiency of class-B push-pull amplifier

Compare class-A and class-B operation and hence explain why class-B is commonly used in the output stage of audio frequency push-pull amplifiers. Derive an expression for the theoretical maximum efficiency of such a stage.

A class-B push-pull output stage has two transistors each rated at 5 W. Calculate the maximum power output for a sinusoidal input and an actual efficiency of 75 per cent. Determine also the maximum power output if the efficiency is 50 per cent.

(H.N.C.)

The advantages of class-B push-pull over class-A are

(1) It is possible to achieve much higher power outputs for any given pair of transistors at a given supply voltage.

(2) Negligible power is dissipated in the transistors under no-signal conditions.

(3) Much higher efficiencies are possible in class-B.

The disadvantages are

(1) The harmonic distortion is higher in class-B.

(2) Self-bias cannot be achieved if exact class-B is used.

(3) The supply voltage must have good regulation.

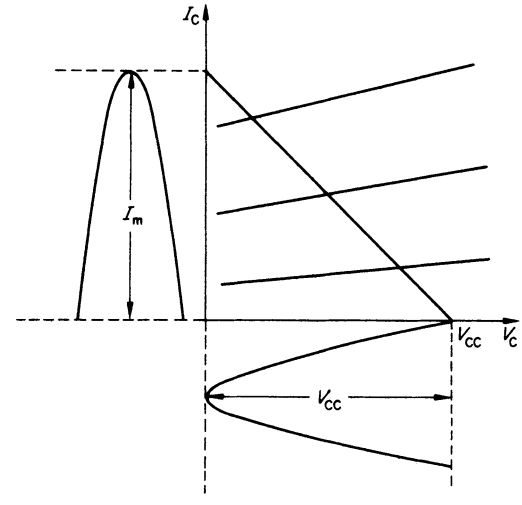


Figure 4.13

Figure 4.13 shows the output characteristics for one transistor in a class-B push-pull amplifier with a load line superimposed on them. If the bias is such that the quiescent collector current is zero and the transistor is subjected to extreme sinusoidal drive conditions, the corresponding collector current and voltage waveforms are shown in figure 4.13. The output current and voltage waveforms of the two transistors connected in push-pull will be assumed to be perfectly sinusoidal.

Therefore power output

$$P_o = \frac{V_{CC}}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}} = \frac{V_{CC} I_m}{2}$$

The corresponding direct collector current in each transistor is the average value of the half sine-wave. As $I_{dc} = I_m/\pi$ for this waveform the d.c. input power from the supply is

$$P_{in} = 2I_m V_{CC}/\pi$$

which is the total for both transistors.

Therefore efficiency

$$\eta = 100P_o/P_{in} = 100\pi/4 = 78{\cdot}5 \text{ per cent}$$

Now the input power P_1 is equal to the output power plus the power dissipated in the transistor.
Therefore

$$P_{in} = P_o + 5$$

when

$$\eta = 0{\cdot}75 = P_o/P_{in} = P_o/(P_o + 5) \qquad (4.2)$$

$$0{\cdot}75P_o + 3{\cdot}75 = P_o$$

$$P_o = 15 \text{ W}$$

In equation 4.2, if

$$\eta = 0{\cdot}5 = P_o/(P_o + 5)$$

$$0{\cdot}5P_o + 2{\cdot}5 = P_o$$

$$P_o = 5 \text{ W}$$

4.8 Transformerless push-pull amplifier

Draw a complete circuit diagram, including a driver stage, of a push-pull amplifier incorporating a complementary pair of transistors as the output stage.

Describe the operation of this circuit. State two advantages of this circuit over one using transformers.

(ET4)

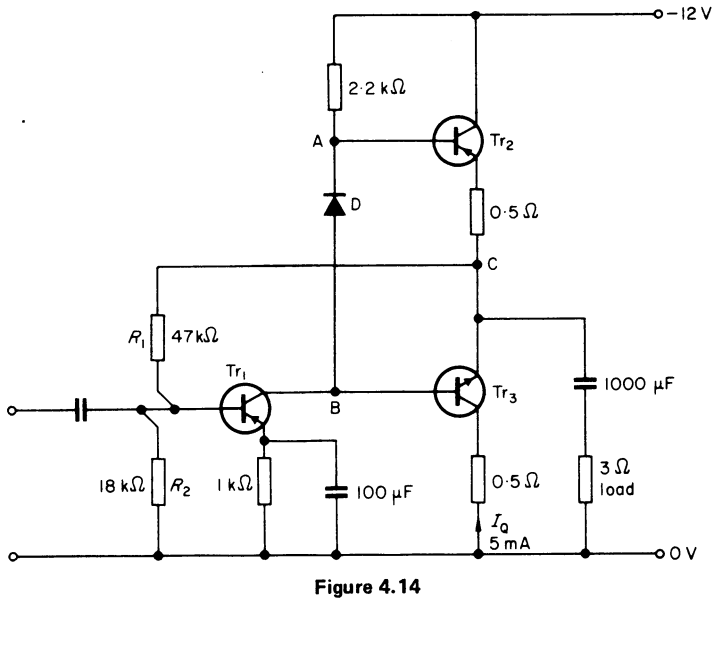


Figure 4.14

Figure 4.14 shows the circuit diagram of a push-pull amplifier using complementary transistors and also its driver stage. Under quiescent conditions, a current of about 5 mA (that is set by suitable choice of R_1 and R_2) will flow through Tr_2 and Tr_3, and this eliminates crossover distortion. Considering quiescent conditions, the voltage at point C will be −6 V, as the complementary transistors should be a matched pair. The voltage at point A will be slightly more negative than that at point C, to ensure that Tr_2 passes 5 mA. Similarly, the voltage at point B will be slightly more positive than that at point C, to ensure that Tr_3 passes the same current.

On the positive half cycle of input voltage, Tr_2 is cut off and Tr_3 is driven hard on and just saturates at the peak of the input signal; hence the output voltage at point C will be approximately 0 V. Similarly, on the negative half cycle of input voltage, Tr_3 cuts off and Tr_2 saturates at the negative peak; and the output voltage rises to a maximum of approximately −12 V. Therefore, the output voltage varies sinusoidally between 0 and 12 V. In practice, however, the undistorted output voltage will be less than this, because of the voltage drops across the transistors and across the emitter resistors, and also because of the 'knee' voltage of the characteristics.

Note that no output transformer is required in this circuit as the load connected to the 0 V line is in series with a 1000 μF capacitor so as not to upset the d.c. conditions. Other points to note are (1) that the diode D while providing the small offset voltage required between the two bases, will also compensate for temperature-related variations of the transistor input characteristic; (2) that as R_1 is connected to the output of the circuit, d.c. and a.c. negative feedback is provided.

One advantage of this circuit is that no input and output transformers are required, thereby saving cost, weight and space. A second advantage is that the output waveform will not suffer the odd-harmonic distortion that transformers introduce.

The disadvantage of the circuit is that matched pairs of complementary transistors with high output power ratings are difficult to obtain. If higher output powers are required, the complementary pair is used in the driver stage and this is then followed by a push-pull output stage using high-power transistors.

4.9 Equivalent thermal circuit of power amplifier

Briefly explain why an RC-coupled common-emitter amplifier stage has more 'built-in' thermal stability than is possible with an output stage using an output transformer. Indicate, by means of a

suitable circuit diagram, the various paths through which the heat is dissipated from the collector junction of a power output transistor to the surrounding air with the aid of a heat sink.

Such an arrangement has the following thermal resistances: through the heat sink $\theta_t = 4{\cdot}7\,^\circ$C/W*; through the mica washer* $\theta_w = 2{\cdot}2\,^\circ$C/W*; from junction to case* $\theta_j = 1{\cdot}6\,^\circ$C/W*; from the case to air direct* $\theta_d = 24\,^\circ$C/W*; from the heat sink to air* $\theta_a = 3\,^\circ$C/W.

If the transistor is required to operate with a maximum junction temperature of 95 °C*, and the maximum temperature of the surrounding air is assumed to be 28* °C*, determine the allowable dissipation of the transistor under these conditions.*

(H.N.C.)

The thermal stability of the *RC*-coupled amplifier is better because of the emitter resistor used and because of the negligible resistance of the transformer primary; for this makes the collector voltage of the transistor much higher and thus increases the power dissipation in the transistor. Heat sinks are normally used to conduct this heat away from the transistor to the air.

It is found experimentally that the steady state temperature rise at the collector junction is proportional to the power dissipated at the junction, that is

$$\Delta T = T_j - T_a \propto P_D$$

therefore

$$T_j - T_a = \theta P_D$$

where T_j and T_a are the collector junction and ambient temperatures respectively (in degrees Celsius), and P_D is the power (in watts) dissipated at the collector junction (neglecting the small amount of power dissipated at the base-emitter junction). The constant of proportionality, θ, is known as the thermal resistance; its value depends upon (i) the size of the transistor; (2) the convection and radiation from the transistor to its surroundings; (3) the conduction from the transistor to its heat sink.

Hence, θ can be considered as the resistance to the removal of heat from the collector junction, and is comparable with ohmic resistance.

The equivalent thermal circuit of the transistor and heat sink is shown in figure 4.15.

From figure 4.15 the total thermal resistance θ is given by

$$\theta = \theta_j + \frac{\theta_d(\theta_w + \theta_t + \theta_a)}{\theta_d + \theta_w + \theta_t + \theta_a}$$

$$= 1{\cdot}6 + 24 \times \frac{9{\cdot}9}{33{\cdot}9}$$

$$= 8{\cdot}6\,^\circ\text{C/W}$$

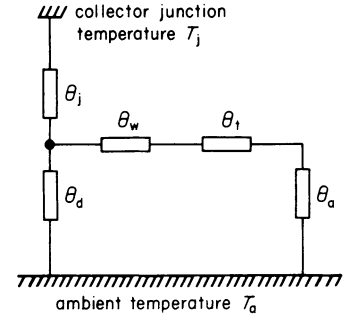


Figure 4.15

Now

$$T_j - T_a = P_D\theta$$

$$95 - 28 = 8{\cdot}6P_D$$

$$P_D = \frac{67}{8{\cdot}6} = 7{\cdot}8\text{ W}$$

4.10 Heat-sink design

A silicon power transistor operates in a class-A mode. In an ambient temperature of 30 °C *the transistor is to have a maximum junction temperature of 100* °C *when its collector power dissipation is 10* W*. Calculate the minimum area of heat sink required when the material used dissipates 1·25* mW/cm^2 *for each degree Celsius above ambient. The junction-to-sink thermal resistance may be taken as 1* °C/W.

What would be the maximum collector power dissipation for an infinite heat sink?

(I.E.R.E.)

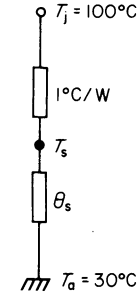


Figure 4.16

Figure 4.16 shows the equivalent thermal circuit for the transistor and its heat sink.

$$T_j - T_a = P\theta$$

where θ = total thermal resistance from junction to air.
Therefore

$$100 - 30 = 10\theta$$

$$\theta = 7\ ^\circ\text{C/W}$$

Therefore, the thermal resistance of the heat sink $\theta_s = 6\ ^\circ\text{C/W}$
Also

$$T_j - T_s = 10 \times 1$$

$$T_s = 90\ ^\circ\text{C/W}$$

Hence, the heat sink is 60 °C above ambient temperature. Let the area of the heat sink be A cm^2; therefore, the power dissipated by the heat sink is

$$P = 1{\cdot}25 \times 10^{-3} \times A \times 60 = 10\ \text{W}$$

and

$$A = 10/75 \times 10^{-3} = 133{\cdot}3\ \text{cm}^2$$

If the sink had infinite thermal capacity, then the case would be at ambient temperature.
That is

$$100 - 30 = P_{max} \times 1$$

$$P_{max} = 70\ \text{W}$$

4.11 Exercises

Exercise 4.1

Explain what is meant by class-A operation of a power amplifier.

A transistor has the input and output characteristics given below.

V_{BE} (mV)	370	450	500	545	597	623
I_B (mA)	7·5	20	30	40	50	60

V_{CE} (V)	2	6	12	for I_B (mA)
I_C (A)	0·67	0·68	0·69	10
	1·53	1·57	1·64	30
	2·32	2·4	2·52	50

This transistor is used in a common-emitter power amplifier with a load resistance of 2 Ω which is connected to the transistor by a 2:1 step-down transformer.

Under no-signal conditions the base current is to be 30 mA and the collector dissipation 15 W. Plot the characteristics; draw the a.c. load line; and, for a sinusoidal input base current of peak value 20 mA, estimate (a) the load power; (b) the efficiency; (c) the collector supply voltage required; (d) the r.m.s. base input voltage; (e) the power gain.
(Answers: 2·68 W, 18 per cent, 9·3 V, 99 mV, 62·8 dB.)

(ET5)

Exercise 4.2

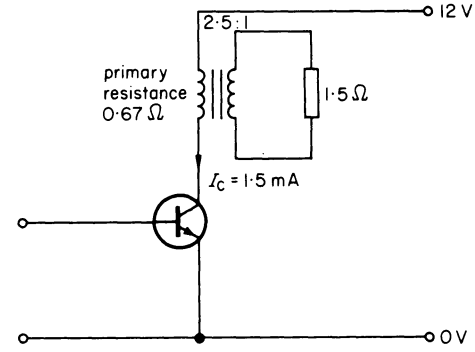


Figure 4.17

The output characteristics of the transistor used in the circuit of figure 4.17 are given below.

V_{CE} (V)	2	10	20	for I_B (mA)
I_C (A)	0·48	0·49	0·5	10
	1·25	1·31	1·38	30
	1·56	1·66	1·79	40
	2·2	2·36	2·56	60

Plot these characteristics and superimpose on them (a) the 18 W collector dissipation curve; (b) the d.c. load line; (c) the a.c. load line for the circuit.

Assuming a sinusoidal input of 25 mA peak value, estimate the power dissipated in the 1·5 Ω resistor, stating any further assumptions made.
(Answer: 3·6 W)

(ET5)

Exercise 4.3

A power amplifier operating in class-A with a load of 5 Ω referred to the primary of the coupling transformer has a quiescent current of 2·7 A. During one half-cycle it is driven to $I_{c(max)}$ = 4·9 mA where it saturates with $V_{CE(sat)}$ = 0·5 V. During the alternate half-cycle $I_{c(min)}$ = 0·1 A. Calculate (a) the output power at the fundamental frequency; (b) the percentage second harmonic distortion; (c) the supply voltage; (d) the maximum instantaneous power dissipation; (e) the maximum permissible thermal resistance between the collector junction and its surroundings if, in the interest of reliability, the junction temperature must not exceed 135°C, the maximum ambient temperature being 35°C.
(Answers: 14·4 W; 4·16 per cent, 11·5 V, 31·25 W, 3·2 °C/W)
(H.N.C.)

Exercise 4.4

A germanium transistor is connected in its common-emitter mode with the load coupled by means of an ideal 3·5:1 step-down transformer. The operating point is determined by a resistor connected between the base and negative supply rail. If the supply voltage is 16 V and the collector dissipation is not to exceed 250 mW, use the table below to find by a graphical method an operating point that delivers maximum undistorted output power to a load resistor of 75 Ω connected across the transformer secondary. Calculate the power output under these conditions and the value of the bias resistor required. The thermal resistance between the transistor case and the air is 200 °C/W. Find the temperature of the case if the ambient temperature is 20°C when the transistor is working under the given load conditions.

V_{CE} (V)	2·5	10	20	30	for I_B (mA)
I_C (mA)	0·5	0·5	0·55	0·65	0
	5·5	6·4	6·9	7·5	0·1
	17	18·5	19·4	20·4	0·3
	29·5	31·7	33·2	34·7	0·5

(Answers: (16 V, 15 mA), 100 mW, 67 kΩ, 48°C) (H.N.C.)

Exercise 4.5

What is meant by the terms class-A and class-B when applied to valve or transistor amplifiers?

Explain with the aid of diagrams the operation of a push–pull amplifier and list the possible reasons for its use. Show how the bias is obtained for (a) class-A operation and (b) class-B operation.
(ET4)

Exercise 4.6

What are the advantages of operating valves or transistors in push–pull? What is meant by class-B push–pull and what are its advantages over class-A push–pull? Why is class-AB often used in practice?

Draw a circuit diagram to show either a valve or transistor push–pull output stage fed via one type of electronic phase-splitting circuit (that is, a push–pull input transformer must not be used). Explain the operation of the phase splitter.
(ET5)

Exercise 4.7

Two transistors, each having a rated dissipation of 500 mW, are used in a class-B push–pull output stage. Calculate the maximum power output if the input is sinusoidal and the actual efficiency is 75 per cent. What would be the maximum power output if the efficiency were 50 per cent?
(Answers: 1.5 W, 1 W)

Exercise 4.8

A silicon transistor can dissipate 6 W and has a maximum junction temperature of 150°C. Determine the maximum temperature of the surrounding air if the thermal resistances are as follows

through the heat sink	4·5°C/W
through the mica washer	2·0°C/W
from junction to case	1·5°C/W
from case to air direct	25°C/W
from heat sink to air	3·5°C/W

(Answer: 98·1° C) (H.N.C.)

Exercise 4.9

To prevent thermal runaway in a power transistor, it is required to limit its junction temperature to 80°C when it is dissipating 10 W at an ambient air temperature of 20°C. Calculate the minimum surface area of the heat sink required if 6 cm^2 of the sink material has a thermal resistance of 100 °C/W and a mica washer is included

in the mounting with a thermal resistance of 1·2 °C/W. Also assume that the transistor has a junction-to-case thermal resistance of 0·8 °C/W.

(Answer: 150 cm^2) (I.E.R.E.)

Exercise 4.10

A silicon transistor can dissipate 8 W and has a maximum junction temperature of 90°C. Find the maximum ambient temperature at which it can be operated in each of the following cases (i) with a mica washer of resistance 3 °C/W on a heat sink of 4 °C/W; (ii) on the same heat sink but without the washer. The resistance from junction to case is 1·5 °C/W and from the case of the transistor to air direct is 28 °C/W.

At what ambient temperature could the transistor operate on a heat sink of infinite thermal capacity assuming no washer is used.
(Answers: 33·2°C, 50°C, 78°C)

Exercise 4.11

Derive an expression for the thermal resistance from junction to air as a function of the collector power dissipated, the junction temperature, and the ambient temperature. It may be assumed that the rate of removal of heat from a collector junction is proportional to the difference between the junction and ambient temperatures.

A silicon power transistor with a maximum junction temperature of 120°C dissipates 20 W when the ambient temperature is 40°C. Calculate the area of the heat sink that would be required, with and without the mica washer, when using (i) a matt black surface with a thermal resistivity of 50 °CW/in^2; (ii) a polished surface with a thermal resistivity of 75 °CW/in^2. Assume that the thermal resistance from junction to transistor case is 1·8°C/W, from case through a mica washer to sink is 1·5 °C/W, and from case to air is 25 °C/W.
(Answers: 54·8 in^2, 82·2 in^2) (I.E.R.E.)

5 Tuned circuits and high-frequency transistor amplifiers

5.1 Relationship between Q-factor and bandwidth

Define the Q-factor of a tuned coil and deduce the relationship between Q and the bandwidth about the frequency of resonance.

A tuned coil of inductance 1 mH *in the collector of a high frequency amplifier resonates at 500* kHz *with a bandwidth of 50* kHz. *What is its dynamic resistance at resonance?*

(H.N.C.)

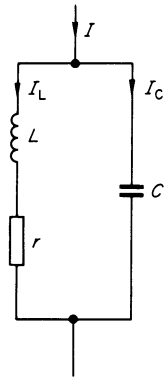


Figure 5.1a

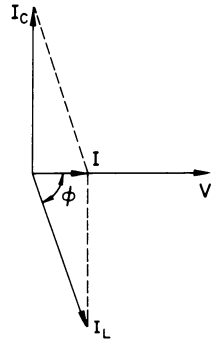


Figure 5.1b

Figure 5.1a shows the circuit diagram of a tuned coil and figure 5.1b shows the corresponding phasor diagram for the resonant condition. The Q-factor is defined at resonance as

$$Q = \frac{\text{current through the capacitor at resonance}}{\text{total circuit current}}$$

$$= I_C/I = \frac{I_L \sin\phi}{I_L \cos\phi} = \tan\phi = X_L/r$$

then

$$Q = \frac{\omega_0 L}{r}$$

In general, at any frequency f, the Q-factor of a coil is defined as $Q = \omega L/r$ where $\omega = 2\pi f$.

Considering figure 5.1a, the circuit impedance is

$$Z = \frac{(r + j\omega L/j\omega C)}{r + j\omega L + 1/j\omega C} \tag{5.1}$$

In general, $r \ll \omega L$; therefore equation 5.1 becomes

$$Z = \frac{L/C}{r + j(\omega L - 1/\omega C)} \tag{5.2}$$

The maximum circuit current occurs at resonance, which will be when Z is a minimum.

Therefore, from equation 5.2, resonant frequency f_0 is given by

$$\omega_0 L = \frac{1}{\omega_0 C}$$

or

$$f_0 = \frac{1}{2\pi\sqrt{(LC)}}$$

Similarly, the circuit impedance at this frequency is $Z = L/Cr$. Note that this is purely resistive, is referred to as the dynamic resistance R_D, and is usually of very high value.

From equation 5.2

$$Z = \frac{L/Cr}{(1 + j\omega L/r)(1 - 1/\omega^2 LC)}$$

$$= \frac{R_D}{1 + jQ(1 - \omega_0^2/\omega^2)} \tag{5.3}$$

The variation in circuit impedance Z with frequency is shown in figure 5.2. When this circuit is used as the collector load in a transistor amplifier, the output voltage is given by

$$v_o = i_c Z = g_m v_{in} Z$$

where g_m is the mutual conductance of the transistor.

Then voltage gain

$$A_v = v_o/v_{in} = g_m Z$$

The frequency response curve of the amplifier will therefore have a similar shape to the impedance response curve. The bandwidth of the circuit is defined as the range of frequencies between which the circuit impedance falls to $R_D/\sqrt{2}$. Alternatively, when the circuit is used as an amplifier, the bandwidth is defined as the range of frequencies between which the voltage gain falls to $1/\sqrt{2}$ of its value at the resonant frequency. Therefore, bandwidth is defined when

$$|Z| = \frac{R_D}{\sqrt{2}} \quad \text{or} \quad Z = \frac{R_D}{1 + j1} \tag{5.4}$$

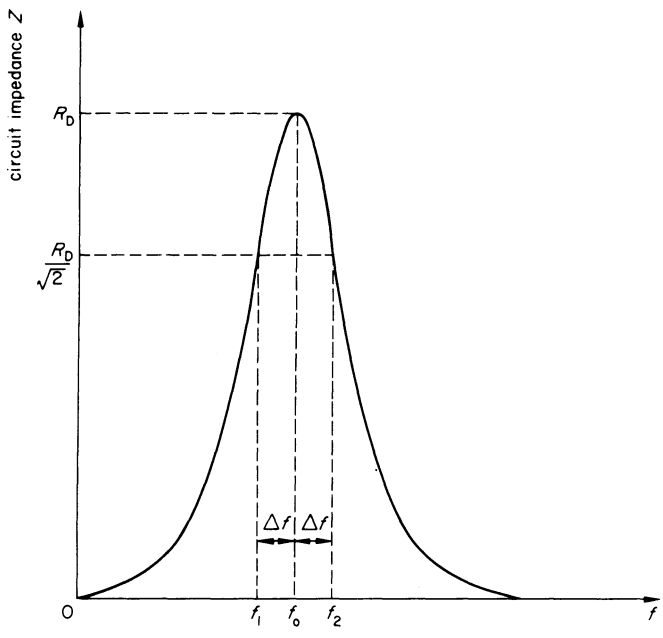


Figure 5.2

Comparing equations 5.3 and 5.4 to determine an expression for bandwidth

$$Q\left(1-\frac{\omega_0^2}{\omega^2}\right)=\pm 1$$

$$Q=\frac{\pm\omega^2}{\omega^2-\omega_0^2}=\frac{\pm\omega^2}{(\omega-\omega_0)(\omega+\omega_0)}$$

$$=\frac{+f^2}{(f-f_0)(f+f_0)} \qquad (5.5)$$

As the bandwidth of a tuned circuit $2\Delta f$ is small compared with the resonant frequency f_0 then

$$f\approx f_0 \quad f-f_0\approx\Delta f \quad \text{and} \quad f+f_0\approx 2f_0$$

In equation 5.5

$$Q=\frac{f_0^2}{\Delta f \times 2f_0}=\frac{f_0}{2\Delta f}$$

$$Q=\frac{\text{resonant frequency}}{\text{bandwidth}}$$

For the values given in the question

$Q = 500/50 = 10$

Now

$$R_D=\frac{L}{Cr}=\frac{\omega_0 L}{\omega_0 Cr}=\frac{Q}{\omega_0 C}=Q\omega_0 L$$

$$=10\times 2\pi\times 500\times 10^3\times 10^{-3}=31{\cdot}4\ \text{k}\Omega$$

5.2 Tuned-collector amplifier

(a) If the voltage gain at the extremes of the bandwidth of an amplifier is 3 dB *down on the maximum gain show that these two frequencies are the 'half-power points'.*

(b) The load of a tuned collector amplifier consists of a capacitor of 2μ F *in parallel with a coil of inductance of 10* mH *and a Q-factor of 14·15 at the resonant frequency. The amplifier has an a.c. input resistance of 700 Ω and a current gain of 152. Assuming that the shunting effect of the transistor is negligible, calculate (i) the frequency at which the amplifier voltage gain is a maximum; (ii) the voltage gain at this frequency; (iii) the amplifier bandwidth. State the effect on the bandwidth if the tuned circuit is shunted by the a.c. input resistance of a second transistor stage.*

(ET4)

(a) In section 2.12, it was proved that at the extremes of the bandwidth the voltage gain was 3 dB down on the maximum voltage gain; that is, assuming the same input voltage

$$v_o/v_{o(\max)}=1/\sqrt{2}$$

Now output power is proportional to v_o^2, that is $P_o = Kv_o^2$ therefore

$$\frac{P_o}{P_{o(\max)}}=\frac{Kv_o^2}{Kv_{o(\max)}^2}=\frac{1}{2}$$

Hence, the frequencies at the extremes of the bandwidth are often referred to as the half-power points.

(b) (i) Resonant frequency $f_0=\dfrac{1}{2\pi\sqrt{(LC)}}$

$$=\frac{1}{2\pi\sqrt{(10^{-2}\times 2\times 10^{-6})}}$$

$$=1{\cdot}125\ \text{kHz}$$

(ii) Input voltage $v_{in} = i_{in}r_{in} = 700i_{in}$

Output voltage $v_o = i_oR_D = A_i i_{in}R_D$

Now

$$R_D = Q\omega_0 L = 14{\cdot}15 \times 2\pi \times 1{\cdot}125 \times 10^{-2} = 1\ \text{k}\Omega$$

then

$$v_o = 152 \times 10^3 i_{in}$$

Voltage gain

$$A_v = v_o/v_{in} = \frac{152 \times 10^3 i_{in}}{700 i_{in}} = 217$$

(iii) Bandwidth $= f_0/Q = \dfrac{1{\cdot}125 \times 10^3}{14{\cdot}15} = 79{\cdot}5$ Hz

If the load were shunted by the input resistance of another stage, the effective load would decrease and the bandwidth would increase.

5.3 Skin effect and dynamic impedance

(a) Explain what is meant by (i) 'skin' effect in a conductor, and (ii) Q-factor of a coil.

(b) Describe and explain one method by which skin effect can be reduced at high frequencies.

(c) A coil is connected in parallel with a capacitor that is adjusted to give resonance at 1 MHz, *the Q-factor being 80. If the impedance at resonance is R_D ohms, what are the upper and lower frequencies between which the impedance of the circuit will be greater than $R_D/\sqrt{2}$ ohms?*

(ET4)

(a) (i) A wire carrying an electric current produces a magnetic field that exists both inside and outside the wire and is strongest at the centre of the wire. If the current is a.c., then an e.m.f. of self-induction is set up which opposes the flow of the current and which again is greatest at the centre of the wire. Therefore, the actual impedance of the wire increases progressively towards its centre; hence, the current tends to flow in the outer skin of the wire. This is known as the *skin effect*. It is negligible at low frequencies but can be considerable at radio frequencies, especially in a coil.

(ii) The Q-factor of a coil was defined in section 5.1.

(b) One common method of reducing skin effect is to use stranded cable, thereby effectively reducing the diameter of each current-carrying conductor. Other methods include the use of hollow conductors, and the use of conductors plated with silver (or some other metal that has a very low resistivity) in order to reduce the resistance of the outer layer.

(c) Bandwidth $= f_0/Q = 10^6/80 = 12{\cdot}5$ kHz

Lower frequency is $(1000 - 6{\cdot}25) = 993{\cdot}75$ kHz

Upper frequency is $(1000 + 6{\cdot}25) = 1006{\cdot}25$ kHz

5.4 Parallel tuned circuit as amplifier load impedance

A coil of inductance 100 μH *has a Q-factor of 60 at a frequency of 1* MHz. *Calculate the required value of shunting capacitor to cause resonance at this frequency and determine the dynamic impedance of this resonant circuit.*

The circuit is to be used as the load of an amplifying device which has an internal resistance of 60 kΩ. *Calculate the amplifier bandwidth.*

(ET4)

Resonant frequency

$$f_0 = \frac{1}{2\pi\sqrt{(LC)}}$$

therefore

$$C = \frac{1}{4\pi^2 \times 10^{-4} \times 10^{12}} = 253\ \text{pF}$$

Dynamic impedance

$$R_D = Q\omega_0 L = 60 \times 2\pi \times 10^6 \times 10^{-4} = 37{\cdot}7\ \text{k}\Omega$$

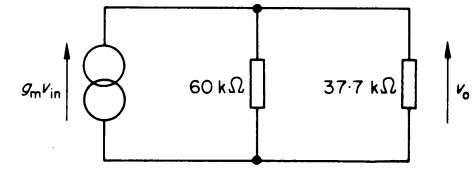


Figure 5.3

Figure 5.3 shows the equivalent circuit of the amplifier, which now has an effective load

$$R = \frac{60 \times 37{\cdot}7}{97{\cdot}7} = 23{\cdot}2\ \text{k}\Omega$$

therefore the effective Q-factor

$$Q_e = \frac{R}{\omega_0 L}$$

$$= \frac{23{\cdot}2 \times 10^3}{2\pi \times 10^6 \times 10^{-4}}$$

$$= 36{\cdot}9$$

and the amplifier bandwidth = $f_0/Q = 10^6/36{\cdot}9 = 27{\cdot}1$ kHz.

5.5 Radio-frequency amplifier

A radio-frequency amplifier uses a transistor having r_{ce} = 500 kΩ *and g_m = 50* mS. *Connected in its collector circuit is a 20*μH *coil of Q-factor 50, and this is tuned to parallel resonance at 1592* kHz. *The output voltage is fed to a second stage of z_{in} = 500* kΩ, *through a coupling capacitor of negligible reactance. Determine (a) the gain of the stage at resonance; (b) the bandwidth; (c) the reduction in gain in* dB *at a frequency 10* kHz *above resonance. Prove any formulae used.*

(H.N.C.)

It has already been shown in section 5.1 that the impedance of a parallel-tuned circuit, when $\omega L \gg r$, is given by

$$Z = \frac{R_D}{1 + j(\omega L/r - 1/\omega Cr)} \qquad (5.6)$$

Let δ = a fractional amount of detuning away from resonance, then

$$\delta = \frac{\omega - \omega_0}{\omega_0}$$

or

$$\omega = \omega_0(1 + \delta)$$

In equation 5.6

$$\frac{Z}{R_D} = \frac{1}{1 + j(\omega_0(1+\delta)L/r - 1/\omega_0(1+\delta)Cr)}$$

$$= \frac{1}{1 + jQ(1 + \delta - 1/(1+\delta))}$$

$$= \frac{1+\delta}{1 + \delta + jQ\delta(2+\delta)}$$

If $\delta \ll 1$

$$\frac{Z}{R_D} = \frac{1}{1 + j2Q\delta}$$

then

$$\left|\frac{Z}{R_D}\right| = \frac{1}{\sqrt{(1 + 4Q^2\delta^2)}} \qquad (5.7)$$

At any frequency the voltage gain $A_v = g_m Z$; then if A_{vo} is the voltage gain at resonance, from equation 5.7

$$\left|\frac{A_v}{A_{vo}}\right| = \left|\frac{g_m Z}{g_m R_D}\right| = \frac{1}{\sqrt{(1 + 4Q^2\delta^2)}}$$

$$A_v = \frac{A_{vo}}{\sqrt{(1 + 4Q^2\delta^2)}} \qquad (5.8)$$

Dynamic impedance $R_D = Q\omega_0 L$

$$= 50 \times 2\pi \times 1592 \times 10^3 \times 20 \times 10^{-6}$$

$$= 10 \text{ k}\Omega$$

The dynamic impedance is shunted by r_{ce} of the transistor, so that the effective load R is given by

$$10 \times 500/510 = 9{\cdot}8 \text{ k}\Omega$$

from which the voltage gain at resonance ($A_{vo} = g_m R$) is calculated as $50 \times 9{\cdot}8 = 490$.

Effective Q-factor

$$Q_e = R/\omega_0 L$$

$$= \frac{9{\cdot}8}{2\pi \times 1592 \times 20 \times 10^{-6}} = 49$$

therefore

$$\text{Bandwidth} = f_0/Q_e = 1592/49 = 32{\cdot}5 \text{ kHz}$$

Fractional detuning

$$\delta = 10/1592 = 6{\cdot}28 \times 10^{-3}$$

In equation 5.8

$$A_v = \frac{490}{[1 + 4 \times 49^2(6{\cdot}28 \times 10^{-3})^2]^{1/2}} = 417$$

therefore change in dB = $-20 \log (490/417) = -1{\cdot}4$ dB

5.6 Q-factor of series tuned circuit

(a) In an experiment, series resonance is obtained at various frequencies between a coil of unknown inductance and a variable capacitor, the results being given below. The circuit is known to possess stray capacitance which is assumed to be of constant value in parallel with the variable capacitor. By plotting a suitable graph, or otherwise, deduce the values of the coil inductance and stray capacitance.

Resonant frequency (kHz)	100	150	200	250	300
Capacitor setting (pF)	940	385	190	100	51

(b) Measurements of Q-factor of the tuned circuit at the various frequencies show that the Q-factor first rises with frequency, then reaches a maximum value, and finally falls as frequency continues to rise. Explain why this occurs.

(TT5)

(a)

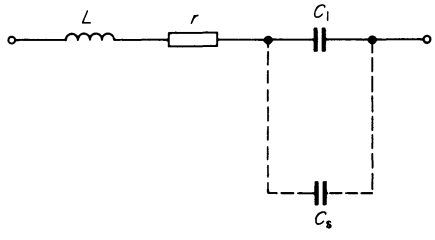


Figure 5.4

Figure 5.4 shows the series tuned circuit. Series resonance occurs when the capacitive reactance is equal to the inductive reactance; that is when

$$1/\omega_0 C = \omega_0 L$$

The resonant frequency f_0 is then given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{5.9}$$

where C includes the stray capacitance (that is $C = C_1 + C_s$).

Therefore using these results in equation 5.9 at 100 kHz and at 200 kHz

$$10^5 = \frac{1}{2\pi[L(940 + C_s)]^{1/2}} \tag{5.10}$$

$$2 \times 10^5 = \frac{1}{2\pi[L(190 + C_s)]^{1/2}} \tag{5.11}$$

Dividing equation 5.11 by equation 5.10

$$2 = \frac{(940 + C_s)^{1/2}}{(190 + C_s)^{1/2}}$$

Squaring both sides

$$760 + 4C_s = 940 + C_s$$

therefore

$$C_s = 180/3 = 60 \text{ pF}$$

Substituting for C_s in equation 5.10

$$10^5 = \frac{1}{2\pi(L \times 10^{-9})^{1/2}}$$

$$L = 1/40\pi^2 = 2{\cdot}53 \text{ mH}$$

(b) At series resonance the circuit impedance is a minimum and is equal to the resistance of the coil; therefore, the circuit current is a maximum, and so are the voltages across the inductance and capacitance. The Q-factor of the series tuned circuit is defined as the ratio of the voltage across the inductance or capacitor to the supply voltage. Therefore, as the frequency increases from zero, the circuit impedance is capacitive and decreases to a minimum at f_0. As the frequency is further increased, the impedance becomes inductive and increases again. Hence, the circuit current, the voltage across the inductance, and the Q-factor all rise to a maximum value at f_0 and then fall again as frequency is further increased.

5.7 Hybrid-π equivalent circuit

Figure 5.5 shows the high-frequency equivalent circuit of a transistor used in a common-emitter resistance-capacitance-coupled stage. Discuss briefly the physical significance of each component shown in the equivalent circuit.

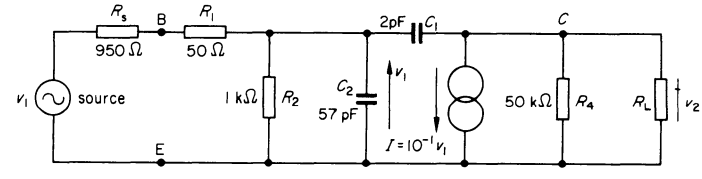


Figure 5.5

(a) If a collector load resistance of 500 Ω is used, show that the circuit can be simplified to eliminate the coupling between collector and base. Calculate the modified value of C_2.

(b) Calculate the frequency at which the gain is 3 dB down relative to the low-frequency value.

(c) Describe two methods of improving the high-frequency response of this amplifier.

(I.E.R.E.)

In figure 5.5

$R_1 = r_{bb'}$ = the base spreading resistance, that is the resistance of the lightly doped base region and leads between the intrinsic base and the terminal

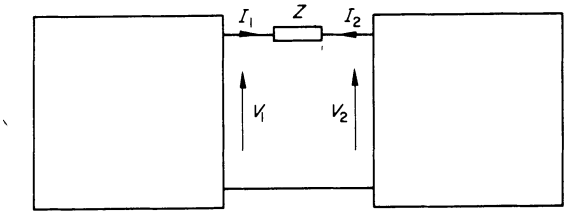
$R_2 = r_{b'e}$ = the resistance to account for the base-emitter junction

$C_2 = C_{b'e}$ = the capacitance of the emitter-base junction, which takes into account depletion layer and transit time (diffusion) capacitances

$C_1 = C_{b'c}$ = the capacitance of the reversed-biased base-collector junction

$10^{-1} V_1 = g_m v_{b'e}$ = the current generator required to represent transistor action by delivering $h_{fe} i_b$ into a short-circuit output

$R_4 = r_{ce}$ = the collector-emitter resistance contributing to the output impedance



(a)

Figure 5.6a

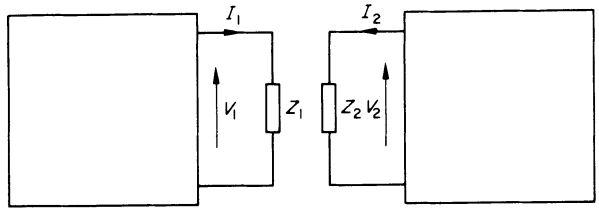


Figure 5.6b

Miller's theorem states that the circuit of figure 5.6a can be replaced by that of figure 5.6b by the following analysis. Let $V_2/V_1 = K$, in figures 5.6a and 5.6b

$$I_1 = \frac{V_1 - V_2}{Z} = \frac{V_1}{Z_1}$$

therefore

$$Z_1 = \frac{ZV_1}{V_1 - V_2} = \frac{Z}{1 - K}$$

also

$$I_2 = \frac{V_2 - V_1}{Z} = \frac{V_2}{Z_2}$$

$$Z_2 = \frac{ZV_2}{V_2 - V_1} = \frac{KZ}{K - 1}$$

Hence, as replacing Z by Z_1 and Z_2 does not change the circuit current and voltage conditions, the two circuits are equivalent.

For the hybrid-π circuit terminated with a resistance R_L, R_4 can normally be neglected, as $R_4 \gg R_L$ therefore

$$K = V_2/V_1 = \frac{-g_m v_{b'e} R_L}{v_{b'e}} = -g_m R_L$$

The modified value of C_2 now becomes

$$C_{in} = C_2 + C_1(1 + g_m R_L)$$

that is two capacitors in parallel.

Therefore

$$C_{in} = 57 + 2(1 + 10^{-1} \times 500) = 159 \text{ pF}$$

Note that in the output circuit

$$C_0 = \frac{-g_m R_L C_1}{-g_m R_L - 1} \approx C_1$$

This would be in parallel with R_L but as it is so small it is usually neglected.

(b)

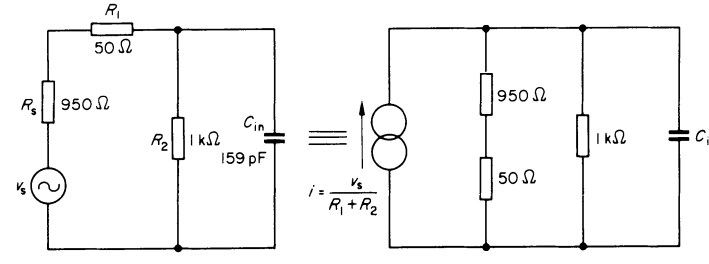


Figure 5.7

Figure 5.7 shows the input circuit together with its constant-current generator equivalent circuit. At low frequencies C_{in} is negligible and the voltage gain A_{vo} is proportional to the resistance network.

Therefore

$$A_{vo} = 500 K_1 \qquad (5.12)$$

At high frequencies the voltage gain becomes

$$A_v = K_1 \times 500X_c/(500^2 + X_c^2)^{1/2}$$

$$= \frac{K_1 \times 500}{(1 + 500^2/X_c^2)^{1/2}} \qquad (5.13)$$

When the voltage gain is 3 dB down

$$A_v = A_{vo}/\sqrt{2}$$

Therefore from equations 5.12 and 5.13 this occurs when

$$500^2/X_c^2 = 1$$

that is, when

$$1/(2\pi fC) = 500$$

which is at frequency

$$f = \frac{10^{12}}{2\pi \times 159 \times 500} = 2 \text{ MHz}$$

(c) One method of improving the high-frequency response is to use inductance in series with the collector load resistor, thereby increasing the effective collector load at high frequencies. However, the value of inductance depends critically on the transistor input and output capacitances, and the inevitable spread in the values of these capacitances in manufactured items makes it difficult to predict an exact value for every amplifier.

A better method is to use complex negative feedback to keep the frequency response curve level over a wider range of frequencies, though this has the attendant disadvantage that it lowers the overall gain.

5.8 Exercises

Exercise 5.1

Define Q-factor of a tuned circuit and show how it is related to the bandwidth of the circuit.

The resonant frequency of a parallel tuned circuit is 5 MHz and the effective shunt capacitance is 250 pF. When the signal frequency differs by 20 kHz from the resonant frequency, the circuit impedance falls to 70·7 per cent of the dynamic impedance. Calculate the dynamic impedance and the Q-factor of this circuit.
(Answers: 15·9 kΩ, 125)

Exercise 5.2

Show that a parallel tuned circuit of high Q-factor, shunted by a high resistance, may be regarded as an unshunted parallel tuned circuit of lower effective Q-factor. Determine an expression for the new Q-factor in terms of the constants of the tuned circuit and the shunting resistor.

A parallel tuned circuit has an inductance of 100 μH, a Q-factor of 100, a resonant frequency of 955 kHz, and is shunted by a resistance of 40 kΩ. If a constant current of variable frequency is passed through this shunt combination, determine the bandwidth of the circuit.
(Answer: 23·9 kHz)

Exercise 5.3

Draw labelled high-frequency equivalent circuits for (a) a valve and (b) a transistor. Describe for each device the methods employed both in manufacturing techniques and circuit techniques to obtain good high-frequency amplification. What is meant by the *cut-off frequency* of a transistor?

(ET5)

Exercise 5.4

A single stage, common-emitter, tuned transistor amplifier has an effective load resistance at resonance of 25 kΩ. The transistor h-parameters are h_{ie} = 2 kΩ, h_{fe} = 55, and both h_{re} and h_{oe} are negligible. The signal source connected between base and emitter has an open circuit e.m.f. of 3 mV and resistive internal impedance of 500 Ω. Calculate (a) the signal voltage across the amplifier input terminals (b) the input signal current and (c) the signal power in the collector load. (Assume the effects of biasing and coupling components on the signal to be negligible.) Sketch a typical circuit diagram for the amplifier.
(Answers: 2·4 mV, 1·2 μA, 0·109 mW) (TT5)

Exercise 5.5

The transistor in a tuned amplifier has g_m = 40 mS and r_{ce} = 250 kΩ. The collector load is a parallel circuit having a Q-factor of 90 and resonant at 796 kHz. The coil is tuned by a loss-free capacitor of 200 pF. Calculate from first principles the voltage gain at resonance, and the reduction in gain (stated in dB) at a frequency 12 kHz away from resonance.
(Answers: 2648, 7 dB)

Exercise 5.6

(a) Show that the high frequency hybrid-π equivalent circuit of a transistor may be reduced to the form shown in figure 5.8. Discuss the physical significance of the components. What factors determine the value of the capacitance?

(b) Calculate the high frequency current gain of the circuit shown in figure 5.9. Determine the upper cut-off frequency and

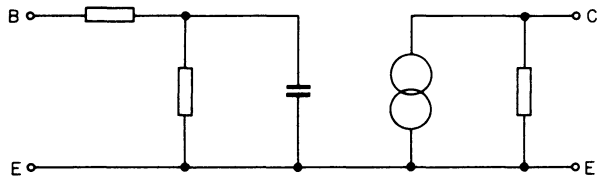


Figure 5.8

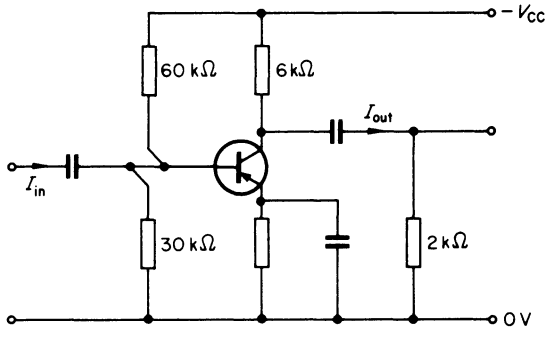


Figure 5.9

sketch the high-frequency current-gain response curve. Neglect the effect of coupling and decoupling capacitors.
Assume that $r_{b'e}$ = 1·5 kΩ, g_m = 0·02 S, $C_{b'c}$ = 1000 pF, $C_{b'c}$ = 50 pF and $r_{bb'}$ = 100 Ω. State any assumptions made.
(Answers: 44·7 kHz) (I.E.R.E.)

Exercise 5.7

The frequencies at which the gain of an amplifier is 3 dB below that at midband are commonly used to define the bandwidth. Comment briefly on the merits or otherwise of this empirical definition.

Two amplifiers, whose lower and upper cutoff frequencies (defined in the above way) are respectively 50 Hz and 2 MHz, and 30 Hz and 3 MHz, are connected in cascade as part of a sensitive electronic voltmeter.

What are the lower and upper frequencies for which the overall gain is 95 per cent of that at midband? Assume each amplifier to have a 6 dB/octave cutoff.
(Answer 293 kHz, 179·2 Hz) (I.E.E.)

6 Field-effect transistors

6.1 Junction FET and common-source amplifier

Sketch the construction and describe the principle of operation of a junction field-effect transistor. Explain what is meant by pinch-off and show its effect on the drain characteristic curves.

Draw the circuit diagram of an automatically biased junction FET used as a class-A amplifier in the common-source mode.

Compare its input resistance and voltage gain with (a) a voltage amplifying pentode; (b) a junction transistor connected as a common-emitter voltage amplifier.

(ET4)

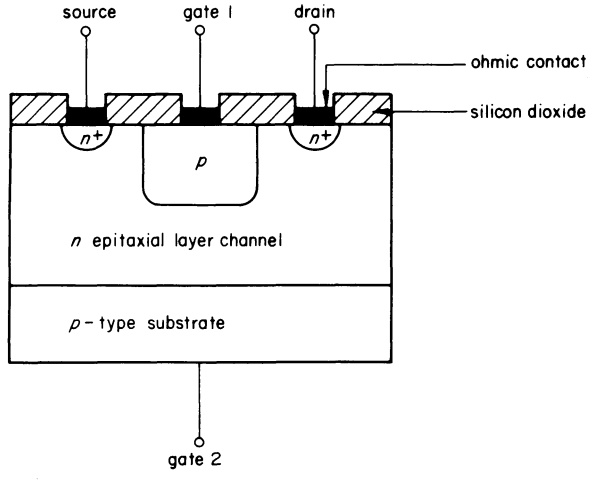


Figure 6.1

Figure 6.1 shows the construction of an FET using a single *n*-type epitaxial layer on a *p*-type substrate. The FET is manufactured by the planar process described in chapter 2, and consists essentially of a length of *n*-type semiconductor with ohmic contacts made at each end, together with two *p*-type regions known as gates. The length of *n*-type material between the two gates is known as the channel. If the gates are short-circuited to the source terminal and a positive potential V_{DS} is applied between drain and source, a flow of electrons will take place from source to drain. Note that one essential difference between the FET and the bipolar junction transistor is that only majority carriers are used for current flow in the FET, and it is known as a unipolar device.

As the channel has a finite resistivity, there will be an approximately linear rise in potential along the channel from source to drain. As the gates are at the same potential as the source, they form reverse-biased *pn* junctions with the channel, and depletion layers are formed as shown in figure 6.2. Note that the depletion

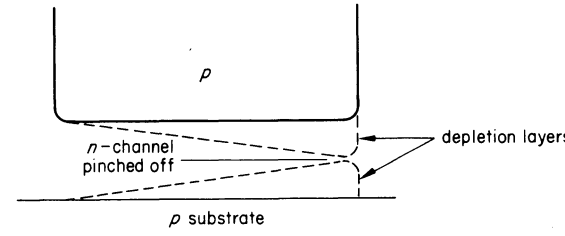


Figure 6.2

layers will be widest at the drain end because the reverse bias is a maximum at that end. Thus, current flow is restricted to the wedge-shaped channel shown. If the drain voltage is increased, the depletion layers eventually meet, and the channel is said to be *pinched-off*. Further increase in drain voltage produces very little increase in drain current, as the pinched-off channel tends to spread back towards the source.

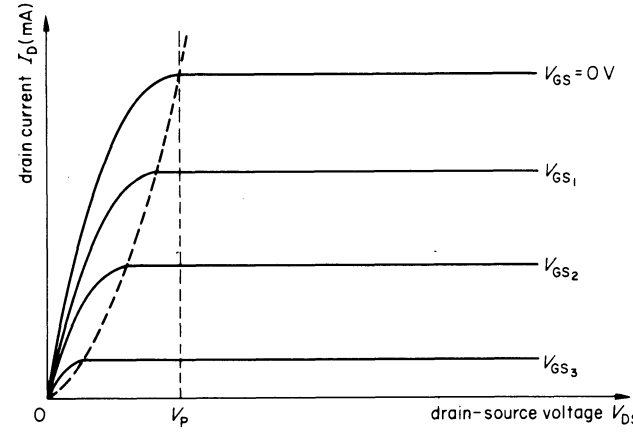


Figure 6.3

In figure 6.3, considering the characteristic for zero gate-source voltage $V_{GS} = 0$, initially, as drain voltage V_{DS} is increased, the channel acts as a semiconductor resistor, and the drain current I_D increases approximately linearly with increase in V_{DS}. When pinch-off occurs the characteristic becomes nearly flat, as can be seen

from figure 6.3. The value of drain voltage V_{DS} at this point is referred to as the *pinch-off voltage* V_P.

If the gate-source is now negatively biased, then the depletion layers will be thicker for a given value of V_{DS} than when there is no bias. This means that pinch-off and saturation of I_D will occur at lower values of V_{DS} and I_D. Figure 6.3 shows a set of drain characteristics as V_{GS} is increased negatively; a pinch-off locus can be drawn obeying the equation

$$|V_{DS}| = |V_P| - |V_{GS}|$$

To the left of this locus, the FET acts like a variable resistor and this region is referred to as the *ohmic* or *triode region*. To the right of the locus, the FET has a very low output conductance, and this is termed the *pinch-off region.*

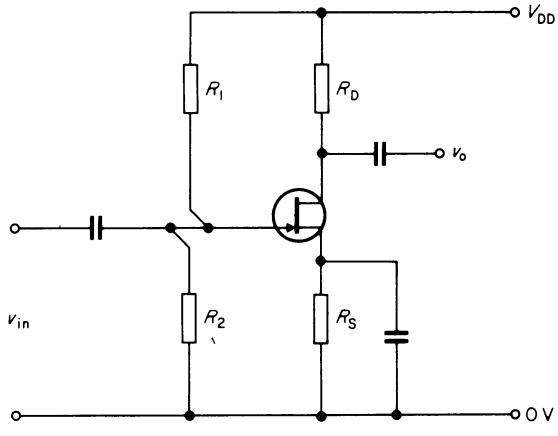


Figure 6.4

Figure 6.4 shows the circuit diagram of a common-source amplifier which has a similar layout to that of the common-emitter transistor amplifier using potential divider stabilisation. The input impedance of the FET is very high (10^3 to 10^6 MΩ), as its input circuit essentially consists of a reverse-biased diode, though this is shunted by the potential-divider resistors R_1 and R_2. Nevertheless, it is still higher than that of a pentode amplifier, and very much higher than a common-emitter transistor amplifier. Its voltage gain, however, is much lower than those of the pentode and common-emitter amplifiers.

6.2 Depletion and enhancement type insulated gate FETs

Describe the principle of operation and sketch the BS symbol of either of the following insulated gate field effect transistors (MOSTs) (i) depletion type (ii) enhancement type. Illustrate your answer with appropriate sketches and draw typical gate/drain characteristic curves.

What is the name given to the value of gate voltage at which drain current ceases to flow, in the type you have described?

(ET4)

The metal oxide semiconductor field-effect transistor, which is the more usual form of insulated gate FET, differs from the junction FET by having its gate electrode isolated from the channel by a thin layer of insulating material, usually silicon dioxide, as shown in figure 6.5.

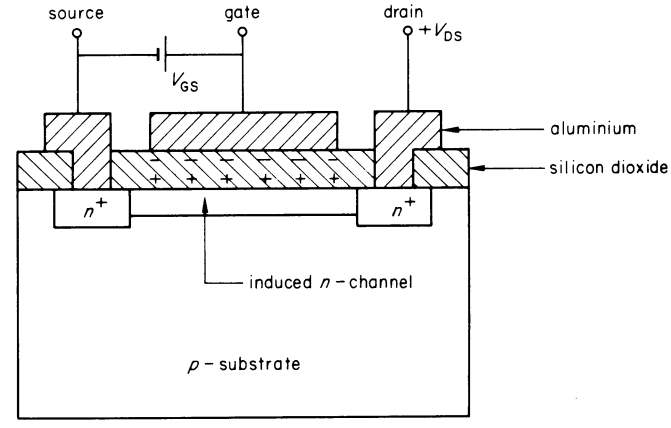


Figure 6.5

In figure 6.5, when a positive voltage V_{GS} is applied between gate and source, a negative charge is induced in the silicon dioxide layer near the gate terminal, and this is counterbalanced by a positive charge in the silicon dioxide near its junction with the substrate. This positive charge repels the majority carriers at the surface of the *p*-substrate and causes the surface to change its conductivity type; that is, the minority electrons cause an *n*-channel to be formed in the *p*-substrate (because of thermal and other effects). Therefore, when a positive drain voltage V_{DS} is applied, electrons flow from source to drain. If the gate-source voltage V_{GS} is increased, the channel becomes wider or is said to be *enhanced*; hence, this is an *n*-channel *enhancement type* IGFET.

Figures 6.6a and 6.6b show the drain and gate characteristic curves for an *n*-channel enhancement mode IGFET (note that, in the enhancement mode, the gate characteristic does not cross the

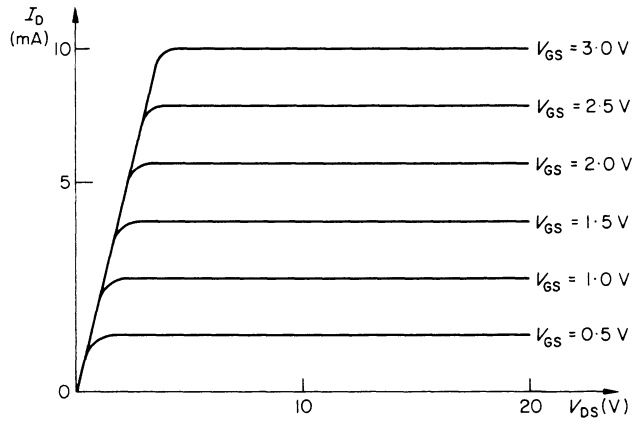


Figure 6.6a

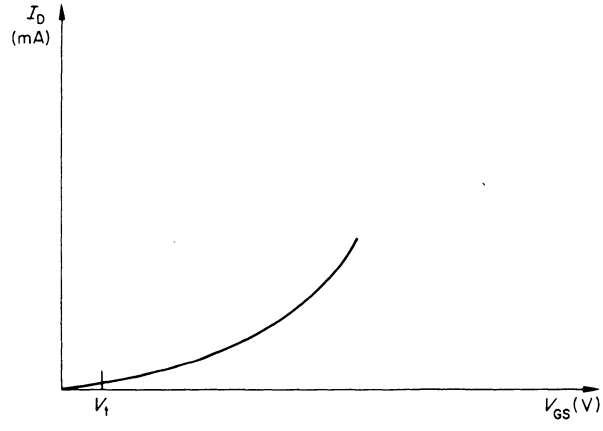


Figure 6.6b

Y-axis). The value of gate-source voltage at which the drain current falls to zero, is referred to as the *threshold voltage* V_t and is analogous to the *pinch-off* voltage of a junction FET.

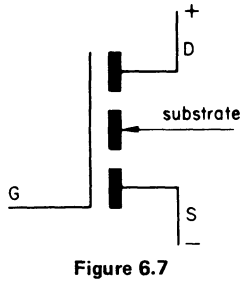


Figure 6.7

Figure 6.7 shows the BS symbol for an *n*-channel enhancement IGFET. Because these are normally-off devices, their symbols incorporate broken lines to represent channels that are normally open circuit. The polarity is denoted by the arrow, which represents the *pn* direction of the channel-substrate junction. The substrate is thus always marked even though no physical connection may be made to it.

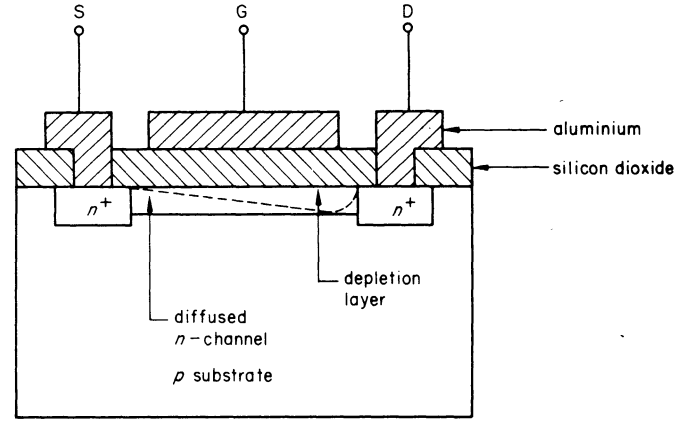


Figure 6.8

Figure 6.8 shows the construction of an *n*-channel *depletion mode* IGFET, in which the *n*-channel is introduced during manufacture by moderate *n*-type doping of the surface layer of the substrate between source and drain n^+ regions. Therefore, even with zero gate-source voltage, a positive drain voltage V_{DS} causes a flow of electrons between drain and source. If a negative gate-source voltage is applied however, the *n*-channel is depleted (that is, narrowed) as electrons are expelled from the depletion layer, and the flow of electrons from drain to source is increased. Similarly, if a positive gate-source voltage is applied the channel is enhanced and electron flow increases. Therefore, this type of IGFET can operate both in the enhancement and depletion modes.

Figures 6.9a and 6.9b show the drain and gate characteristic curves of an *n*-channel depletion mode IGFET. Note that the threshold voltage V_t now has a negative value and that the drain current for zero gate-source voltage is given the symbol I_{DSS}. The BS symbol for this type of IGFET is shown in figure 6.10.

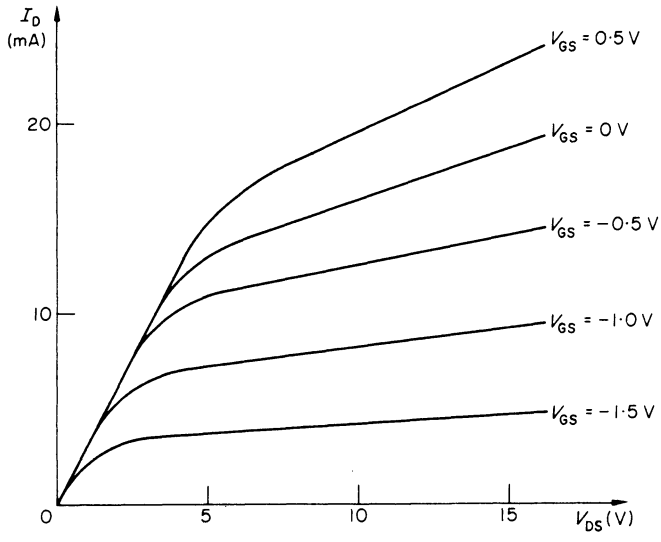


Figure 6.9a

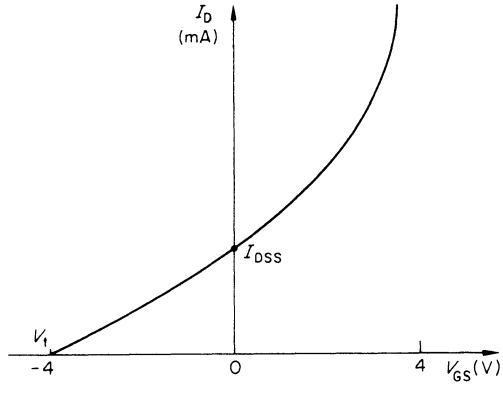


Figure 6.9b

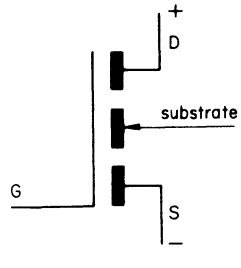


Figure 6.10

6.3 Mutual conductance of an FET

For nearly all FETs operating in the saturation region, the following equation is true

$$I_D = I_{DSS}(1 - V_{GS}/V_P)^2 \qquad (6.1)$$

Define each term in the equation and derive an expression for the mutual conductance (transconductance) of an FET. Indicate how the value of mutual conductance can be calculated when $V_{GS} = 0$.

In the above equation

I_D = drain current
I_{DSS} = drain current when gate-source voltage is zero
V_{GS} = gate-source voltage
V_P = pinch-off voltage

The mutual conductance of an FET, defined for small signal changes, is given the symbol g_{fs}, and is the small change in drain current produced by a small change in gate-source voltage.

$$g_{fs} = \frac{dI_D}{dV_{GS}}$$

Differentiating equation 6.1

$$g_{fs} = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) \qquad (6.2)$$

When $V_{GS} = 0$, from equation 6.2

$$g_{fso} = \frac{-2I_{DSS}}{V_P}$$

This is the value of mutual conductance for zero gate-source voltage. I_{DSS} and V_P are easily found, by direct measurement, and hence g_{fso} can be found. Alternatively, it can be found from the gate characteristics as shown in figure 6.11.

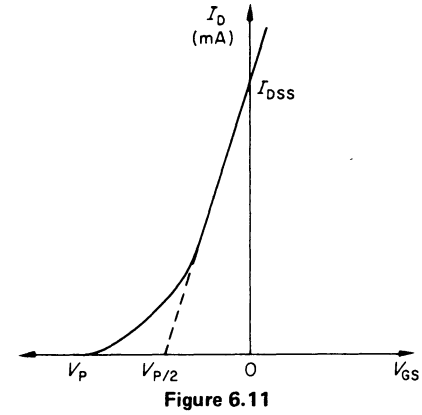


Figure 6.11

6.4 Equivalent circuit of common-source amplifier

Draw the small-signal equivalent circuit of a junction FET in common-source mode, operating in the pinch-off region, explaining the significance of each term. Hence, derive an expression for the input capacitance of this FET.

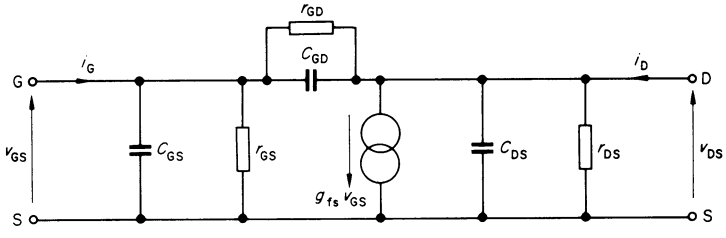


Figure 6.12

Figure 6.12 shows the small-signal equivalent circuit of an FET. The gate leakage resistance r_{GS} to source and r_{GD} to drain have very high values (exceeding $10^9\ \Omega$), though these are shunted by the gate-source and gate-drain capacitances respectively.

r_{DS} is the incremental resistance of the channel and is usually about 500 Ω. This is shunted by the channel capacitance C_{DS}, which mainly consists of the encapsulation or header capacitance and is therefore much smaller than either C_{GS} or C_{GD}. Finally, as g_{fs} is the mutual conductance of the FET, the output current generator is represented by $g_{fs}v_{GS}$, where g_{fs} is positive for the direction of current shown in the diagram.

If the drain and source are short-circuited for a.c., the input capacitance C_{iss} will be given by

$$C_{iss} \approx C_{GS} + C_{GD} \qquad (6.3)$$

However, when the drain and source are not short-circuited, the effective input capacitance will be increased by the *Miller effect.*

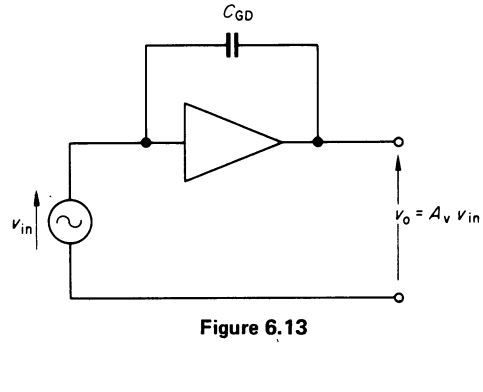


Figure 6.13

Figure 6.13 shows the block diagram of the FET regarded as an amplifier of gain A_v with C_{GD} connected across it. Therefore voltage across $C_{GD} = v_{in} - v_o = \int i\,dt/C_{GD}$. Substituting for v_o

$$v_{in}(1 - A_v) = \int i\,dt/C_{GD}$$

$$v_{in} = \frac{\int i\,dt}{(1 - A_v)C_{GD}}$$

Hence the apparent input capacitance is given by

$$C_{in} = C_{GS} + (1 - A_v)C_{GD} \qquad (6.4)$$

$C_{in} > C_{iss}$, because A_v has a negative numerical value, and thus the apparent input capacitance is increased. As the reverse transfer capacitance C_{rss} is equal to the gate-drain capacitance C_{GD}, and as C_{DS} is normally much smaller than C_{rss}, then

$$C_{rss} \approx C_{oss}$$

In equation 6.3

$$C_{iss} = C_{GS} + C_{rss}$$

so that

$$C_{GS} = C_{iss} - C_{rss}$$

Substituting in equation 6.4

$$C_{in} = C_{iss} - C_{rss} + (1 - A_v)C_{rss}$$
$$= C_{iss} - A_v C_{rss}$$

For a junction FET with C_{iss} = 4 pF, C_{rss} = 1 pF and A_v = 10,

$$C_{in} = 14\ \text{pF}$$

6.5 Pinch-off region of junction FET

Describe, with the aid of diagrams and characteristic curves, the operation of the junction FET. State an experimental expression for the drain current, I_D, in the pinch-off region.

Figure 6.14 shows an amplifier using an n-channel FET, for which $V_P = -3$ V and $I_{DSS} = 2{\cdot}5$ mA. It is desired to bias the circuit at $I_D = 1{\cdot}2$ mA, using $V_{DD} = 20$ V. Assume that the resistance from drain to source $r_{DS} \gg R_d$. Find (i) V_{GS}; (ii) the transconductance g_{fs}; (iii) R_s; (iv) R_d, such that the voltage gain is at least 20 dB, *with R_s by-passed with a large capacitor.*

(H.N.C.)

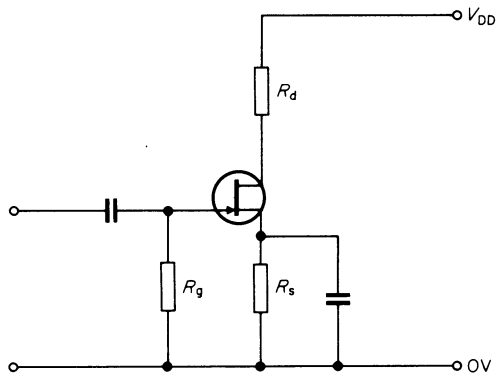


Figure 6.14

The operation and characteristic curves of the junction FET have already been dealt with in section 6.1. The expression for the drain current is

$$I_D = I_{DSS}(1 - V_{GS}/V_P)^2 \qquad (6.5)$$

(i) Substituting the values given

$$1{\cdot}2 = 2{\cdot}5(1 + V_{GS}/3)^2$$

$$V_{GS}/3 = \left(\frac{1{\cdot}2}{2{\cdot}5}\right)^{1/2} - 1$$

$$V_{GS} = -0{\cdot}922 \text{ V}$$

(ii) $$g_{FS} = dI_D/dV_{GS}$$

$$= \frac{-2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) \qquad (6.6)$$

From equation 6.5

$$(I_D/I_{DSS})^{1/2} = 1 - V_{GS}/V_P$$

Substituting in equation 6.6

$$g_{FS} = \frac{-2I_{DSS}}{V_P}\left(\frac{I_D}{I_{DSS}}\right)^{1/2}$$

$$= -2\left(\frac{2{\cdot}5}{-3}\right)\left(\frac{1{\cdot}2}{2{\cdot}5}\right)^{1/2}$$

$$= 1{\cdot}15 \text{ mS}$$

(iii) $$R_S = -V_{GS}/I_D = \frac{0{\cdot}922}{1{\cdot}2 \times 10^{-3}} = 768\ \Omega$$

(iv) Neglecting the capacitors, the equivalent output circuit for low frequency operation is shown in figure 6.15, neglecting the shunting effect of r_{DS} on R_d (as $r_{DS} \gg R_d$).

Therefore voltage gain

$$A_v = v_o/v_{in} = -g_{FS}R_d$$

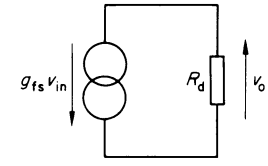


Figure 6.15

As 20 dB corresponds to a voltage gain of 10, $g_{FS}R_d \geqslant 10$ therefore

$$R_d \geqslant \frac{10}{1{\cdot}155 \times 10^{-3}}$$

that is

$$R_d \geqslant 8{\cdot}66 \text{ k}\Omega$$

6.6 Voltage gain and input resistance of common-source amplifier

(a) Explain the difference between the terms 'pinch-off region' and 'pinch-off voltage' in a field-effect transistor.

(b) Why does the bias arrangement used in the class-A amplifier shown in figure 6.16 give good d.c. stability? What is the purpose of R_2? The FET used has a mutual conductance of 3 mS *and the circuit output is connected to an external load of 3* kΩ.

If R_1 = 47 kΩ, *R_2 = 1* MΩ, *R_3 = 5·1* kΩ, *R_4 = 1* kΩ, *R_5 = 1* kΩ, *determine (i) the voltage gain; (ii) the circuit a.c. input resistance. State any assumptions made.*

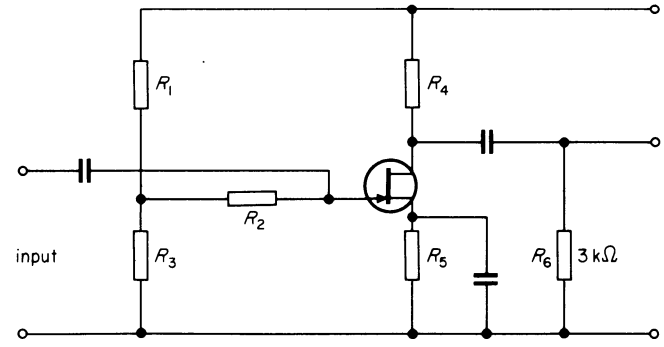


Figure 6.16

(ET4)

(a) The terms *pinch-off voltage* and *pinch-off region* have already been defined (see section 6.1).

(b) The bleed current through R_1 and R_3 is very large compared with the gate current, and the d.c. gate voltage is fixed by this bleed current, and is relatively unaffected by changes in temperature, etc. If the drain current increases, the voltage across R_5 increases, and the consequent increase in gate-source voltage thereby decreases the drain current. Hence, the d.c. stability is improved.

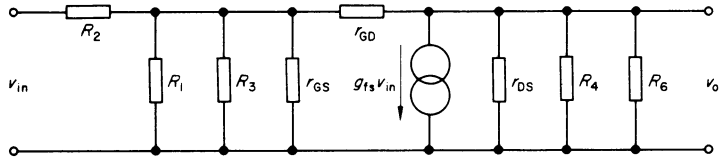


Figure 6.17

Figure 6.17 shows the small-signal low-frequency equivalent circuit of the amplifier shown in figure 6.16, assuming that all the FET capacitances can be neglected at low frequencies. Normally r_{GS} and r_{GD} are large compared with R_1 and R_3 and can therefore be neglected. Without R_2, the input resistance of the circuit would be R_1 and R_3 in parallel; that is, 4·6 kΩ, which is very low for a voltage amplifier. With R_2 in circuit, the a.c. input resistance is increased by the same amount. Thus, in practice, a.c. input resistance is R_2 = 1 MΩ.

(i) Assuming $r_{DS} \gg R_4$ and R_6, output voltage v_o is given by

$$v_o = -g_{fs}v_{in}\frac{R_4R_6}{R_4 + R_6}$$

Low-frequency voltage gain

$$A_{vo} = v_o/v_{in}$$
$$= -3 \times 1 \times \tfrac{3}{4}$$
$$= -2{\cdot}25$$

The minus sign indicates the 180° phase shift between input and output voltages.

6.7 Voltage gain and upper cut-off frequency of common-source amplifier

Figure 6.18 shows the basic form of a common-source amplifier, omitting the detailed bias circuit. R_G is the equivalent series input resistance consisting of a combination of signal-source internal resistance and bias components resistance. Show that the voltage gain remains appreciably constant for varying frequencies if $|g_{fs}/j\omega C_{GD}| \gg 1$ *and* $\gg A_{vo}$ *(where* A_{vo} *= low frequency gain).*

Determine the value of voltage gain if g_{fs} *= 1·5* mS *and* R_L *= 8·2* kΩ.

Determine also the upper cut-off frequency, given R_G *= 1* MΩ, *and for the FET,* C_{GS} *= 4* pF *and* C_{GD} *= 2* pF. *Comment on this result.*

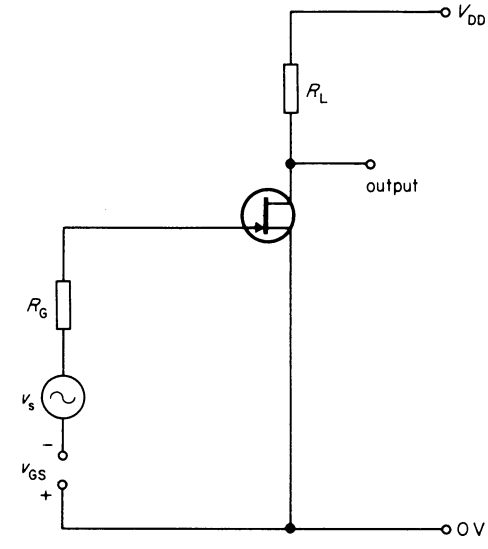


Figure 6.18

The equivalent circuit of the amplifier at low frequencies is shown in figure 6.19.

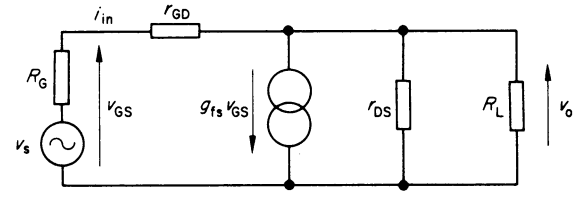


Figure 6.19

From figure 6.19

$$v_o = -g_{fs}v_{GS}R$$

where

$$R = r_{DS}R_L/(r_{DS} + R_L)$$

Therefore, the low-frequency voltage gain

$$A_{vo} = v_o/v_s = -g_{fs}R \qquad (6.7)$$

At frequencies where the capacitive reactances cannot be neglected, the equivalent circuit is as shown in figure 6.20.

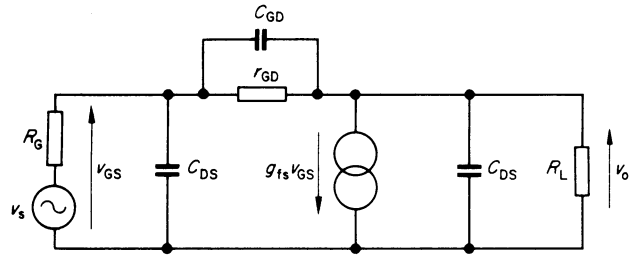


Figure 6.20

To determine the voltage gain at any frequency, it is convenient to use a constant voltage generator and equivalent series resistance as shown in figure 6.21.

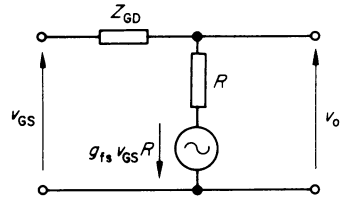


Figure 6.21

In figure 6.21, it is assumed that the reactance of C_{DS} is large compared with R at the frequencies under consideration; hence, it is neglected. Z_{GD} is the impedance of R_{GD} and C_{GD} in parallel. From figure 6.21

$$v_o = -g_{fs}v_{GS}R + iR$$

$$= -v_{in}g_{fs}R + \frac{R(v_{in} - v_o)}{Z_{GD}}$$

$$= v_{in}A_{vo} - \frac{(v_{in} - v_o)A_{vo}}{g_{fs}Z_{GD}}$$

Voltage gain

$$A_v = v_o/v_{in} = A_{vo} - \frac{(1 - A_v)A_{vo}}{g_{fs}Z_{GD}}$$

therefore

$$A_v = A_{vo}(g_{fs}Z_{GD} - 1)/(g_{fs}Z_{GD} - A_{vo}) \qquad (6.8)$$

At frequencies where the reactance of C_{GD} is much larger than r_{GD}, equation 6.8 becomes

$$A_v = \frac{A_{vo}(g_{fs}/j\omega C_{GD} - 1)}{g_{fs}/j\omega C_{GD} - A_{vo}}$$

Hence if

$$|g_{fs}/j\omega C_{GD}| \gg 1 \text{ and is also} \gg A_{vo}, \quad A_v \approx A_{vo}$$

If $r_{DS} \gg R_L$, then from equation 6.7

$$A_{v0} = -1{\cdot}5 \times 8{\cdot}2 = -12{\cdot}3$$

The equivalent input circuit is shown in figure 6.22.

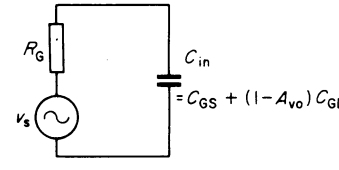


Figure 6.22

In this circuit, r_{GS} is much larger than R_G and than the reactance of C_{in}, and so it is neglected.

Thus upper cut-off frequency

$$f = \frac{1}{2\pi C_{in}R_G}$$

$$= \frac{1}{2\pi \times 30{\cdot}6 \times 10^{-12} \times 10^6} = 5{\cdot}2 \text{ kHz}$$

This is a very low cut-off frequency and thus the common-source amplifier makes effective use of the very high input resistance at low frequencies only.

6.8 Source-follower amplifier

Determine the low frequency voltage gain and upper cut-off frequency of the simple common-drain (source-follower) amplifier shown in figure 6.23.

The parameters of the FET are $g_{fs} = 1{\cdot}5$ mS, $C_{GD} = 4$ pF, $C_{GS} = 2$ pF.

The equivalent circuit is shown in figure 6.24.

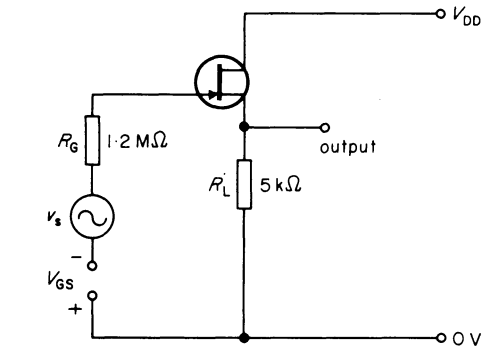


Figure 6.23

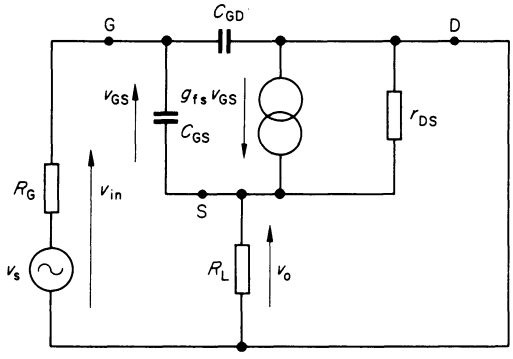


Figure 6.24

The very high gate-source and gate-drain resistances have been neglected, and at low frequencies the reactances of the capacitors are very high and take negligible current.

Therefore

$$g_{fs}v_{GS} = v_o(1/R_L + 1/r_{DS}) \qquad (6.9)$$

Also

$$v_{GS} = v_{in} - v_o$$

In equation 6.9

$$g_{fs}(v_{in} - v_o) = v_o(1/R_L + 1/r_{DS})$$

this low-frequency voltage gain

$$A_{vo} = v_o/v_{in} = \frac{g_{fs}}{g_{fs} + 1/R_L + 1/r_{DS}}$$

As the FET is working in the pinched-off region, $r_{DS} \gg R_L$

$$A_{vo} \approx \frac{g_{fs}R_L}{1 + g_{fs}R_L}$$

$$= \frac{1{\cdot}5 \times 5}{1 + (1{\cdot}5 \times 5)} = 0{\cdot}88$$

At high frequencies, where the effects of C_{GS} and C_{GD} cannot be neglected, from figure 6.24

$$i_{in} = v_{in}j\omega C_{GD} + (v_{in} - v_o)j\omega C_{GS}$$

thus

$$Y_{in} = i_{in}/v_{in} = j\omega[C_{GD} + (1 - A_v)C_{GS}]$$

and effective input capacitance

$$C_{in} = C_{GD} + (1 - A_v)C_{GS}$$

$$= 4 + (1 - 0{\cdot}88)2 \quad (\text{as } A_v \approx A_{vo})$$

$$= 4{\cdot}24 \text{ pF}$$

This is much lower than that of the common-source stage.
Cut-off frequency

$$f_c = \frac{1}{2\pi C_{in}R_G}$$

$$= \frac{10^{12}}{2\pi \times 4{\cdot}24 \times 1{\cdot}2 \times 10^6}$$

$$= 31{\cdot}25 \text{ kHz}$$

Thus, the bandwidth is much larger than that of the corresponding common-source amplifier.

6.9 Voltage gain of common-drain amplifier

(a) Describe in detail the construction and principle of operation of (i) the junction field-effect transistor; (ii) the insulated-gate field-effect transistor.

(b) Define the terms mutual conductance, g_{fs}, and slope resistance, r_{ds}, as applied to the field-effect transistor.

(c) Calculate the voltage gain v_o/v_{in} of the common-drain stage, shown in figure 6.25. It may be assumed that g_{fs} = 1·2 mS, r_d = 20 kΩ and that r_{GD} and r_{GS} are very much greater than 1 MΩ. The effect of the capacitor C can be ignored.

(I.E.R.E.)

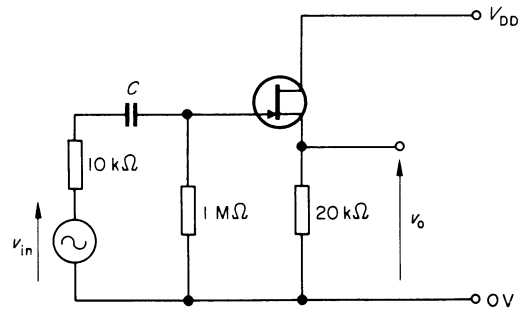


Figure 6.25

(a) This part of the question has already been covered in sections 6.1 and 6.2.

(b) Mutual conductance is the ratio of a small change in drain current to the small change in gate-source voltage which caused it; and is expressed as

$$g_{fs} = dI_D/dV_{GS}$$

The slope resistance is the ratio of a small change in drain-source voltage to the corresponding small change in drain current, and is expressed as

$$r_{ds} = dV_{DS}/dI_D$$

(c) The equivalent circuit at low frequencies of the amplifier shown in figure 6.25, is given in figure 6.26.

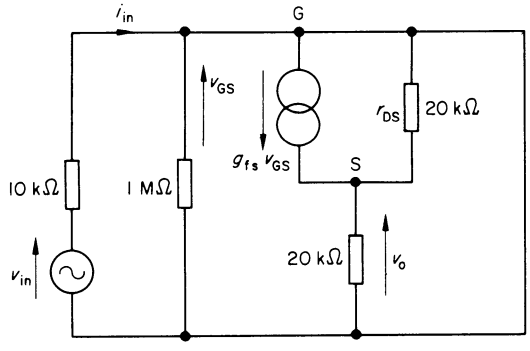


Figure 6.26

In figure 6.26

$$v_{GS} = v_{in} - 10i_{in} - v_o \qquad (6.10)$$

$$v_o = g_{fs}v_{GS}10 = 12v_{GS} \qquad (6.11)$$

Also

$$v_{GS} + v_o = (i_{in} - g_{fs}v_{GS})1000$$

$$= 1000i_{in} - 1200v_{GS}$$

$$i_{in} = 1{\cdot}201v_{GS} + \frac{v_o}{1000}$$

substitute for v_{GS} from equation 6.11

$$i_{in} = 1213v_o/12\,000$$

Substituting for i_{in} and v_{GS} in equation 6.10

$$\frac{v_o}{12} = v_{in} - \frac{1213}{1200}v_o - v_o$$

therefore

$$v_o(100 + 1213 + 1200) = 1200v_{in}$$

Voltage gain

$$A_v = v_o/v_{in} = 1200/2513 = 0{\cdot}477$$

6.10 Common-gate amplifier

Figure 6.27 shows the circuit diagram of a basic common-gate FET amplifier.

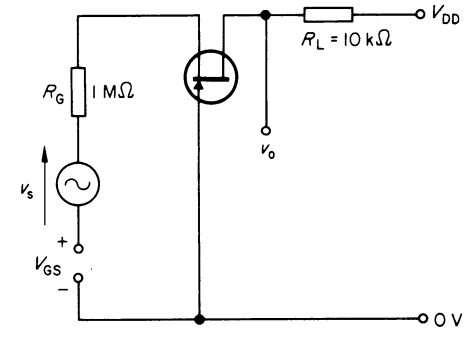


Figure 6.27

Calculate the a.c. input resistance and low-frequency voltage gain of this stage given the following FET parameters, g_{fs} = 1·5 mS, r_{DS} = 50 kΩ, all other parameters being negligible.

Discuss the use of this type of amplifier in practice.

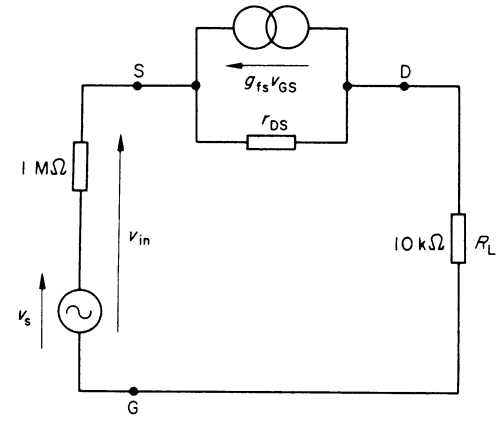


Figure 6.28a

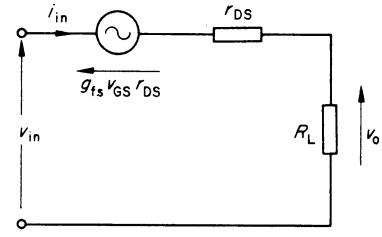


Figure 6.28b

Figure 6.28a shows the equivalent circuit of the common-gate amplifier and figure 6.28b shows the same circuit with the current generator and parallel r_{DS} replaced by the equivalent voltage generator and series r_{DS}. Thus

$$v_{in} - g_{fs}r_{DS}v_{GS} = i_{in}(r_{DS} + R_L)$$

But

$$v_{GS} = -v_{in}$$

therefore

$$v_{in}(1 + 1{\cdot}5 \times 50) = i_{in}60 \times 10^3$$

Input resistance

$$r_{in} = v_{in}/i_{in} = 60 \times 10^3/76 = 789\ \Omega$$

Also

$$v_o = i_{in}R_L = R_L(v_{in} + g_{fs}v_{in}r_{DS} - v_o)/r_{DS}$$
$$= 0{\cdot}2v_{in} + 15v_{in} - 0{\cdot}2v_o$$

therefore voltage gain

$$A_v = v_o/v_{in} = 15{\cdot}2/1{\cdot}2 = 12{\cdot}7$$

It can be seen that the input resistance of this stage is lower than that of a common-emitter transistor amplifier. Its voltage gain also is lower. Thus, the main advantage of the FET amplifier (that is, its high input-resistance) has been lost. This mode of operation is therefore used only occasionally, and then only at high frequencies.

6.11 Voltage gain, input and output impedances of source-follower

(a) State the properties of a source-follower.

(b) Estimate the voltage gain, input impedance and output impedance of the circuit shown in figure 6.29.

(c) What is the purpose of capacitor C in the circuit? For the FET g_{fs} = 3·6 mS. Other parameters may be neglected.

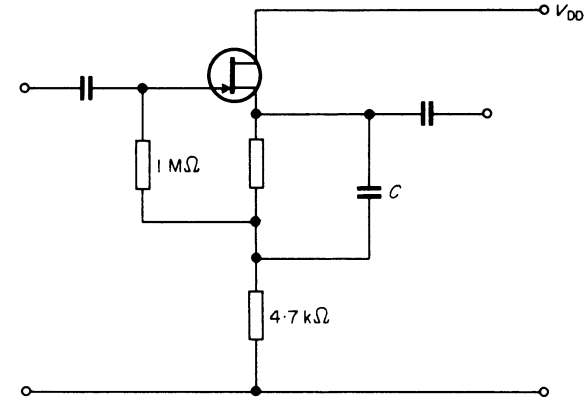


Figure 6.29

(ET5)

(a) A source-follower has a very high input impedance (megohms), a low output impedance (a few hundred ohms), a voltage gain just less than unity, and a zero phase shift from input to output.

(b) Figure 6.30 shows the equivalent circuit of the source-follower of figure 6.29.

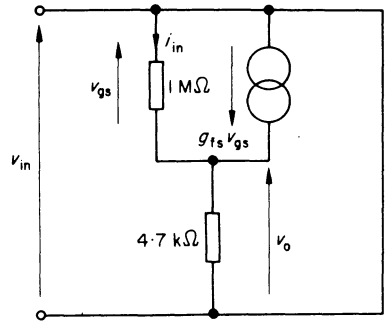


Figure 6.30

From this

$$v_{in} = i_{in}10^6 + (3{\cdot}6 \times 10^{-3}v_{gs} + i_{in})4{\cdot}7 \times 10^3$$
$$= i_{in}10^6 + 16{\cdot}92v_{gs} + i_{in}4{\cdot}7 \times 10^3$$

The last term is negligible with respect to the first term in this equation.
Therefore

$$v_{in} = i_{in}10^6 + 16{\cdot}92v_{gs} \qquad (6.12)$$

Also

$$v_{gs} = i_{in}10^6$$

substituting this in equation 6.12

$$v_{in} = 17{\cdot}92v_{gs} \qquad (6.13)$$

From figure 6.30

$$v_{gs} = v_{in} - v_o$$

Substituting in equation 6.13

$$v_{in} = 17{\cdot}92(v_{in} - v_o)$$

therefore voltage gain

$$A_v = v_o/v_{in} = 16{\cdot}92/17{\cdot}92 = 0{\cdot}944$$

Substituting for v_{gs} in equation 6.13

$$v_{in} = 17{\cdot}92 \times 10^6 i_{in}$$

therefore input resistance

$$r_{in} = v_{in}/i_{in} = 17{\cdot}92\ \text{MΩ}$$

Figure 6.31 shows the equivalent circuit required to determine the output impedance, with the load replaced by a voltage generator e and the voltage source replaced by its internal impedance (which is negligible in this calculation). From this circuit

$$e = (i + g_{fs}v_{gs})10^6$$

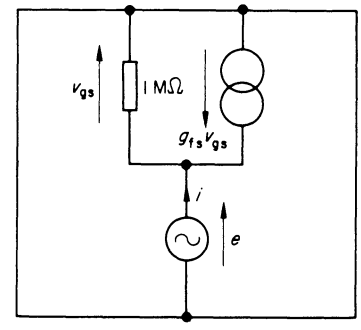


Figure 6.31

Also

$$v_{gs} = -e$$
$$e = 10^6 i - 3{\cdot}6 \times 10^3 e$$

Therefore output impedance

$$r_o = e/i \approx 10^6/3{\cdot}6 \times 10^3 = 278\ \Omega$$

(c) The capacitor C is used to decouple the unmarked resistor; that is, it will have negligible reactance at the operating frequency of the amplifier. Thus for a.c. the 1 MΩ and 4·7 kΩ resistors are effectively connected to the FET source.

6.12 Exercises

Exercise 6.1

A junction FET obeys the square-law relationship

$$I_D = I_{DSS}(1 - V_{GS}/V_P)^2$$

If I_{DSS} = 5 mA and V_p = −8 V, calculate I_D and g_{fs} at V_{GS} = 0, −2, −4, −6 and −8 V. Hence plot a graph of I_D against V_{GS}. The maximum slope of this graph occurs when V_{GS} = 0; if this slope is extended show that it cuts the voltage axis at $V_P/2$.

Exercise 6.2

Show that the input capacitance of a field-effect transistor in the common-source mode is

$$C_{in} = C_{GS} + C_{GD}(1 - A_V)$$

where

C_{GS} is the gate-source capacitance
C_{GD} is the gate-drain capacitance
A_V is the voltage gain of the stage

(U.L.C.I.)

Exercise 6.3

The simple common-source amplifier shown in figure 6.32 is to have a voltage gain of 21·6 dB with R_s effectively decoupled down to 31·8 Hz.

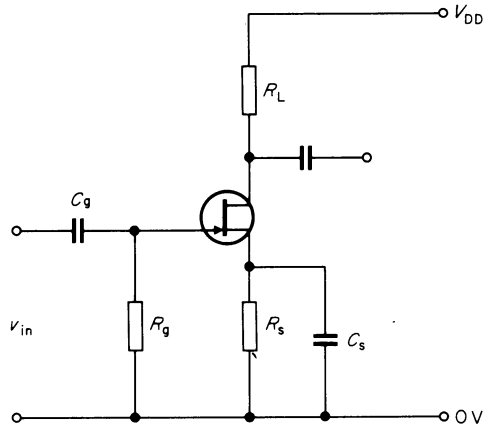


Figure 6.32

For the FET, $V_P = -2$ V, $I_{DSS} = 2$ mA, and at the operating condition $I_D = 1$ mA. Calculate V_{GS}, g_{fs}, R_s, C_s and R_L assuming $r_{DS} \gg R_L$.
(Answers: −0·59, 1·41 mS, 590 Ω, 85 μF, 8·5 kΩ)

Exercise 6.4

In the common-source amplifier shown in figure 6.32, if $R_L = 5$ kΩ, $R_g = 1{\cdot}2$ MΩ, $R_S = 1$ kΩ, $V_{DD} = 25$ V, $I_{DSS} = 4$ mA, $V_P = -3$ V, $r_{DS} = 50$ kΩ and $g_{fs} = 2$ mS, all other parameters being negligible, determine (a) I_D; (b) V_{GS}; (c) the quiescent drain voltage V_D; (d) the voltage gain A_v at frequencies where C_g and C_s are negligible.
(Answers: 2·25 mA, −0·75 V, 13·75 V, 9·1)

Exercise 6.5

In the common-source amplifier shown in figure 6.33, under quiescent conditions, $V_{GS} = -1{\cdot}5$ V and the drain current $I_D = 5$ mA.

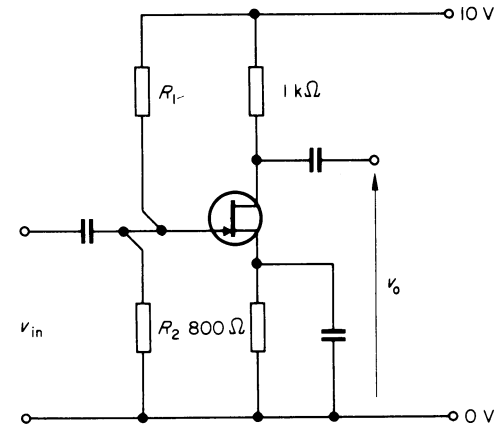


Figure 6.33

Assuming the input resistance of the FET is infinite, determine the values of R_1 and R_2 such that the input resistance of the stage will be 1·5 MΩ. Determine also the low-frequency voltage gain if $g_{fs} = 10$ mS.
(Answers: 6 MΩ, 2 MΩ, 10)

Exercise 6.6

In a simple common-source amplifier, the equivalent series input resistance is 1·2 MΩ. The parameters of the FET are $g_{fs} = 1{\cdot}8$ mS, $C_{GD} = 2{\cdot}6$ pF, $C_{GS} = 4$ pF, $r_{DS} = 100$ kΩ, and the load resistor is 20 kΩ. Determine the low-frequency voltage gain and upper cut-off frequency of the amplifier.
(Answers: 30, 1·6 kHz)

Exercise 6.7

An FET has the following equivalent circuit parameters, $g_{fs} = 50$ mS, $r_{DS} = 1$ MΩ. When used as a simple source-follower, its voltage gain is found to be 0·95. Find the value of the source load.
(Answer: 380 Ω) (U.L.C.I.)

Exercise 6.8

Show that at low frequencies the output impedance of a source-follower is given by

$$Z_o = 1/R_s + g_{DS} + g_{fs}$$

where R_S is the source load resistor, g_{DS} is the FET output admittance ($1/r_{DS}$) and g_{fs} is the FET mutual conductance.

Exercise 6.9

Determine the voltage gain v_o/v_s of the source-follower stage shown in figure 6.34 given g_{fs} = 3 mS, r_{DS} = 80 kΩ, and the effect of all other components may be neglected.

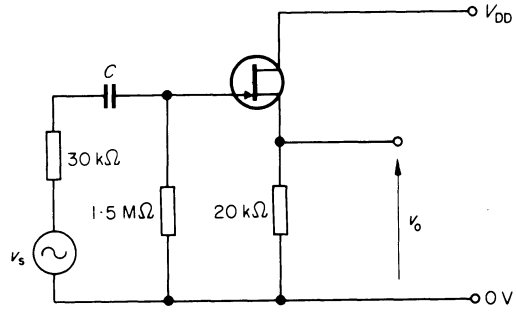


Figure 6.34

(Answer: 0·96)

Exercise 6.10

In a simple common-gate amplifier, the parameters of the FET are g_{fs} = 2 mS, r_{DS} = 100 kΩ, all other parameters being negligible. If the load resistor is 15 kΩ, determine the a.c. input resistance and low-frequency voltage gain of the amplifier.
(Answers: 572 Ω, 26·2)

Exercise 6.11

(a) Sketch the circuit diagram of a single-stage class-A amplifier in which the active device is an FET.

(b) Describe how the operating point will alter with variation in the temperature of the device.

(c) Explain the principle of operation of the particular type of transistor used in your diagram.

(ET4)

7 Negative feedback

7.1 Gain of amplifier with negative feedback

If the gain of an amplifier stage without feedback is represented by A, derive an expression for the gain when a fraction of the output voltage is fed back in opposition to the input.

An amplifier has a gain of 1000 without feedback. Calculate the gain when 0·9 per cent of negative feedback is applied. If, due to ageing, the gain without feedback falls to 800, calculate the percentage reduction in gain (a) without feedback; (b) with feedback. Comment upon the significance of the results of (a) and (b) and state two other advantages of negative feedback.

(ET4)

Figure 7.1 shows the block diagram of voltage feedback in series with the input.

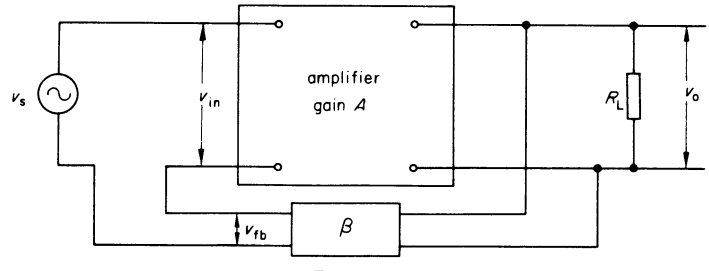


Figure 7.1

Voltage gain A of the amplifier without feedback = v_o/v_s
Voltage gain A' of the amplifier with feedback = v'_o/v_s

When feedback is applied, output voltage $v'_o = Av_{in}$. But for negative feedback

$$v_{in} = v_s - v_{fb}$$

therefore

$$v'_o = Av_s - Av_{fb} \qquad (7.1)$$

Also, feedback voltage

$$v_{fb} = \beta v'_o$$

Substituting in equation 7.1

$$v'_o = Av_s - A\beta v'_o$$

$$A' = v'_o/v_s = \frac{A}{1 + \beta A} \qquad (7.2)$$

Hence, the gain of the amplifier has been reduced by the use of negative feedback.

In equation 7.2, when $\beta = 0{\cdot}009$

$$A' = \frac{1000}{1 + (0{\cdot}009 \times 1000)} = 100$$

(a) Without feedback, percentage reduction in gain is

$$\frac{(1000 - 800)100}{1000} = 20 \text{ per cent}$$

(b) With feedback, new gain

$$A' = \frac{800}{1 + 0{\cdot}009(800)} = 97{\cdot}56$$

therefore percentage reduction in gain with feedback is

$$(100 - 97{\cdot}56) \times 100/100 = 2{\cdot}44 \text{ per cent}$$

Thus, with negative feedback, the percentage reduction in gain is much smaller, and the amplifier is said to be gain-stabilised against the ageing of components and against variations in the supply voltage. The other advantages of negative feedback are

(i) more linear frequency response;
(ii) increase in bandwidth;
(iii) reduction in harmonic, phase, and frequency distortion;
(iv) reduction of any noise produced in the amplifier;
(v) input and output impedance values can be modified to nearly any desired values.

7.2 Effect of negative feedback on amplifier input-impedance

Show that (a) negative feedback in series with the input voltage always increases the input impedance of an amplifier; (b) negative feedback in parallel with the input voltage always reduces the input impedance of an amplifier.

(a) Figure 7.2a shows an amplifier with a feedback voltage $v_{fb} = \beta v_o$ in series with the signal voltage. Without feedback, input impedance

$$Z_{in} = v_s/i_{in}$$

therefore

$$i_{in} = v_s/Z_{in} \qquad (7.3)$$

With negative feedback applied, and with the signal voltage increased to v'_s to maintain the same value of input current i_{in}

$$i_{in} = \frac{v'_s - v_{fb}}{Z_{in}}$$

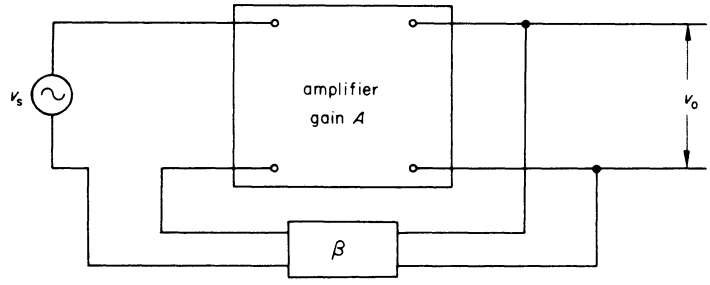


Figure 7.2a

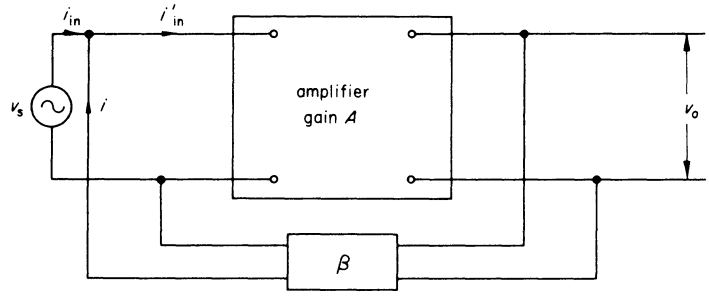


Figure 7.2b

therefore

$$v'_s = i_{in}Z_{in} + v_{fb}$$

With feedback input impedance

$$Z'_{in} = v'_s/i_{in} = Z_{in} + v_{fb}/i_{in}$$

substituting for i_{in} from equation 7.3

$$Z'_{in} = Z_{in} + v_{fb}Z_{in}/v_s$$
$$= Z_{in}(1 + \beta v_o/v_s)$$
$$= Z_{in}(1 + \beta A v_s/v_s)$$
$$= Z_{in}(1 + \beta A)$$

Thus, with negative feedback in series with the input the input impedance is always increased by a factor (1 + βA).

(b) Figure 7.2b shows an amplifier with a feedback voltage $v_{fb} = \beta v_o$ in parallel with the signal voltage. Without feedback

$$i_{in} = v_s/Z_{in}$$

With feedback, input impedance

$$Z'_{in} = v_s/i'_{in} = v_s/(i_{in} + i)$$

where $i = v_{fb}/Z_{in}$.

Substituting this value for i and for i_{in} from equation 7.3

$$Z'_{in} = \frac{v_s}{v_s/Z_{in} + v_{fb}/Z_{in}}$$
$$= Z_{in}v_s/(v_s + \beta A v_s)$$
$$= Z_{in}/(1 + \beta A)$$

Thus, with negative feedback in parallel with the input, the input impedance is always reduced by a factor (1 + βA).

7.3 Effect of negative feedback on amplifier output-impedance

Show that (a) voltage (shunt-derived) negative feedback always decreases the output impedance of an amplifier and that (b) current (series-derived) negative feedback always increases the output impedance of an amplifier.

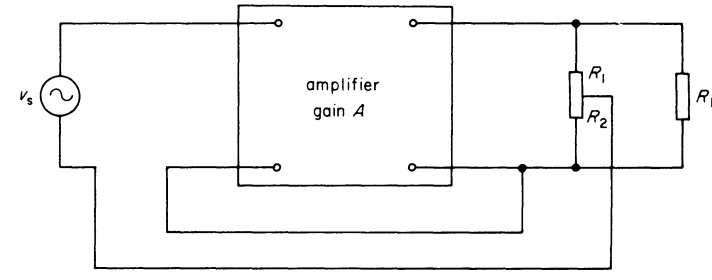


Figure 7.3a

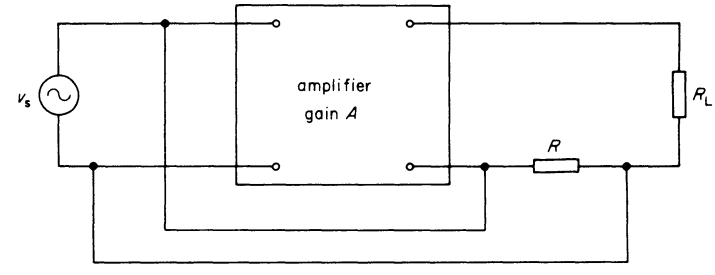


Figure 7.3b

Looking into the amplifier from its output terminals it may be regarded as a voltage generator e in series with its own internal or output impedance Z, as shown in figure 7.4.

In figure 7.4, the open-circuit output voltage is e; the short-circuit output current $i = e/Z$; and the output impedance $Z = e/i$.

(a) Figure 7.3a shows an amplifier using voltage negative feedback. The feedback voltage is usually obtained by connecting a very high-resistive potential-divider chain across load resistor R_L

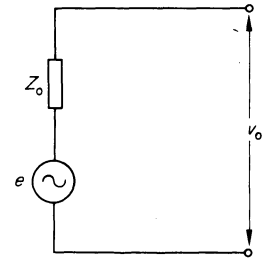


Figure 7.4

The feedback fraction is then $\beta = R_2/(R_1 + R_2)$, neglecting the shunting effect of the potential-divider chain on R_L. The open-circuit and short-circuit conditions for this amplifier are shown in figures 7.5a and 7.5b respectively.

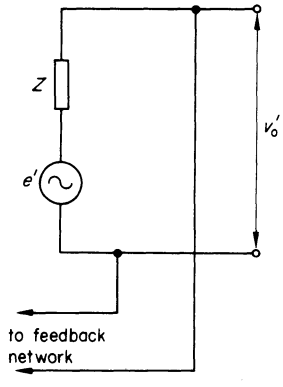


Figure 7.5a

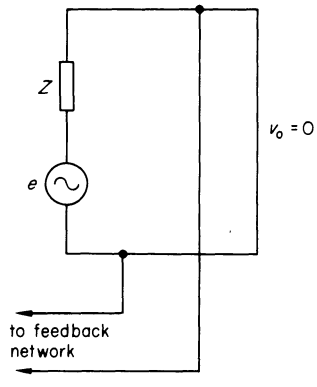


Figure 7.5b

In figure 7.5a, on open-circuit

$$e' = v_o' = Av_s/(1 + \beta A) \qquad (7.4)$$

In figure 7.5b, on short-circuit, there will be no feedback voltage; so that $e' = e = Av_s$, and the short-circuit current

$$i = Av_s/Z \qquad (7.5)$$

Dividing equation 7.5 by equation 7.4 the output impedance with feedback is

$$Z' = e'/i = Z/(1 + \beta A)$$

Thus, with voltage negative-feedback, the output impedance is always reduced by a factor $(1 + \beta A)$.

(b) Figure 7.3b shows an amplifier using current negative feedback. The feedback voltage is usually obtained by connecting a small resistor R in series with the load resistor R_L, and is given by $v_{fb} = i_o R$. The feedback fraction β is given by

$$\beta = \frac{v_{fb}}{v_o} = \frac{i_o R}{i_o(R + R_L)} = \frac{R}{R + R_L}$$

Usually $R \ll R_L$, so that $\beta = R/R_L$. The open-circuit and short-circuit conditions for this amplifier are shown in figures 7.6a and 7.6b respectively.

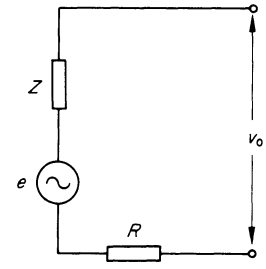


Figure 7.6a

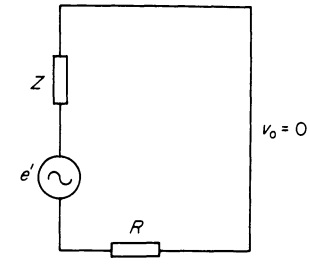


Figure 7.6b

In figure 7.6a, on open-circuit, there will be no feedback. Therefore open-circuit output voltage

$$v = e = Av_s \qquad (7.6)$$

In figure 7.6b, on short-circuit, if $R \ll Z$, then R can be neglected; and short-circuit current is

$$i = e'/Z = Av_s/(1 + \beta A)Z \qquad (7.7)$$

Dividing equation 7.7 by equation 7.6, the output impedance with feedback is

$$Z' = e'/i = (1 + \beta A)Z$$

Thus with current feedback, the output impedance is always increased by a factor $(1 + \beta A)$.

7.4 Shunt-series negative feedback

A negative feedback amplifier is shown in figure 7.7. When the 330 Ω resistor is short-circuited, the magnitude of the voltage gain v_o/v_{in} is 1000. What is the voltage gain when the short-circuit is removed?

If the resistors used in the feedback network each have a tolerance of ±5 per cent, calculate the maximum and minimum values of voltage gain with feedback. (The effects of the input and output impedances of the amplifier may be assumed to be negligible.) State how negative feedback affects the following properties

of the amplifier shown in figure 7.7 (i) harmonic distortion; (ii) bandwidth; (iii) d.c. and a.c. stabilities.

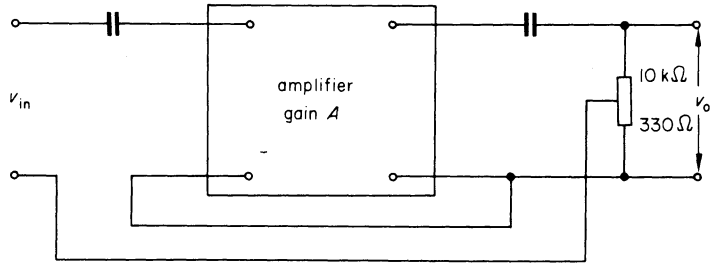


Figure 7.7

(ET4)

With the 330 Ω resistor short-circuited, the voltage gain A = 1000.
With the 330 Ω resistor in circuit, the feedback fraction is

$$\beta = 0{\cdot}33/(10 + 0{\cdot}33) = 0{\cdot}0319$$

Therefore amplifier gain with negative feedback is

$$A' = A/(1 + \beta A) = 1000/(1 + 31{\cdot}9) = 30{\cdot}4$$

If the resistors have tolerance of ±5 per cent, the maximum value of β is obtained when the 330 Ω resistor increases by 5 per cent and the 10 kΩ resistor decreases by 5 per cent; and vice versa for the minimum value of β.
Therefore maximum value of $\beta = 0{\cdot}3465/(9{\cdot}5 + 0{\cdot}3465) = 0{\cdot}0352$
Minimum value of gain with negative feedback, assuming the gain without feedback remains at 1000, is therefore

$$A' = 1000/(1 + 35{\cdot}2) = 27{\cdot}6$$

Similarly, minimum value of β is

$$\beta = 0{\cdot}3135/(10{\cdot}5 + 0{\cdot}3135) = 0{\cdot}029$$

Maximum gain with feedback is

$$A' = 1000/(1 + 29) = 33{\cdot}3$$

Negative feedback will (i) decrease harmonic distortion; (ii) increase the bandwidth; (iii) improve the d.c. and a.c. stabilities.

7.5 Emitter-follower amplifier

Sketch the circuit diagram of either an emitter follower or a cathode follower. Describe how the circuit acts as a matching stage between source and load.

Determine the approximate power gain (in dB*) of an emitter follower having an a.c. input resistance of 50* kΩ *and a load of 500* Ω.

(ET4)

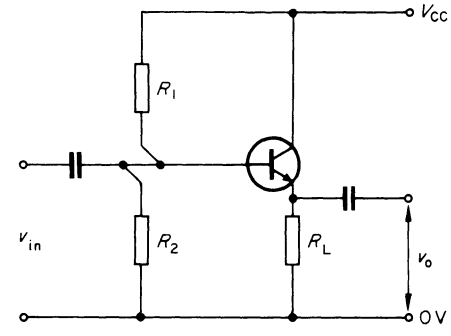


Figure 7.8

Figure 7.8 shows the circuit diagram of an emitter-follower amplifier where the load resistor is in the emitter circuit. The base-emitter voltage of the transistor is very small, and the name emitter follower is therefore derived from the fact that as the base voltage changes sinusoidally the emitter voltage changes in the same manner; that is, it *follows* the base voltage. Note that in this circuit *all* the output voltage is fed back in series opposition, so $v_{be} = v_{in} - v_o$ and the feedback fraction $\beta = 1$; that is, 100 per cent negative feedback is applied. The voltage gain of an emitter follower is

$$A' = A/(1 + A) \approx 1$$

Also, as it is *voltage* negative-feedback, the output impedance is reduced to a very low value; and, as the feedback is in *series* with the input voltage, the input impedance is increased to a very high value. Hence, this amplifier is ideal for matching a stage of high output impedance to one of low input impedance, as it does not shunt the output voltage of the first stage and its own output voltage is not seriously shunted by the low input impedance of the following stage.

Let the input voltage to the emitter follower be v_{in} and let its output voltage be v_o; then

$$\text{Input power } P_{in} = (v_{in})^2/r_{in} = \frac{(v_{in})^2}{50}$$

$$\text{Output power } P_o = (v_o)^2/r_o = \frac{(v_o)^2}{0{\cdot}5}$$

Power gain $A_p = P_o/P_{in} = 10 \log [50(v_o)^2/(v_{in})^2 0{\cdot}5]$

$= 10 \log 100 \quad (\text{as } A_v = 1)$

$= 20$ dB

7.6 Gain stabilisation by negative feedback

Discuss the effects of negative feedback on an amplifier in terms of (a) gain stability; (b) linearity of frequency response; (c) bandwidth.

An amplifier has an open-loop gain of 270 which is found to fall by 10 per cent due to changes in supply voltage. If the gain is to be stabilised so that it falls by only 1 per cent, calculate the amount of negative feedback required. If the original upper 3 dB *frequency was 50* kHz, *calculate its value when this amount of negative feedback is applied. Prove any formulae used.*

(H.N.C.)

(a) The gain of an amplifier with negative feedback is given by $A' = A/(1 + \beta A)$. If $\beta A \gg 1$, $A' = 1/\beta$ from which it is apparent that the gain with feedback is virtually independent of changes in supply voltage, component tolerances, transistor parameters etc. Therefore the gain is stabilised against these changes.

(b) If $\beta A \gg 1$, the frequency response would be flat. Even in practice, the linearity of the response is greatly improved with negative feedback.

(c) The bandwidth is increased with negative feedback, the lower 3-dB frequency f_1 is reduced to $f_1/(1 + \beta A)$ Hz and the upper 3-dB frequency f_2 is increased to $f_2(1 + \beta A)$. Therefore, neglecting the lower 3-dB frequency, the bandwidth is increased by a factor $(1 + \beta A)$.

The gain of the amplifier with negative feedback is

$$A' = A/(1 + \beta A) \tag{7.8}$$

When A falls to $0{\cdot}9A$, A' must fall to only $0{\cdot}99A'$ therefore

$$0{\cdot}99A' = \frac{0{\cdot}9A}{1 + \beta 0{\cdot}9A} \tag{7.9}$$

Dividing equation 7.9 by equation 7.8

$$0{\cdot}99 = \frac{0{\cdot}9(1 + \beta A)}{1 + 0{\cdot}9\beta A}$$

$$0{\cdot}09 = 0{\cdot}9(1 - 0{\cdot}99)\beta A$$

$$\beta A = 10$$

$$\beta = 1/27$$

At high frequencies, the amplifier gain is

$$A = A_o/(1 + jf/f_2)$$

where A_o is the midband gain and f_2 is the upper 3-dB frequency. With negative feedback the gain is

$$A' = A/(1 + \beta A)$$

Substituting for A

$$A' = \frac{A_o}{1 + jf/f_2 + \beta A_o}$$

Dividing through by $(1 + \beta A_o)$

$$A' = \frac{A_o/1 + \beta A_o}{1 + j[f/f_2(1 + \beta A_o)]}$$

$$= \frac{A'_o}{1 + j[f/f_2(1 + \beta A_o)]} \tag{7.10}$$

The new upper 3-dB frequency is defined as the frequency at which

$$|A'| = A'_o/\sqrt{2}$$

Let that frequency be f'_2, then from equation 7.10

$$f'_2/f_2(1 + \beta A_o) = 1$$

$$f'_2 = f_2(1 + \beta A_o)$$

$$= 50(1 + 270/27)$$

$$= 550 \text{ kHz}$$

7.7 Negative feedback in an integrated-circuit amplifier

An extract from the specifications of an integrated-circuit amplifier is as follows

Nominal gain = 86 dB

95 per cent sample range is 80–89 dB

Input impedance 100 kΩ

Frequency response characteristics are shown in figure 7.9.

This amplifier is to be used with voltage negative feedback in series with the input to give a nominal gain of 1000. For the feedback amplifier determine (a) the gain spread of the system; (b) the input impedance of the system; (c) the bandwidth of the system.

(ET5)

(a) Nominal gain of the amplifier without feedback is 86 dB. Therefore

$$20 \log A = 86$$

$$A = 19\,950$$

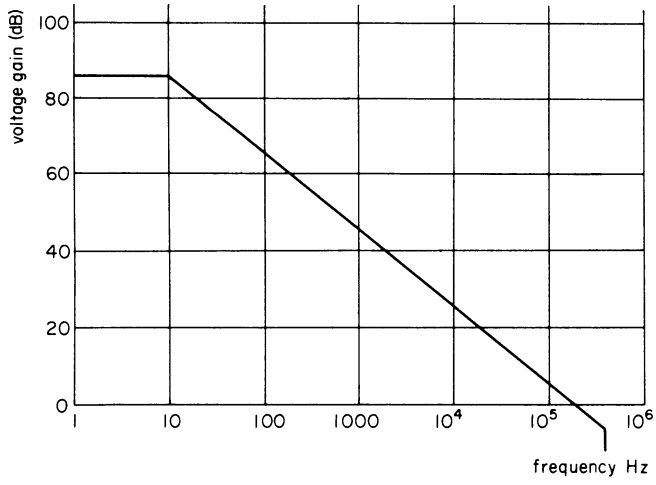


Figure 7.9

With feedback, nominal gain

$$A' = 1000 = 19\,950/(1 + \beta 19\,950)$$

$$1 + \beta 19\,950 = 19{\cdot}95$$

$$= 18{\cdot}95/19\,950 = 9{\cdot}5 \times 10^{-4}$$

Minimum gain A_1 of the amplifier without feedback is 80 dB, therefore

$$20 \log A_1 = 80$$

$$A_1 = 10\,000$$

With feedback, minimum gain

$$A_1' = 10\,000/(1 + 9{\cdot}5) = 952{\cdot}4$$

$$= 59{\cdot}6 \text{ dB}$$

Maximum gain without feedback

$$A_2 = 89 \text{ dB}$$

Therefore

$$20 \log A_2 = 89$$

$$A_2 = 28\,180$$

Then maximum gain of the amplifier with feedback is

$$A_2' = \frac{28\,180}{1 + 26{\cdot}77} = 1015 = 60{\cdot}1 \text{ dB}$$

That is the gain spread is from 59·6 to 60·1 dB.

(b) Input impedance with series negative-feedback is

$$r_{in} = (1 + \beta A) r_{in}$$

$$= (1 + 18{\cdot}95)100$$

$$= 1995 \text{ k}\Omega$$

$$\approx 2 \text{ M}\Omega$$

(c) Neglecting the lower cut-off frequency, the bandwidth is equal to the upper cut-off frequency (that is, the frequency at which the gain is 3 dB down from its midband value). From the graph, without feedback the upper cut-off frequency $f_c \approx 14$ Hz; therefore, with negative feedback the new upper cut-off frequency will be

$$f_c' = f_c(1 + \beta A)$$

$$= 14 \times 19{\cdot}95$$

$$= 279 \text{ Hz}$$

7.8 Instability in feedback amplifier

List the effect of series voltage negative-feedback on the performance of an amplifier.

An amplifier with an open-loop gain of A has a fraction β of its output fed back to the input. With the aid of a diagram develop an expression for the new gain A′ with feedback in terms of the other quantities.

If the open-loop gain is 1000∠70° and the feedback factor is −0·02∠20°, determine the gain of the amplifier with negative feedback. What limiting value and phase of the feedback fraction β would be required to make the amplifier unstable?

(H.N.C.)

The effects of series voltage negative-feedback have already been discussed in previous questions.

In section 7.1 it was shown that the gain of an amplifier with negative feedback was

$$A' = \frac{A}{1 + \beta A} \tag{7.2}$$

It will be shown in section 8.1 that the gain with positive feedback is

$$A' = \frac{A}{1 - \beta A} \tag{7.11}$$

Substituting the given values in equation 7.2

$$A' = \frac{1000\angle 70^\circ}{1 - (1000\angle 70^\circ \times 0{\cdot}02\angle 20^\circ)}$$

$$= \frac{1000\angle 70^\circ}{1 - 20\angle 90^\circ}$$

$$= \frac{1000\angle 70^\circ}{1 - j20}$$

$$= \frac{1000\angle 70^\circ}{20{\cdot}02\ \angle -87{\cdot}1^\circ}$$

$$= 49{\cdot}9\angle -17{\cdot}1^\circ$$

For instability, from equation 7.11

$$\beta A = 1\angle 0^\circ$$

$$\beta = 1/(1000\angle 70^\circ)$$

$$= 0{\cdot}001\angle -70^\circ$$

7.9 Compound negative feedback

Explain clearly the importance of matching when designing a system with serially-connected devices.

An amplifier with an output resistance of 600 Ω has an overall voltage gain of 10 000∠180° when connected to a 600 Ω load. The overall gain is to be reduced to 100 by the simultaneous application of current and voltage feedback in series with the input so that the output impedance remains unaltered. Calculate the necessary current-feedback resistance to be connected in series with the 600 Ω load and the percentage voltage feedback.

(I.E.E.)

The importance of matching has already been discussed in previous questions.

Considering the general expression for the gain of an amplifier with negative feedback

$$A' = \frac{A}{1 + \beta A}$$

substituting the values given

$$100 = \frac{-10\,000}{1 - 10\,000\beta}$$

$$1 - 10\,000\beta = -100$$

$$\beta = 101/10\,000 = 1{\cdot}01 \times 10^{-2}$$

Let the current-feedback factor be β_1 and the voltage-feedback factor be β_2. The output resistance change will then be in the ratio $(1 + \beta_1 A)/(1 + \beta_2 A)$. But, as the output resistance must not change with the application of feedback

$$\beta_1 = \beta_2 = \beta/2 = 5{\cdot}05 \times 10^{-3}$$

Percentage voltage feedback is 0·505 per cent.
Assuming the resistor R in series with the load is small compared with the load

$$\beta_1 = R/600$$

$$R = 5{\cdot}05 \times 10^{-3} \times 600$$

$$= 3{\cdot}03\ \Omega$$

7.10 Exercises

Exercise 7.1

(a) Voltage negative-feedback is applied to an amplifier. Explain how it affects (i) the frequency response; (ii) variation in stage gain due to fluctuating supply voltage.

(b) When voltage feedback is applied to an amplifier of gain 100 the overall stage gain falls to 50. Calculate the fraction of the output voltage fed back. If this fraction is maintained, calculate the value of the amplifier gain required if the overall stage gain is to be 75.

(Answer 0·01, 300) (ET4)

Exercise 7.2

State three reasons why negative feedback may be applied to an amplifier.

An amplifier having a gain of 500 without feedback has overall negative feedback applied which reduces the gain to 100. Calculate the fraction of output voltage fed back. If due to ageing of components, the gain without feedback falls by 20 per cent, calculate the percentage fall in gain with feedback.

(Answers: 0·008, 4·76 per cent) (ET4)

Exercise 7.3

(a) An amplifier having a gain of 100 has 9 per cent voltage negative-feedback applied in series with the input signal. Calculate the overall stage-gain with feedback.

If a supply voltage variation causes the gain with feedback to fall by 10 per cent, determine the percentage change in gain without feedback.

(b) Draw circuit diagrams to show how (i) voltage feedback; (ii) current feedback, may be applied separately to a valve or transistor amplifier. In each case state the effect of feedback on the amplifier output impedance.
(Answers: 10, 52·6 per cent) (ET4)

Exercise 7.4

Explain the conditions which can give rise to oscillation in a multistage amplifier employing overall negative-feedback. A three-stage amplifier has an open loop gain of 5×10^5, input impedance of 100 kΩ and output impedance of 100 Ω. Overall voltage negative-feedback is applied in series with the input to reduce the gain to 10^3. Determine (a) the feedback factor required; (b) the input impedance; (c) the output impedance.
(Answers: $0{\cdot}998 \times 10^{-3}$, 50 MΩ, 0·2 Ω) (ET5)

Exercise 7.5

(a) A video amplifier consists of several common-emitter transistor stages followed by an emitter follower. The overall midband gain is 2000. At a frequency of 3 MHz the overall gain is 20 dB below the midband gain. If 0·02 of the output voltage is fed back as negative feedback in series with the input, calculate the new midband gain and the relative gain at 3 MHz (expressed in dB).

(b) Explain why an emitter follower is used for the final stage.
(Answers: 48·8, 32 dB) (TT5)

Exercise 7.6

An amplifier has a gain of 1000, a bandwidth of 1 MHz, and input and output impedances of 1 kΩ and 20 kΩ respectively. The bandwidth is increased to 50 MHz by the application of voltage negative-feedback in series with the input. Determine the new values of the gain, and of the input and output impedances.
(Answers: 20, 50 kΩ, 400 Ω)

Exercise 7.7

An amplifier of gain A without feedback, has feedback of factor β applied from the output and added to the input. Develop an expression for A', the gain with feedback, in terms of the other quantities.

If the gain without feedback is (800–j100) and the feedback network of $\beta = -1/(40\text{–}j20)$ modifies the output voltage to v_{fb}, which is combined in series with the signal voltage, determine the gain of the amplifier with feedback. List the effects of this type of feedback on the performance of the amplifier.
(Answer: 38·3–j18·3) (H.N.C.)

Exercise 7.8

State the advantages and disadvantages of applying negative feedback to an amplifier.

The amplifier shown in figure 7.10 has a voltage gain of 1500 and internal resistance of 7·5 kΩ measured at the output terminals before the feedback circuit is connected. Comment on the component values used in this feedback circuit. Hence, calculate the gain and output impedance of the feedback amplifier, proving any formulae used.

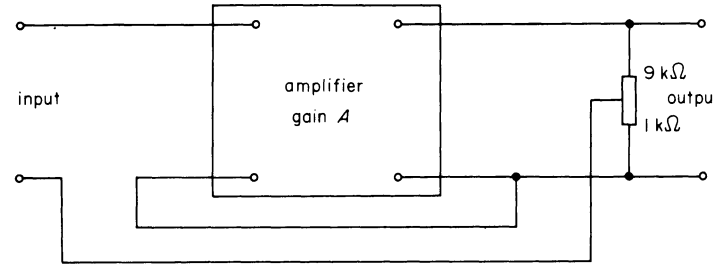


Figure 7.10

(Answers: 9·9, 49·7 Ω) (H.N.C.)

Exercise 7.9

List the effects of feedback on the characteristics of an amplifier. A three-stage transistor amplifier has an overall voltage gain which may be represented by the expression

$$A = \frac{-1000}{(1 - j10^{-5}f)^3}$$

where f is the frequency in Hz. A resistive potential divider feeds back a fraction $\beta = 1/150$ of the output voltage in series with the input. Sketch the polar plot of βA for frequencies between zero and infinity. Show that the amplifier is stable, and calculate the percentage increase in stage gain necessary to introduce instability. Mention all approximations and assumptions made.
(Answer: 20 per cent) (I.E.E.)

Exercise 7.10

A multistage amplifier has a gain tolerance of ±6 dB due to component and transistor tolerances. A fraction of the output voltage is fed back in series with the input so that the overall gain is reduced by 20 dB with respect to its mean value without feedback. Calculate the new tolerance in overall gain in dB.
(Answer: −0·44 to 0·82 dB) (I.E.E.)

8 Transistor oscillators

8.1 Amplifier gain with positive feedback

(a) An amplifier having a voltage gain A without feedback has a fraction β of its output voltage fed back in series with its input. Derive a general expression for the amplifier gain when the feedback loop is closed. Hence, or otherwise, describe the requirements for the maintenance of oscillations when the feedback is positive.

(b) Draw the circuit diagram of a tuned-collector oscillator and explain its principle of operation. How could the feedback fraction be adjusted in a high frequency oscillator of this type?

(ET4)

(a) The expression for the gain of an amplifier using negative feedback was derived in section 7.1. Using positive feedback, the only difference will be that the sign of the feedback voltage will now be positive and it will add to the signal voltage v_s. The analysis used in section 7.1 will result in the expression

$$A' = \frac{A}{1 - \beta A} \tag{8.1}$$

where A' is the gain of the amplifier with positive feedback. Considering equation 8.1, if $\beta A = 1$, the gain with positive feedback becomes infinitely large. In practice, $\beta A = 1$ implies that the loop gain is unity and that zero phase shift occurs around the loop; the feedback voltage is therefore identical to the signal voltage. Thus, even if the signal voltage is zero, there will still be an output voltage; hence, the amplifier becomes an oscillator.

(b) Figure 8.1 shows the circuit diagram of a tuned-collector oscillator (dots indicate points of similar instantaneous polarity).

In this oscillator there is 180° phase shift through the transistor and a further 180° phase shift is introduced by suitable connection of the transformer secondary winding, giving the total phase shift of 360° required for oscillations. The current gain of the transistor h_{fe}, must be high enough to make the loop gain $\beta A = 1$ to sustain oscillations.

The feedback fraction can be altered by using two inductances in series in place of L_1 and feeding back the voltage across only one of them; or, alternatively, by using two capacitors in series for C.

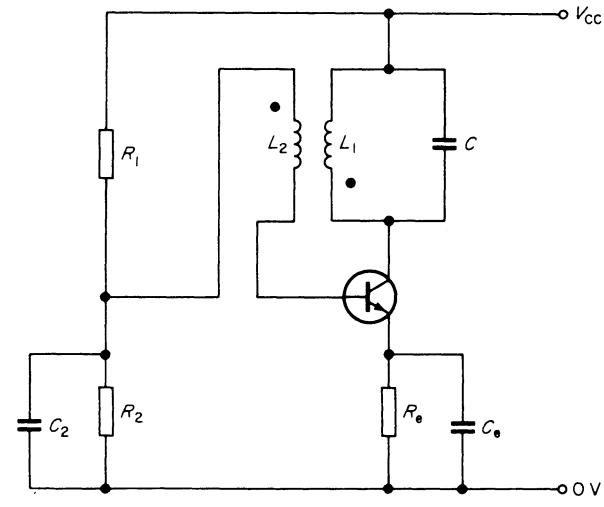


Figure 8.1

8.2 Tuned-collector oscillator

Draw a practical circuit of a transistor tuned-collector oscillator and describe its action.

Draw the equivalent circuit of this oscillator and derive expressions for (i) the minimum gain to maintain oscillation; (ii) the frequency of oscillation.

State carefully any assumptions. (I.E.R.E.)

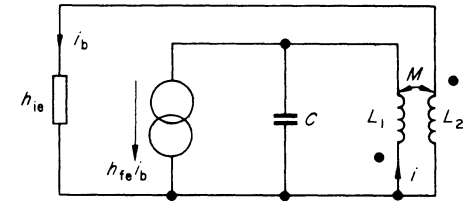


Figure 8.2

The practical circuit of a transistor tuned-collector oscillator is shown in figure 8.1, and its action was described in section 8.1. Figure 8.2 shows the equivalent circuit using h-parameters, but neglecting the effect of the bias components, the voltage generator $h_{re}v_o$, and the transistor output admittance h_{oe}.

Considering the collector circuit

$$(h_{fe}i_b - i)(-j/\omega C) - i(r + j\omega L_1) = -j\omega M i_b$$

therefore

$$i\left(\frac{\mathrm{j}}{\omega C} - \mathrm{j}\omega L_1 - r\right) = i_b\left(-\mathrm{j}\omega M + \mathrm{j}\frac{h_{fe}}{\omega C}\right) \quad (8.2)$$

Considering the input circuit

$$i_b(h_{ie} + \mathrm{j}\omega L_2) = -\mathrm{j}\omega M i \quad (8.3)$$

Dividing equation 8.2 by equation 8.3

$$\frac{\mathrm{j}(1/\omega C - \omega L_1) - r}{-\mathrm{j}\omega M} = \frac{\mathrm{j}(-\omega M + h_{fe}/\omega C)}{h_{ie} + \mathrm{j}\omega L_2}$$

therefore

$$[\mathrm{j}(1/\omega C - \omega L_1) - r]\,[h_{ie} + \mathrm{j}\omega L_2] = \omega M\left(-\omega M + \frac{h_{fe}}{\omega C}\right) \quad (8.4)$$

For oscillations the imaginary part of equation 8.4 must be zero. That is

$$\left(\frac{1}{\omega C} - \omega L_1\right)h_{ie} - \omega L_2 r = 0$$

$$(1 - \omega^2 L_1 C)h_{ie} - \omega^2 L_2 C r = 0$$

$$\omega^2 = \frac{h_{ie}}{L_1 C h_{ie} + L_2 C r} = \frac{1}{L_1 C + L_2 C r/h_{ie}}$$

The frequency of oscillation is given by

$$f = \frac{1}{2\pi(L_1 C + L_2 C r/h_{ie})^{1/2}}$$

If $r \ll h_{ie}$

$$f = \frac{1}{2\pi(L_1 C)^{1/2}}$$

which is the frequency of oscillation of the tuned circuit. Equating the real parts of equation 8.4

$$r h_{ie} + \omega L_2\left(\frac{1}{\omega C} - \omega L_1\right) = \omega M\left(-\omega M + \frac{h_{fe}}{\omega C}\right)$$

$$r h_{ie} C + L_2 - \omega^2 L_1 L_2 C = -\omega^2 M^2 C + h_{fe} M$$

For an iron-cored transformer $M^2 = L_1 L_2$
therefore

$$r h_{ie} C + L_2 = h_{fe} M$$

Minimum value of the transistor current gain is therefore

$$h_{fe} = \frac{r h_{ie} C + L_2}{M}$$

8.3 Colpitts oscillator

The generalised diagram of an oscillator is shown in figure 8.3.

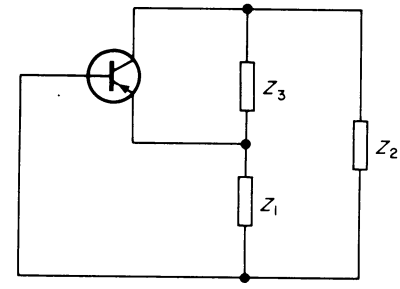


Figure 8.3

If $Z_1 = 1/\mathrm{j}\omega C_1$, $Z_2 = \mathrm{j}\omega L$ and $Z_3 = 1/\mathrm{j}\omega C_2$, show that the condition for oscillations is $|h_{fe}| \geqslant C_2/C_1$ and that the frequency of oscillation is given by

$$f = \frac{1}{2\pi[(1/L)(1/C_1 + 1/C_2)]^{1/2}}$$

The transistor parameters h_{oe} and h_{re} may be neglected. Draw a practical circuit diagram for this oscillator.

(I.E.R.E.)

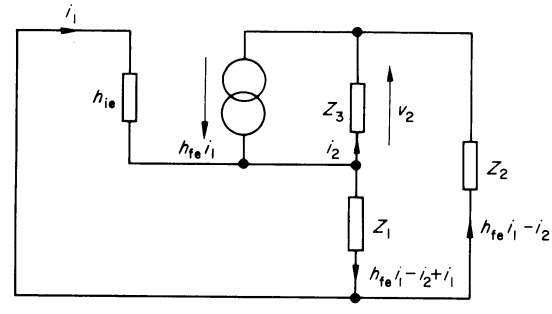


Figure 8.4

Figure 8.4 shows the equivalent circuit of the oscillator of figure 8.3. Considering the input circuit

$$i_1 h_{ie} = -[(h_{fe} + 1)i_1 - i_2]Z_1$$

then

$$i_1[h_{ie} + (h_{fe} + 1)Z_1] = i_2 Z_1 \quad (8.5)$$

Considering the output circuit

$$i_2Z_3 - (h_{fe}i_1 - i_2)Z_2 - [(h_{fe} + 1)i_1 - i_2]Z_1 = 0$$

then

$$i_1[(h_{fe} + 1)Z_1 + h_{fe}Z_2] = i_2(Z_1 + Z_2 + Z_3) \qquad (8.6)$$

Dividing equation 8.6 by equation 8.5

$$\frac{(h_{fe} + 1)Z_1 + h_{fe}Z_2}{h_{ie} + (h_{fe} + 1)Z_1} = 1 + \frac{Z_2}{Z_1} + \frac{Z_3}{Z_1}$$

Dividing numerator and denominator of the left-hand side by Z_1 and substituting for Z_1, Z_2, and Z_3

$$\frac{(h_{fe} + 1) - \omega^2 C_1 L h_{fe}}{j\omega C_1 h_{ie} + (h_{fe} + 1)} = 1 - \omega^2 C_1 L + \frac{C_1}{C_2}$$

$$0 = \omega^2 C_1 L + \frac{(h_{fe} + 1)C_1}{C_2} + j\omega C_1 h_{ie}\left(1 - \omega^2 C_1 L + \frac{C_1}{C_2}\right) \qquad (8.7)$$

For oscillations, the imaginary part of equation 8.7 is zero, therefore

$$1 - \omega^2 C_1 L + \frac{C_1}{C_2} = 0$$

$$\omega^2 = \frac{1}{L}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \qquad (8.8)$$

therefore frequency of oscillation

$$f = \frac{1}{2\pi[(1/L)(1/C_1 + 1/C_2)]^{1/2}}$$

Considering the real part of equation 8.7

$$(h_{fe} + 1)(C_1/C_2) - \omega^2 C_1 L = 0$$

substituting for ω^2 from equation 8.8

$$h_{fe}\frac{C_1}{C_2} + \frac{C_1}{C_2} - 1 - \frac{C_1}{C_2} = 0$$

Then minimum value of current gain

$$h_{fe} = \frac{C_2}{C_1}$$

Figure 8.5 shows the practical circuit diagram of the oscillator of figure 8.3; it is known as a Colpitts oscillator.

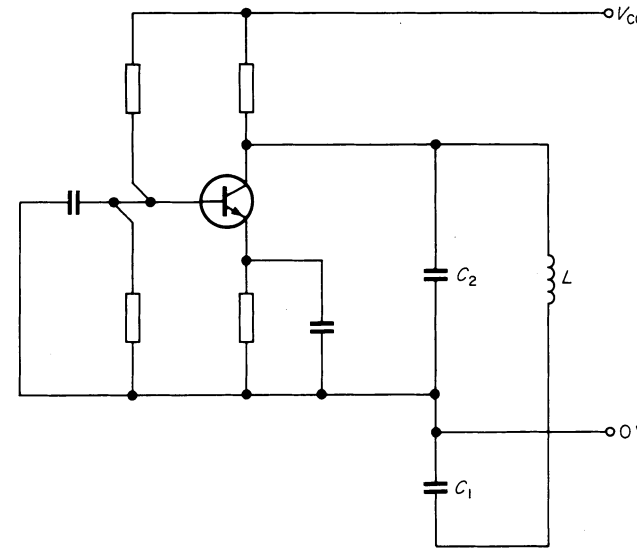


Figure 8.5

8.4 Hartley oscillator

The circuit diagram of a Hartley oscillator is shown in figure 8.6

(a) Explain its principle of operation.

(b) Show how the circuit can be modified to form a Colpitts oscillator.

(c) Upon what factors does the frequency stability of an LC oscillator mainly depend?

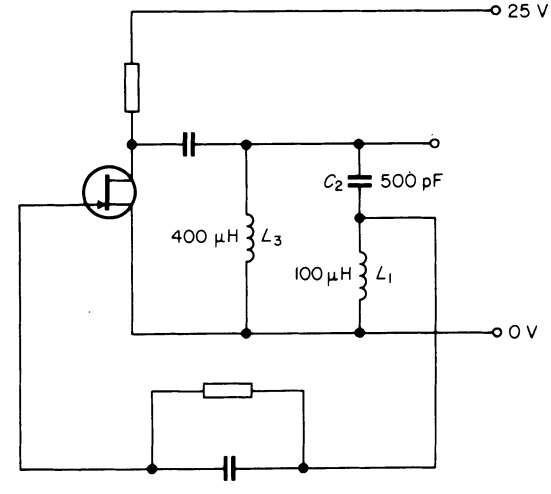


Figure 8.6

(d) For the circuit given, estimate the frequency of oscillation assuming that the coils have no mutual inductance and negligible resistance.

(ET5)

(a) The Hartley oscillator shown in figure 8.6 is based on the general oscillator principle of section 8.3. Z_1 and Z_3 are the inductances of 100 μH and 400 μH respectively, and Z_2 is the 500 pF capacitor. The tuned circuit consists of L_1 and L_3 in series, with C_2 in parallel. There is 180° phase shift between gate and drain and to obtain a loop phase shift of 360°, there must be a further 180° phase shift between the feedback and the output voltages.

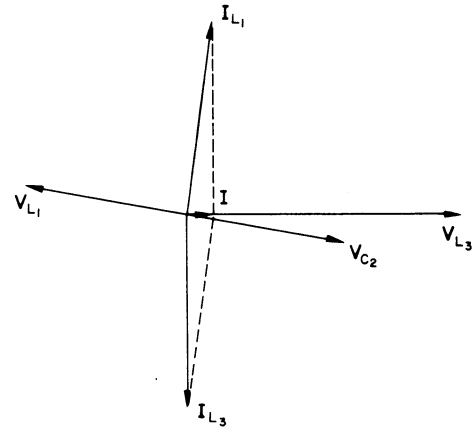


Figure 8.7

Figure 8.7 shows the phasor diagram for the tuned circuit, where **I** is the total current through the circuit at resonance. Therefore as **I** tends to zero, the phase shift between the feedback voltage $\mathbf{V}_{L_1}$ and the output voltage $\mathbf{V}_{L_3}$ tends to 180°. The FET must have a sufficiently high current gain to ensure a loop gain of unity at this frequency.

(b) The circuit could be modified to a Colpitts oscillator by using capacitors for Z_1 and Z_3, and an inductance for Z_2 (as in section 8.3).

(c) The frequency stability of an *LC* oscillator depends upon variations in the parameters of both the transistor and the external circuit. Transistor parameters may vary as a result of changes in operating point, which in turn are caused by changes in the supply voltage or by changes in temperature. The external circuit parameters may vary as a result of changes in load, which in turn are caused by changes in the coils or capacitors of tuned circuits in response to temperature variations, or by changes in effective capacitors that occur when the stray capacitance is affected by the movement of loads or components.

(d) By a similar analysis to that used in section 8.3, it can be shown that the condition for oscillation is

$$1 + \frac{Z_2}{Z_1} + \frac{Z_3}{Z_1} = 0$$

$$1 - \frac{1}{\omega^2 L_1 C} + \frac{L_3}{L_1} = 0$$

$$\omega^2 L_1 C - 1 + \omega^2 L_3 C = 0$$

therefore

$$f = \frac{1}{2\pi[(L_1 + L_3)C]^{1/2}}$$

$$= \frac{1}{2\pi(5 \times 10^{-4} \times 500 \times 10^{-12})^{1/2}}$$

$$= 318 \text{ kHz}$$

8.5 *h*-parameter analysis of common-emitter oscillator

The block diagram of a common-emitter-connected transistor amplifier with feedback is shown in figure 8.8. Show that the circuit will oscillate when the amplifier input is short circuited if

$$0 = (h_{11} + h_{ie})(h_{22} + h_{oe}) - (h_{12} + h_{re})(h_{21} + h_{fe})$$

where h_{11}, h_{12}, h_{22} and h_{21} are the network h-parameters and h_{ie}, h_{re}, h_{oe}, and h_{fe} are the transistor h-parameters.

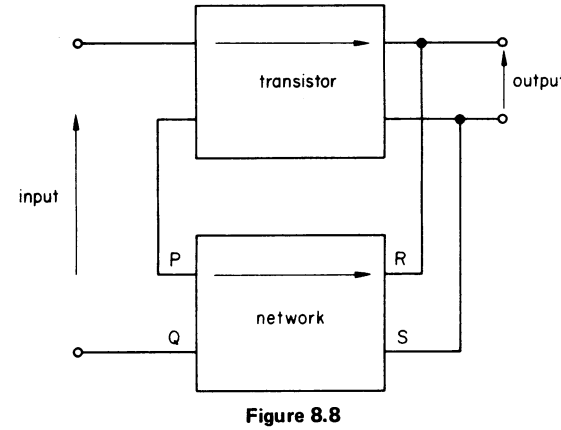


Figure 8.8

For the network shown in figure 8.9, determine the value of h_{fe} required to maintain oscillations and the resulting frequency of oscillation if $h_{11} \gg h_{ie}$, $h_{22} \gg h_{oe}$ and $h_{12} \gg h_{re}$.

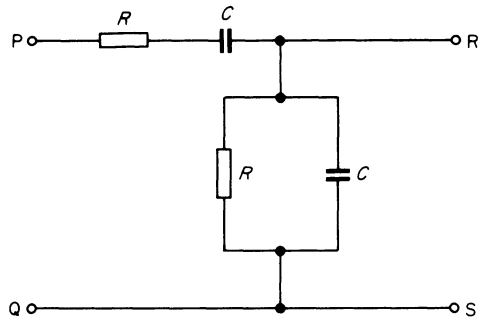


Figure 8.9

(I.E.R.E.)

Figure 8.10 shows the *h*-parameter equivalent circuit for the transistor and network.

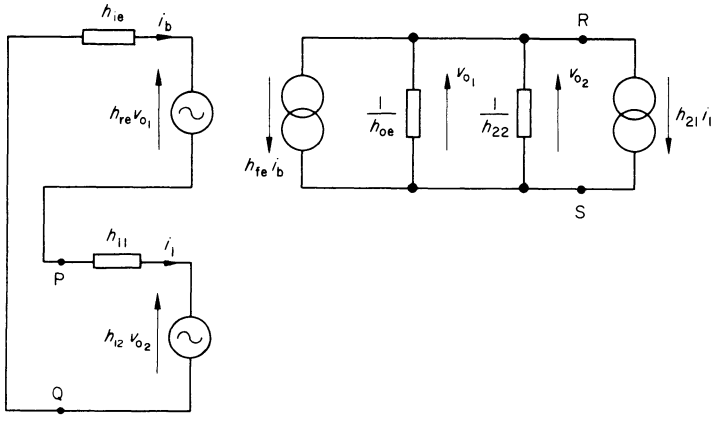


Figure 8.10

From figure 8.10 it can be seen that $i_i = i_b$ and

$$v_{o_1} = v_{o_2} = \frac{-i_1(h_{fe} + h_{21})}{h_{oe} + h_{22}} \qquad (8.9)$$

Considering the input circuit

$$(h_{re} + h_{12})v_{o_1} = -i_1(h_{ie} + h_{11})$$

Substituting for v_{o_1} from equation 8.9

$$-i_1(h_{re} + h_{12})(h_{fe} + h_{21})/(h_{oe} + h_{22}) = -i_1(h_{ie} + h_{11})$$

For oscillations

$$(h_{11} + h_{ie})(h_{22} + h_{oe}) - (h_{12} + h_{re})(h_{21} + h_{fe}) = 0 \qquad (8.10)$$

To determine the *h*-parameters of the network of figure 8.9, first consider the output terminals to be short-circuited. Therefore

$$h_{11} = \frac{v_{in}}{i_{in}} = R + \frac{1}{j\omega C}$$

$$h_{21} = \frac{i_o}{i_{in}} = -1$$

as the input current also flows in the short circuit but in the opposite direction to i_o. Now consider the input terminals to be open-circuited,

$$h_{12} = \frac{v_{in}}{v_o} = 1$$

$$h_{22} = \frac{i_o}{v_o} = \frac{1 + j\omega CR}{R}$$

In equation 8.10, with the conditions given

$$h_{11}h_{22} - h_{12}(h_{21} + h_{fe}) = 0$$

Substituting the values obtained

$$\left(R + \frac{1}{j\omega C}\right)\left(\frac{1 + j\omega CR}{R}\right) - (-1) - h_{fe} = 0$$

then

$$1 - \omega^2C^2R^2 + j2\omega CR + j\omega CR - h_{fe}j\omega CR = 0$$

Therefore, considering imaginary parts, $h_{fe} = 3$. This is the value of current gain required for oscillation; and, considering the real parts, $1 - \omega^2C^2R^2 = 0$. Therefore frequency of oscillation

$$f = \frac{1}{2\pi CR}$$

8.6 Wien-bridge oscillator

Determine expressions for the gain and frequency of operation of a Wien-bridge oscillator employing two similar capacitors C and two similar resistors R in the Wien-bridge network. Taking a basic two-stage, complementary-pair d.c. amplifier, show how this can be modified to obtain a practical Wien-bridge oscillator.

Indicate on your circuit diagram the following feedback paths; those (a) associated with the Wien-bridge network; (b) to control the gain and improve the performance; (c) to stabilise the amplitude of the output; explain the action of this.

Include an output stage which prevents the output load from affecting the operation of the oscillator.

(H.N.C.)

The Wien-bridge network is the one used in section 8.5; however, a general proof will be given in this question.

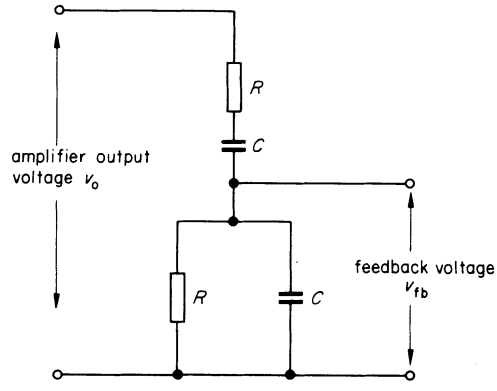


Figure 8.11

It will be assumed in the following proof that (a) there is no phase-shift through the amplifier; (b) the amplifier has a low output impedance, so that the loading effect of the Wien-bridge network is negligible; (c) the amplifier has a high input impedance so that it does not shunt the network.

Considering figure 8.11, the feedback fraction is given by

$$\beta = v_{fb}/v_o = \frac{R/(1 + jXR)}{(1 + jXR)/jX + R/(1 + jXR)}$$

(where $X = \omega C$)

$$= \frac{jXR}{1 - X^2R^2 + j2XR + jXR}$$

$$= \frac{XR}{-j(1 - X^2R^2) + 3XR} \qquad (8.11)$$

For oscillations, as the amplifier phase angle must be zero, there can be no j terms in equation 8.11.
Therefore

$$1 - X^2R^2 = 0$$

$$\omega^2 = \frac{1}{C^2R^2}$$

and

$$f = \frac{1}{2\pi CR}$$

At this frequency, the value of β is obtained from equation 8.11

$$\beta = \frac{XR}{3XR} = \frac{1}{3}$$

Therefore to make the loop gain unity, the amplifier gain A must be 3.

Figure 8.12 shows a basic two-stage complementary-pair d.c. amplifier.

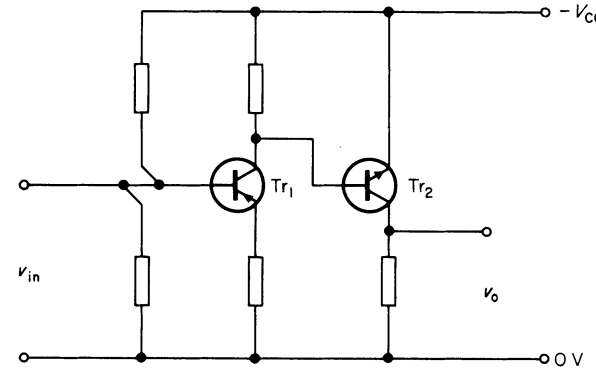


Figure 8.12

Figure 8.13 shows the practical circuit diagram of a Wien-bridge oscillator employing such an amplifier, followed by an emitter-follower stage which provides the low output impedance required.

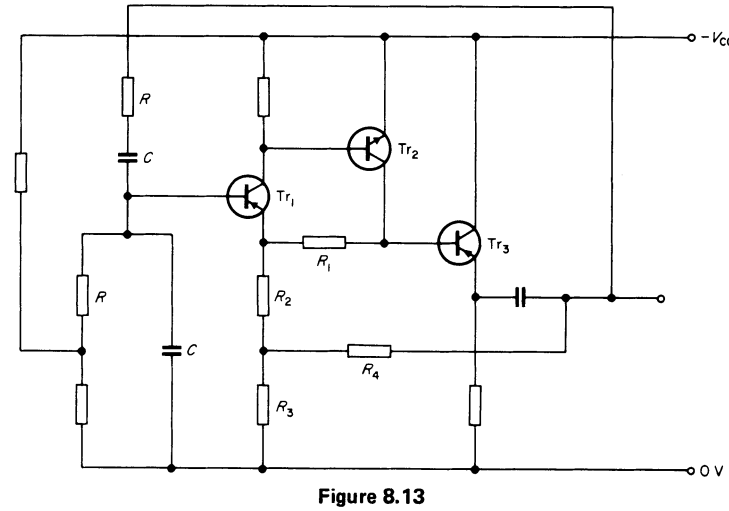


Figure 8.13

As the overall gain is required to be only 3, a considerable degree of negative feedback can be applied by means of R_1, R_2, and R_3, and this provides the high input impedance required. The amplitude of oscillations is stabilised by employing a thermistor R_4 to provide variable negative feedback depending upon the output amplitude; that is, if the amplitude increases with increase in temperature the thermistor resistance decreases, thereby increasing the negative feedback and so decreasing the output voltage. The Wien-bridge provides the positive feedback path; and, by using ganged resistors and ganged capacitors, an audio-frequency oscillator in the range 10 Hz to 100 kHz is easily designed. This type of oscillator is especially suitable for a.f. testing purposes or as a general-purpose laboratory instrument.

8.7 Phase-shift oscillator

State the conditions which must be fulfilled in order that a feedback amplifier shall oscillate. Explain how the type of oscillator shown in figure 8.14 satisfies these conditions. Deduce an expression for the theoretical frequency of oscillation ignoring the input and output impedances of the transistor. If the resistors and capacitors in the frequency-defining network are 6·2 kΩ *and 0·005* μF *respectively, verify that the theoretical frequency is 2·1* kHz. *Explain how and why the RC circuit shown differs from that used in a valve phase-shift oscillator.*

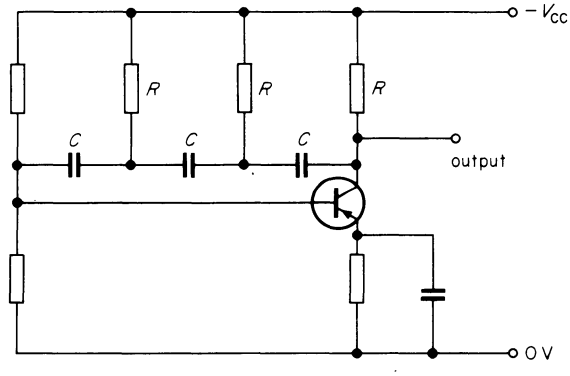


Figure 8.14

(H.N.C.)

For oscillations, the loop gain must be unity: that is $\beta A = 1 \angle 0°$. In this circuit, 180° phase shift occurs through the transistor, and a further 180° phase shift occurs through the three-stage *RC* ladder network. The gain of the amplifier multiplied by the attenuation of the phase-shift network must be at least unity.

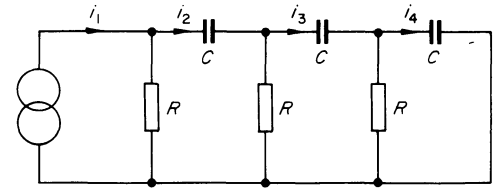


Figure 8.15

Figure 8.15 shows the equivalent circuit of the transistor and feedback network (neglecting the input impedances of the transistor), where i_1 is the signal current in the collector circuit, and i_4 is the signal current in the base circuit.
Therefore

$$i_1R = i_2(2R + jX) - i_3R \tag{8.12}$$

$$i_2R = i_3(2R + jX) - i_4R \tag{8.13}$$

$$i_3R = i_4(R + jX) \tag{8.14}$$

where $X = -1/\omega C$.
Substituting for i_2 from equation 8.13 into equation 8.12

$$i_1R = (2R + jX)^2 i_3/R - (2R + jX)i_4 - i_3R \tag{8.15}$$

Substituting for i_3 from equation 8.14 into equation 8.15

$$i_1R = (2R + jX)^2(R + jX)i_4/R^2 - (2R + jX)i_4 - (R + jX)i_4$$

$$i_1R^3 = (4R^3 - 5X^2R + j8XR^2 - jX^3 - 3R^3 - j2XR^2)i_4$$

$$i_4/i_1 = \frac{R^3}{R^3 - 5RX^2 + j6XR^2 - jX^3} \tag{8.16}$$

For 180° phase shift between i_4 and i_1, the j terms must be zero.
Therefore

$$6XR^2 - X^3 = 0$$

$$X^2 = 6R^2$$

$$\omega^2 = \frac{1}{6C^2R^2}$$

$$f = \frac{1}{2\pi CR\sqrt{6}}$$

$$= \frac{1}{2\pi(5 \times 10^{-9} \times 6{\cdot}2 \times 10^3)\sqrt{6}}$$

$$= 2{\cdot}1 \text{ kHz}$$

Note that at this frequency in equation 8.16

$$\frac{i_4}{i_1} = \frac{R^3}{R^3 - 5RX^2}$$

Substituting $X^2 = 6R^2$

$$\frac{i_4}{i_1} = \frac{R^3}{R^3 - 30R^3} = \frac{-1}{29}$$

Therefore, the current gain of the amplifier must be −29 to give the loop gain of unity that is required for oscillations.

The *RC* network in this amplifier is a current-transfer network; that is, it must be driven from a high-impedance output source, and must feed into a low-impedance load. The common-emitter amplifier satisfies both of these conditions.

Conversely, the equivalent valve circuit would use a voltage-transfer network, would require a low impedance source, and would have the high impedance load usually found in valve circuits.

8.8 Astable multivibrator

An astable multivibrator uses two pnp transistors in the common-emitter connection with 2 kΩ collector loads, base resistors R_B, 0·05 μF coupling capacitors and a −10 V supply. Draw a circuit diagram of this multivibrator and with the aid of sketches of collector and base waveforms, explain its operation.

Calculate the approximate value of R_B if the collector output is to be a 400 Hz square wave. Prove any formulae used and state any assumptions made. (H.N.C.)

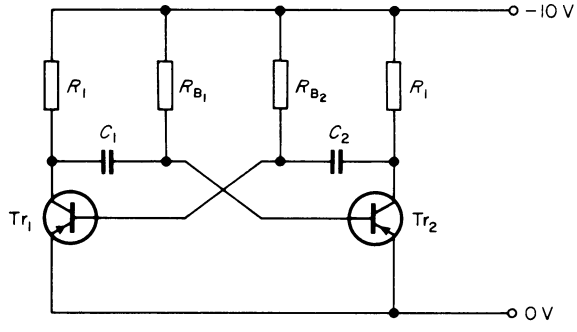


Figure 8.16

The circuit diagram of the astable multivibrator is shown in figure 8.16 and its associated waveforms in figure 8.17. The astable multivibrator is probably the most common type of relaxation oscillator: that is, one which does not have a sinusoidal output. Note that the circuit is basically a two-stage *RC*-coupled amplifier with its output connected back to its input; hence, the 360° phase shift required for oscillation is achieved. Its operation is best explained by reference to the waveforms in figure 8.17.

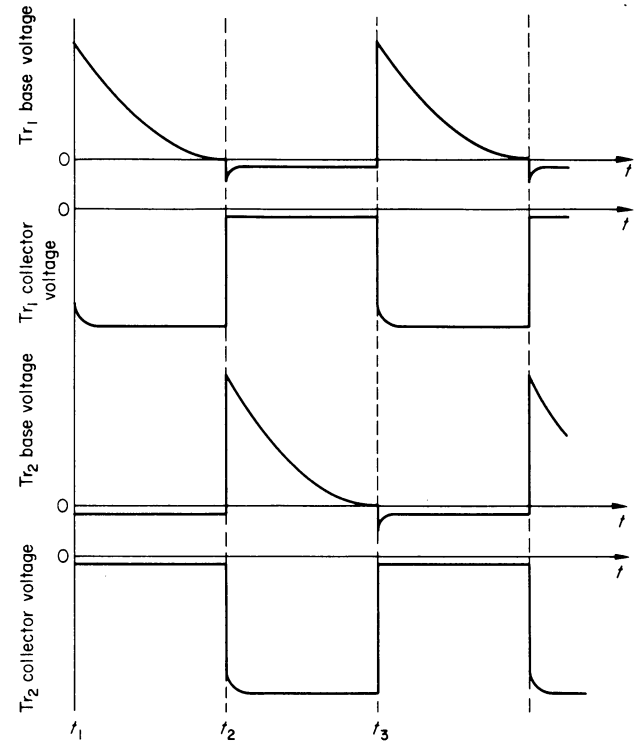


Figure 8.17

At time t_1, Tr_1 is cut off by a positive signal on its base and its collector potential falls to −10 V (neglecting I'_{CO}). At the same time the base potential of Tr_2 is sufficiently negative to saturate it, and its collector potential is approximately zero (neglecting $V_{CE(sat)}$). Tr_2 is now in a stable state but Tr_1 is not, because its base potential is changing negatively as C_2 discharges through R_{B_2}.

At time t_2, Tr_1 base potential is sufficiently negative for Tr_1 to conduct, thus its collector potential changes positively. As the voltage across a capacitor cannot change instantaneously, this positive change is transferred by C_1 without loss in amplitude to the base of Tr_2, cutting off Tr_2. This in turn causes the collector potential of Tr_2 to go to approximately −10 V thereby accelerating the onset of conduction in Tr_1. The process is regenerative, Tr_1 becoming saturated at t_2 and Tr_2 being cut-off.

During time t_2 to t_3, the circuit is governed by C_1 discharging through R_{B_1} until the base potential of Tr_2 is sufficiently negative

for Tr_2 to conduct. The regenerative action this time results in Tr_2 becoming saturated and Tr_1 cut off. The whole cycle then repeats itself continuously.

To determine the frequency of operation, it is necessary to determine the time for which each transistor is cut off. For this analysis, it will be assumed that $V_{BE(on)} = V_{CE(sat)} = 0$ V and also that $I'_{co} = 0$. Consider that at time t_2 a positive charge of 10 V at Tr_1 collector has been transferred instantaneously to Tr_2 base. The circuit conditions existing at this time are shown in figure 8.18.

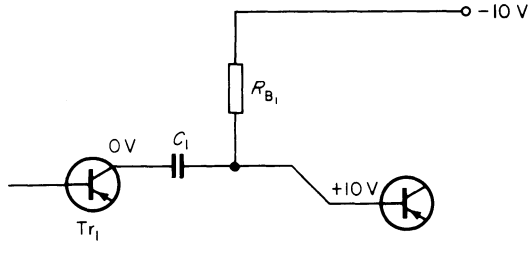


Figure 8.18

C_1 will now start to discharge from +10 V towards −10 V through R_{B_1}. Note however that when the potential on Tr_2 base falls to zero Tr_2 will switch on again.

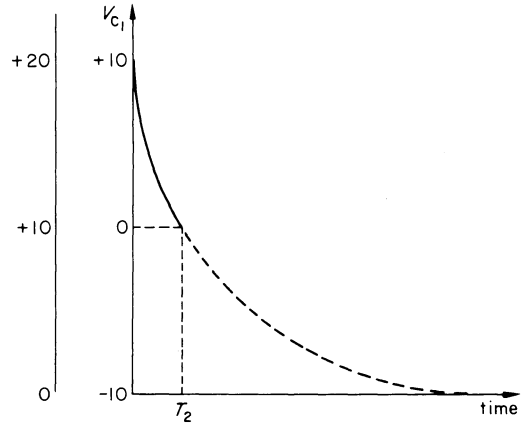


Figure 8.19

The discharge curve is shown in figure 8.19. Its analysis is simplified if a false zero is used; that is, for this particular graph, all potentials are increased by 10 V. Then the time T_2, for which Tr_2 is cut-off, is given by

$$10 = 20 \exp(-T_2/C_1R_{B_1})$$

$$2 = \exp(T_2/C_1R_{B_1})$$

$$T_2 = C_1R_{B_1} \log_e 2 = 0{\cdot}69C_1R_{B_1}$$

Similarly, the time Tr_1 is cut-off is given by

$$T_1 = 0{\cdot}69C_2R_{B_2}$$

Therefore periodic time of waveform $T = T_1 + T_2$ and frequency of waveform

$$f = \frac{1}{0{\cdot}69(C_1R_{B_1} + C_2R_{B_2})}$$

For a square wave $T_1 = T_2$; therefore, if equal capacitors are used, the base resistors must also be equal.

Using the values given in the question

$$400 = \frac{1}{0{\cdot}69 \times 2 \times 5 \times 10^{-8}R_B}$$

therefore

$$R_B \approx 36\ \text{k}\Omega$$

The ratio of T_1 to T_2 is known as the *mark-space ratio* and can be varied by changing the values of one capacitor or resistor. Note that with a very high mark-space ratio, the collector waveform would then be ideal for producing the trigger pulses required for the gate of a thyristor.

8.9 Astable multivibrator with separate base and collector supply-voltages

Explain, with the aid of time-related waveform diagrams, the operation of the oscillator in figure 8.20. Determine either (a) graphically or (b) from first principles, the frequency of oscillation.

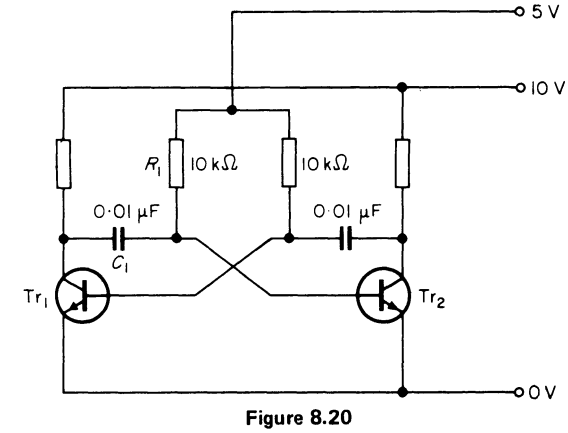


Figure 8.20

(ET5)

The explanation of the astable multivibrator has been given in section 8.8.

However, in figure 8.20, the base resistors have been taken to a separate supply. To determine the frequency of oscillation, consider the circuit conditions when Tr_2 has just been cut off, as shown in figure 8.21.

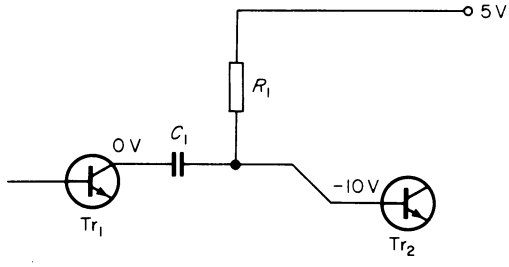


Figure 8.21

C_1 will be discharging from −10 V to 5 V with Tr_2 switching on again when its base potential reaches zero, so the discharge curve will be as shown in figure 8.22.

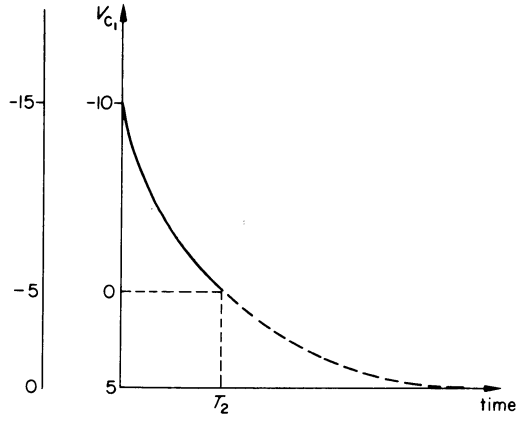


Figure 8.22

Again using a false zero on the graph, the time T_2 for which Tr_2 is cut-off is given by

$$-5 = -15 \exp(-T_2/C_1R_1)$$

$$3 = \exp(T_2/C_1R_1)$$

$$T_2 = C_1R_1 \log_e 3 \approx 1{\cdot}1 \times 10^{-8} \times 10^4$$

$$= 0{\cdot}11 \text{ ms}$$

As the circuit uses equal capacitors and equal resistors, periodic time T = 0·22 ms, and frequency of oscillation = 1/0·22 = 4·54 kHz. This problem illustrates another method of varying the multivibrator frequency; that is, by varying the supply voltage to the base resistors.

8.10 Blocking oscillator

Describe in detail the action of a simple transistor blocking oscillator and draw a circuit diagram. From the circuit diagram derive an expression for the time during which the transistor is turned off.

(I.E.R.E.)

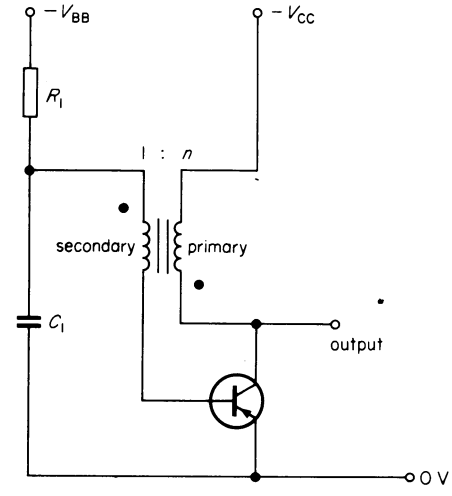


Figure 8.23

Figure 8.23 shows the circuit diagram of a simple transistor blocking oscillator. In this circuit, the transistor provides 180° phase shift and the transformer is connected to give a further 180° phase shift, the dots indicating the points of similar instantaneous polarity. The base is biased negatively by $-V_{BB}$ through R_1 so that the circuit will always revert to the state in which the transistor is conductive.

As soon as the transistor conducts, positive feedback causes oscillation at the resonant frequency of the primary winding. The amplitude of the oscillation builds up quickly, and the capacitor C_1 is quickly charged by the base current of the transistor to a positive voltage which cuts off the transistor. After this, C_1 will discharge through R_1 towards the negative supply $-V_{BB}$. As soon

as the voltage across C_1 has fallen to zero and is just going negative however, the transistor conducts again, and the whole cycle repeats itself continuously.

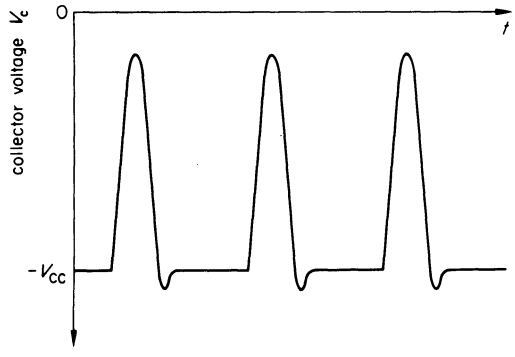


Figure 8.24

Figure 8.24 shows a sketch of the output waveform, provided that the pulse of collector current is large enough to bring the collector-emitter voltage down nearly to zero. The output pulses will be approximately rectangular and suitable, for example, for the trigger pulses required at the gate input of a thyristor.

To determine the off-time of the transistor, note that when the transistor switches on, the change in voltage across the primary is approximately V_{CC}; hence, the corresponding change across the secondary is V_{CC}/n and C_1 therefore charges to V_{CC}/n.

Figure 8.25 shows the discharge curve of C_1 through R_1. If the initial part of the exponential curve is assumed to be linear, it will

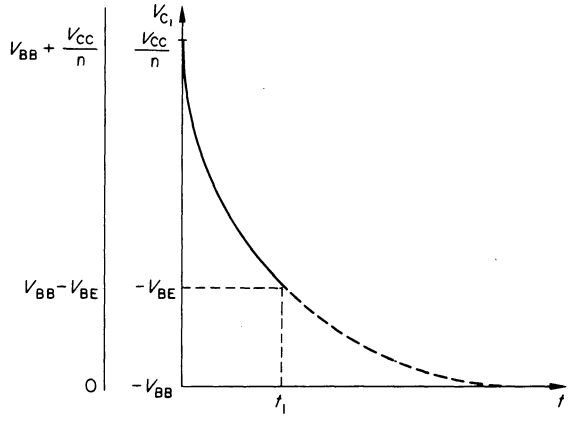


Figure 8.25

have a slope of V/R_1C_1 where V is the initial voltage across the capacitor. Thus, the fall in voltage in a time t is given by

$$\frac{[(V_{CC}/n) + V_{BB}]\,t}{R_1C_1}$$

Therefore, the time t_1 for which the transistor is off is derived from

$$(V_{CC}/n) + V_{BE} = \frac{[(V_{CC}/n) + V_{BB}]\,t}{R_1C_1}$$

therefore

$$t_1 = \frac{R_1C_1(1 + nV_{BE}/V_{CC})}{1 + nV_{BB}/V_{CC}}$$

Note that if $(V_{CC}/n) \gg V_{BE}$ and $V_{BB} = V_{CC}$, then

$$t_1 = \frac{R_1C_1}{1 + n}$$

If the collector-current pulse-width is small compared with t_1, then the frequency of oscillation f is approximately given by

$$f = (1 + n)/R_1C_1$$

Hence the frequency can be controlled by R_1 or C_1; though the method most often used is to vary the base supply voltage V_{BB}.

The collector-current pulse depends upon the resonant frequency of the primary winding: for example, if this resonates at 40 kHz, periodic time $T = 1/(40 \times 10^3) = 25\ \mu s$, and the pulse width is therefore approximately 12·5 μS. If a wider pulse-width is required, a capacitor can be connected across the primary to give the desired value.

In a practical circuit, a diode in series with a small resistor is usually connected across the transformer primary in order to eliminate the large overshoot that would otherwise occur across the primary winding when the collector current is cut off, as such overshoots can exceed the rated collector-emitter voltage of the transistor.

8.11 Exercises

Exercise 8.1

(a) What are the two essential conditions required for oscillation?

(b) With reference to figure 8.26 (i) name the type of circuit; (ii) give the purpose of C_1R_1; (iii) calculate the frequency of opera-

tion; (iv) redraw the circuit for crystal-controlled operation, and explain why crystals may be used in oscillators.
(Answer: 3·18 MHz) (ET3)

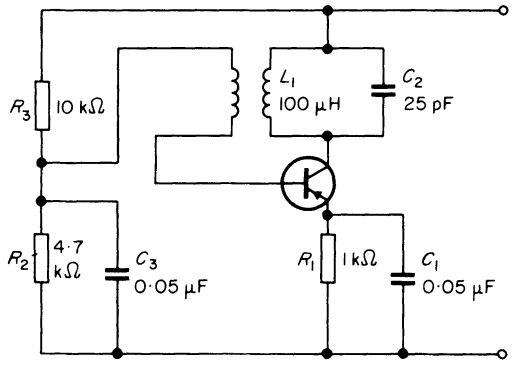


Figure 8.26

Exercise 8.2

Figure 8.27 shows the essential features of an LC oscillator in which the frequency is mainly determined by the series combination of L_o and C_o. Explain the operation of the circuit and discuss its relative merits compared with oscillators using parallel resonance of L_o and C_o.

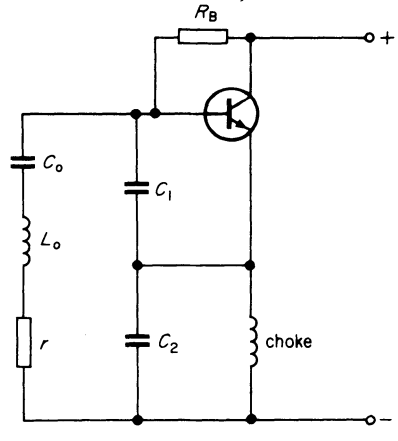


Figure 8.27

In this circuit C_o = 100 pF, L_o = 200 μH, r = 20 Ω, $C_1 = 10^4$ pF, and the only other significant factors are the transistor common-emitter parameters h_{ie} and h_{fe}, where h_{ie} = 1 kΩ. Find the minimum value of h_{fe} for sustained oscillations. Determine the percentage difference between the angular frequency of oscillation and that given by

$$\omega = \frac{1}{(L_o C_o)^{1/2}}$$

(Answers: 103, 1 per cent) (I.E.R.E.)

Exercise 8.3

Sketch a typical circuit diagram for a Hartley-type oscillator using a transistor. Explain the operation of the circuit stating quite clearly the purpose of each component of the circuit.

(TT5)

Exercise 8.4

Define the terms class-A, class-B and class-C as applied to amplifiers. Explain how these terms may be interpreted in relation to the behaviour of oscillators, and mention briefly the features of each class.

Derive an expression for the frequency of oscillation of the oscillator shown in figure 8.28. Show that oscillations will be maintained if the current gain of the amplifying stage is $(C_1 + C_2)/C_1$.

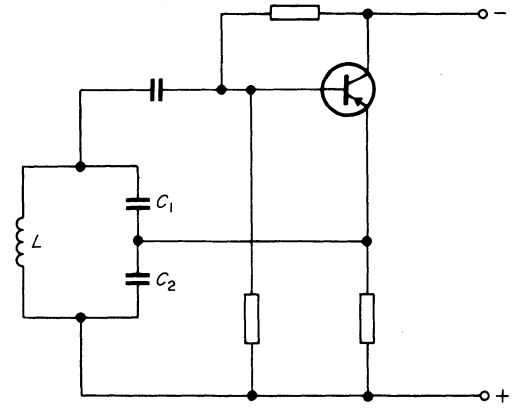


Figure 8.28

(I.E.E.)

Exercise 8.5

(a) Two four-terminal networks are connected as shown in 8.29a. Show that the condition for maintenance of oscillation is

$(h_{ie} + h_{11})(h_{oe} + h_{22}) = (h_{re} - h_{12})(h_{fe} - h_{21})$, where h_{ie}, etc. are the h-parameters of a transistor in common-emitter mode, and h_{11}, etc. are the network h-parameters.

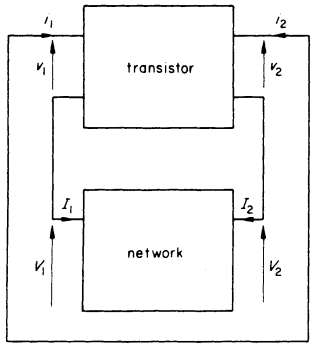


Figure 8.29a

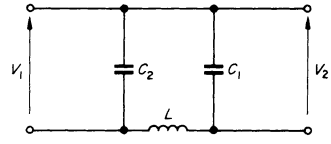


Figure 8.29b

(b) Determine expressions for the frequency of oscillation and the gain required just to maintain oscillation for the network shown in figure 8.29b. It may be assumed that h_{oe} and h_{re} are very small.

$$\left(\text{Answers: } f = \frac{1}{2\pi[LC_1C_2/(C_1 + C_2)]^{1/2}}, \quad h_{fe} = \frac{C_1}{C_2} \right)$$

(I.E.R.E.)

Exercise 8.6

Draw a circuit diagram of a Wien-Bridge oscillator which uses either valves or transistors. Show how frequency and amplitude control may be obtained.

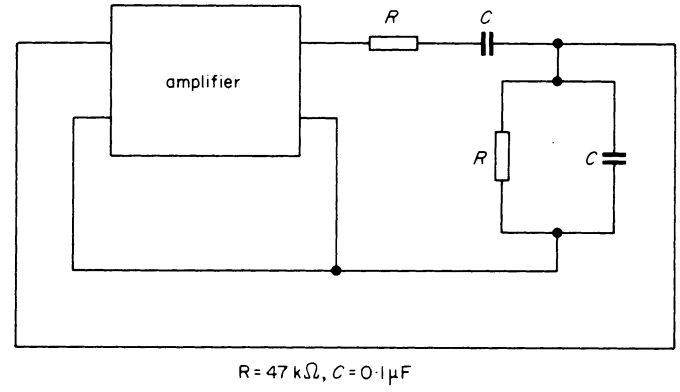
Explain the operation of the circuit and state the formula for the frequency of oscillation in terms of circuit components. Give reasons for any difference between the actual and theoretical frequency of oscillation.

State a typical frequency range over which this oscillator may be used.

(ET4)

Exercise 8.7

What components may be used as frequency-determining elements in an oscillator? Mention electro-mechanical components as well as purely electrical ones. Why are *RC* oscillators popular for laboratory generators of audio frequencies?



R = 47 kΩ, C = 0·1 μF

Figure 8.30

In figure 8.30, it may be assumed that the amplifier input resistance is very high and that its output resistance is very low. The criterion for oscillation is a loop gain of $1 \angle 0$. Calculate the values of m, and the frequency of oscillation if the amplifier gain is (a) $m \angle 0$ and (b) $m \angle 1{\cdot}5°$.

(Answers: 3, 33·9 Hz, 3·002, 32·5 Hz) (I.E.E.)

Exercise 8.8

Describe, with the aid of a circuit diagram, the principles of operation of a phase-advance, phase-shift oscillator. What controls (i) the frequency, and (ii) the amplitude of the oscillations?

State why the amplifier must have a certain minimum gain in order to sustain oscillations. Explain the effect on the output waveform if the open loop gain of the amplifier is appreciably greater than this minimum value. (ET4)

Exercise 8.9

Draw the basic circuit diagram of a single transistor phase-shift oscillator using capacitors and three resistors in the phase-shifting circuit. State the minimum gain necessary for its operation, and the expression for frequency in terms of the component values of the phase-shifting circuit.

If one of the resistors is used to give a current of 100 μA to the base, for a 6 V supply, determine the frequency of operation if the capacitors each have a value of 0·01 μF. Suggest a modification that can be made to limit the amplitude of oscillations and explain its operation. Why is it desirable to limit the amplitude of oscillations?

(Answers: −29, 108·2 Hz) (H.N.C.)

Exercise 8.10

Describe, with the aid of waveform sketches, the action of the multivibrator circuit shown in figure 8.31.

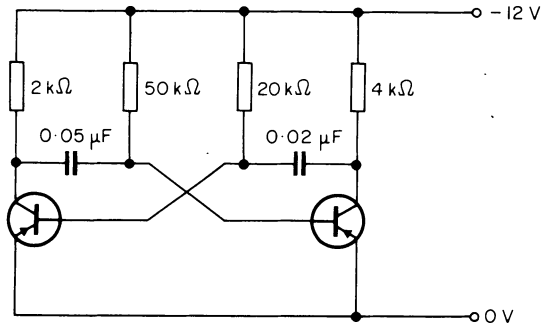


Figure 8.31

Derive a general expression for the cut-off period of one of the transistors. Calculate this time duration for each transistor using the values shown in figure 8.31.

If a high mark-space ratio (say 20:1) is required, describe briefly an alternative circuit arrangement giving reasons for your choice.
(Answers: 1·73 ms, 0·28 ms) (I.E.R.E.)

Exercise 8.11

A multivibrator has two *pnp* transistors with 1 kΩ load resistors and a 10 V supply. The coupling capacitors are each 0·5 μF, and the bases are connected through 100 kΩ resistors (a) to the negative supply line and (b) to a subsidiary line at a potential of −15 V with respect to the emitters. Derive an expression for the frequency of oscillation and evaluate this expression for each of the two conditions.

Draw a circuit to produce positive pulses of 1 ms duration and 5 V amplitude using the multivibrator to determine the repetition frequency.
(Answers: 14·5 Hz, 19·5 Hz) (I.E.E.)

Exercise 8.12

A free-running multivibrator uses two *pnp* silicon transistors in the common-emitter configuration. The collector load resistors each have a resistance of 1 kΩ and the resistors connected between the bases and the collector supply line have a resistance of 22 kΩ.

Draw the circuit diagram and determine from first principles the approximate values of the coupling capacitors, if the oscillation frequency is 250 Hz and the output waveform has a mark-space ratio of 4:1. State any assumptions made.

Draw a circuit for an emitter-coupled multivibrator. Compare the characteristics of the two circuits.
(Answers: 0·05 μF, 0·21 μF) (I.E.E.)

Exercise 8.13

Describe, with the aid of a suitable diagram, the operation of a transistor blocking oscillator, and derive an expression for the natural frequency of operation, stating any assumptions made.

Design a blocking oscillator which has a frequency of 40 kHz with a peak collector current of 8 mA. The transistor has a current gain h_{fe} of 40, and the transformer has a turns ratio of 5:1, the supply voltage of 12 V being common to both base and collector. Find also the new frequency of oscillation if the supply to the base is reduced to 8 V.
(Answers: R = 60 kΩ, C = 2500 pF, 28·9 kHz) (H.N.C.)

9 Wave-shaping and computing circuits

9.1 Differentiating and integrating circuits

The following waveforms are applied in turn to each of the circuits shown in figures 9.1 and 9.2

(a) a symmetrical squarewave of frequency 1 kHz *and amplitude ±10* V.

(b) a sinusoidal voltage of 10 V *peak and frequency 1* kHz.

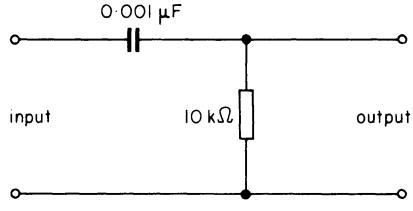


Figure 9.1

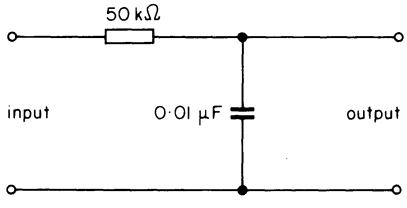


Figure 9.2

For each condition, sketch on the same time-scale two cycles of the input and output waveforms. State which circuit may be used as (i) an integrator and (ii) a differentiator.

Show on the same time-scale the input and output waveforms when the waveform shown in figure 9.3 is applied to the circuit shown in figure 9.2.

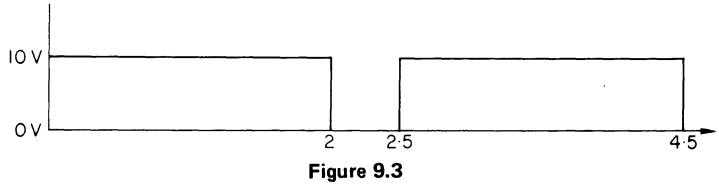


Figure 9.3

(ET5)

Figure 9.1 is a *differentiator*: that is, it produces an output voltage proportional to the slope of the input voltage. This circuit is nearly ideal, as its time constant (10 μs) is very small compared with the periodic time of the input waveform (1 ms). Figure 9.4b shows the output from the circuit; the ideal waveform would be two infinite spikes of zero width. Similarly, figure 9.2 is the *integrator*, and this should produce an output proportional to the area under

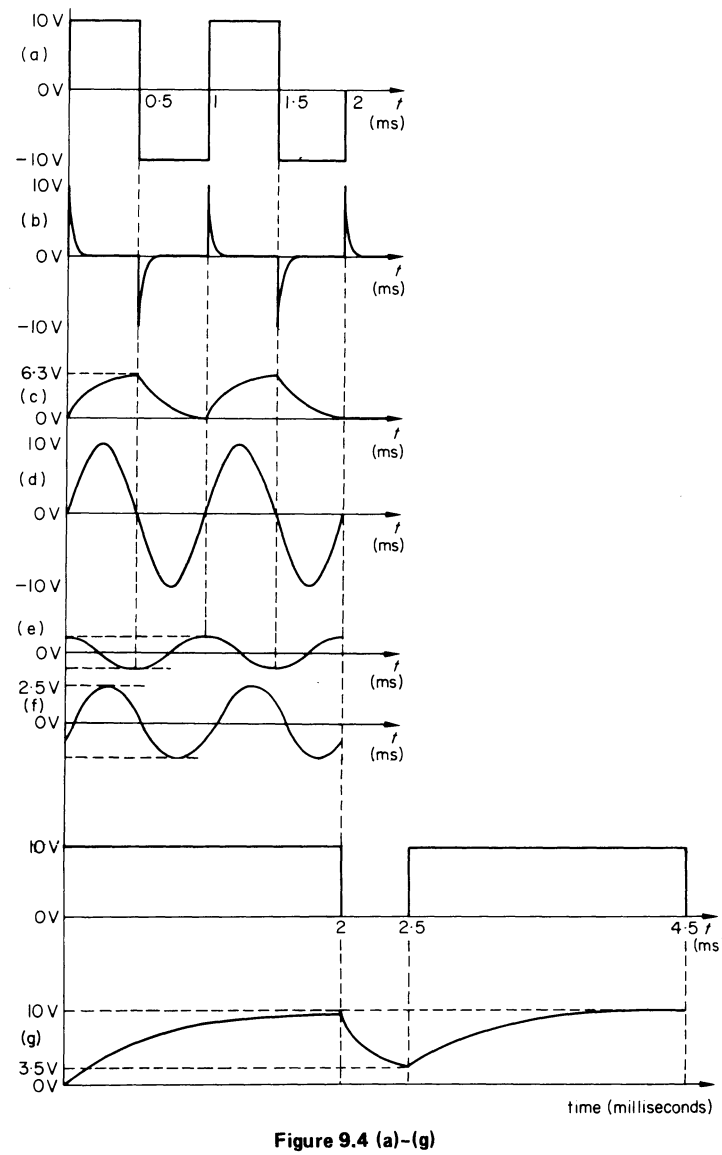


Figure 9.4 (a)–(g)

the input-voltage waveform, that is, a sawtooth wave from the square wave of figure 9.4a. However, the actual output waveform is shown in figure 9.4c, and it can be seen that this is not the ideal sawtooth waveform; this is because the time constant (0·5 ms) of the integrator circuit and the time of the input pulse are only equal. If a more accurate sawtooth output is required, then the time constant should be approximately ten times this value.

When the sine wave of figure 9.4d is applied to the circuit of figure 9.1, the output waveform is as shown in figure 9.4e. Note that as the reactance of the capacitor is about sixteen times the resistor value, the output amplitude is only about 0·59 V, and it will lead the input by approximately 90°. Similarly, when the sine wave of figure 9.4d is applied to the integrator of figure 9.2 as the capacitive reactance is only about one third that of the resistor value, the output amplitude is about 2·5 V and it lags the input by approximately 71° (see figure 9.4f).

When the waveform of figure 9.3 is applied to the circuit of figure 9.2, the output waveform is as shown in figure 9.4g. After the first pulse of 2 ms width, the capacitor will be charged to approximately 9·8 V; during the next 0·5 ms it will discharge to about 3·5 V; and during the second 2 ms will charge again to nearly 10 V.

9.2 Graphical analysis of *RC* circuits

What is meant by the time constant of an RC circuit?

A 0·1 μF *capacitor is charged to a potential difference of 200* V *and then discharged through a resistor of 100* kΩ. *Obtain by graphical construction a curve representing the current during the first 100* ms *of discharge and determine the time taken for the capacitor to discharge to 100* V.

If the resistor and capacitor were to be used as (a) a differentiating circuit; (b) an integrating circuit, comment on a suitable input frequency in each case.

(ET5)

The instantaneous voltage v_c across a capacitor C when it is discharging through a resistor R is

$$v_c = V \exp(-t/RC) \qquad (9.1)$$

where V is the voltage across the capacitor when $t = 0$

R is the resistor value in ohms

C is the capacitor value in farads

When $t = RC$ seconds, the index of the exponential function becomes −1. Therefore

$$v_c = V \exp(-1)$$
$$= 0{\cdot}368\ V$$

Therefore, the voltage across the capacitor has fallen to 36·8 per cent of its initial value (or has lost 63·2 per cent of its initial voltage). Similarly, for a capacitor charging through a resistor, RC is the time taken to reach 63·2 per cent of its final voltage. RC is therefore known as the *time-constant* of the circuit.

For a capacitor discharging through a resistor, current through the resistor is $i = v_c/R$. Substituting the values given in the question

$$i = [200 \exp(-t/10^{-2})]/10^5 \qquad (9.2)$$

The initial current through the circuit will be 2 mA and figure 9.5 shows how the approximate discharge curve can be constructed. A straight line is drawn from I = 2 mA at t = 0 to a point on the time axis equal to the time constant of the circuit. (From the values given in the question CR = 10 ms.) Any point A is selected on this line near to the initial current value, and a straight line is now drawn from A to meet the time axis at a point which is as far to the right of the time constant as A is to the right of the vertical axis. On this second line, any point B is selected, and a straight line is then drawn from B to meet the time axis at a point which is as far to the right of the time constant as B is to the right of the vertical axis. This procedure is repeated until the complete discharge curve is built up. Obviously the closer the points are together the more accurate the curve will be. When the capacitor voltage has fallen to 100 V, the current through the circuit will have fallen to 1 mA. From the curve, the time is 6·7 ms which compares closely with the time of 6·9 ms derived from equations 9.1 or 9.2.

For differentiating circuits, the time constant should be less than one-tenth of the input-pulse width, to give fast discharge, therefore

$$RC \leqslant T/20$$
$$\leqslant \frac{1}{20f}$$

where f is the frequency in Hz

Therefore

$$f \leqslant \frac{1}{20 \times 10^{-2}} \leqslant 5\ \text{Hz}$$

For integrating circuits, the time constant should be greater than ten times the input-pulse width, to give a slow discharge,

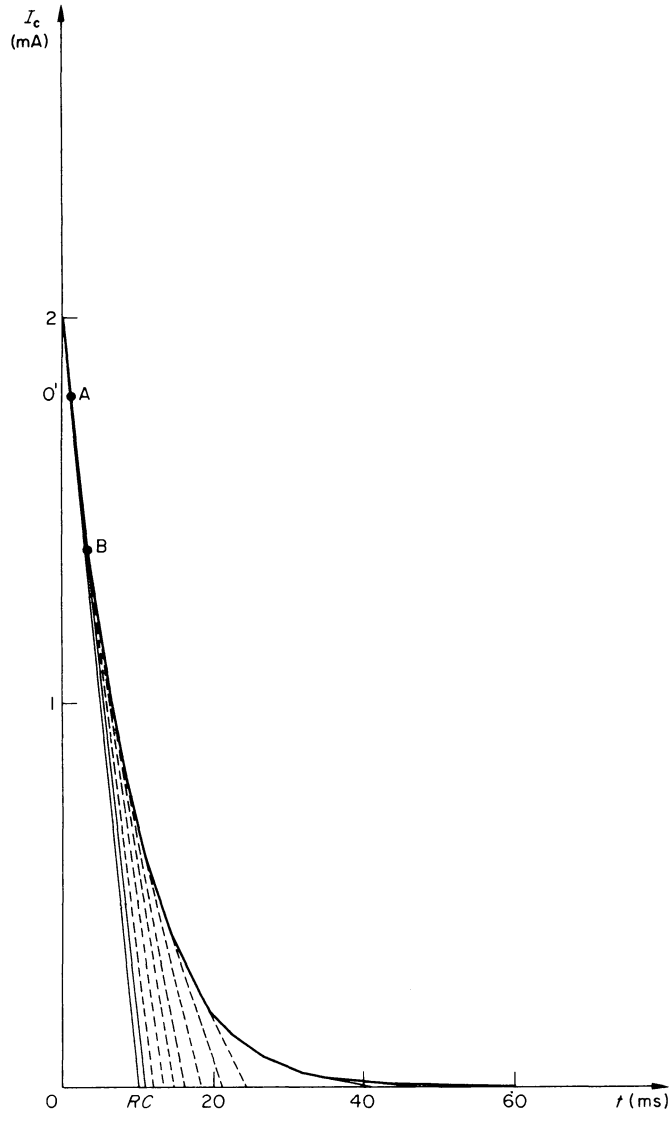


Figure 9.5

therefore

$$RC \geqslant \frac{10}{2f}$$

$$f \geqslant 500 \text{ Hz}$$

9.3 Monostable multivibrator

Explain the action of the circuit shown in figure 9.6 when a trigger pulse is applied to the input. Illustrate your answer with scaled time-and-voltage-waveform diagrams of the voltages at the base and collector of Tr_2. It may be assumed that the collector and base voltages are zero.

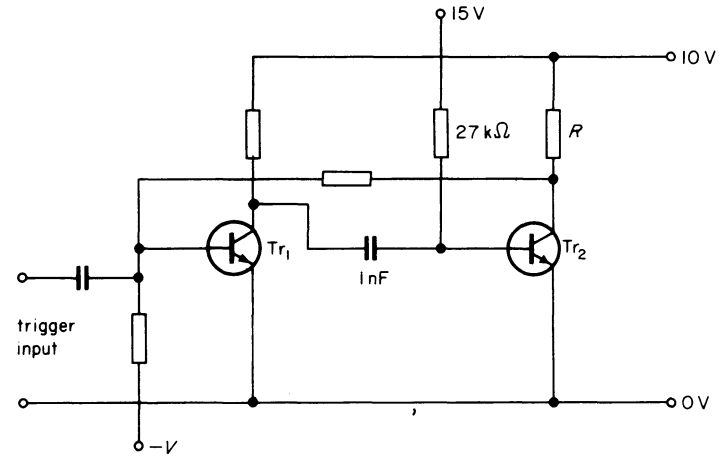


Figure 9.6

(ET5)

The circuit shown in figure 9.6 is a *monostable multivibrator*. Under quiescent conditions, Tr_2 will be saturated, as its base is connected to the 15 V line through the 27 kΩ resistor. Its collector voltage will be zero volts; hence, the base of Tr_1 will be at a negative voltage, and Tr_1 will be cut off. The action of the circuit is best illustrated by considering the waveforms shown in figure 9.7.

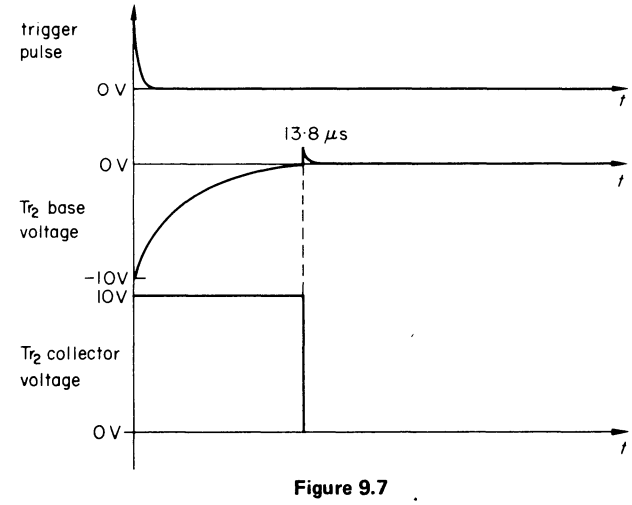


Figure 9.7

On application of a positive trigger-pulse of sufficient amplitude to saturate Tr_1, the collector voltage of Tr_1 changes from 10 V to 0 V. The 1 nF capacitor passes this instantaneous *negative* 10 V change to Tr_2 base thereby cutting off Tr_2, whose collector voltage then rises from 0 V to 10 V. The circuit is now in a quasi-stable state and remains in this state until the 1 nF capacitor discharges from −10 V towards 15 V. However, when the capacitor voltage reaches zero, Tr_2 will saturate and will again cut off Tr_1. The circuit will now remain in this stable state until another trigger pulse is applied.

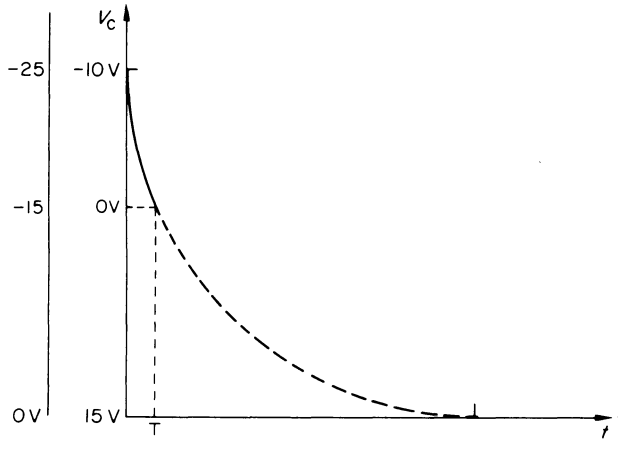


Figure 9.8

The period T of the quasi-stable state can be found from the capacitor discharge curve, using a false zero on the voltage axis, as shown in figure 9.8.

$$-15 = -25 \exp(-T/RC)$$

$$\exp(T/RC) = 1{\cdot}67$$

therefore

$$T = 27 \times 10^3 \times 10^{-9} \log_e 1{\cdot}67$$

$$= 13{\cdot}8\,\mu s$$

9.4 Bistable multivibrator

Draw the circuit diagram of a bistable multivibrator suitable for counting in binary code from a single pulse source. Describe, with the aid of suitable waveform diagrams, its principle of operation; give reasons for the use of steering diodes and pulse differentiating circuits. Explain with the aid of a block diagram how a number of such stages can be connected to count in decades.

(ET5)

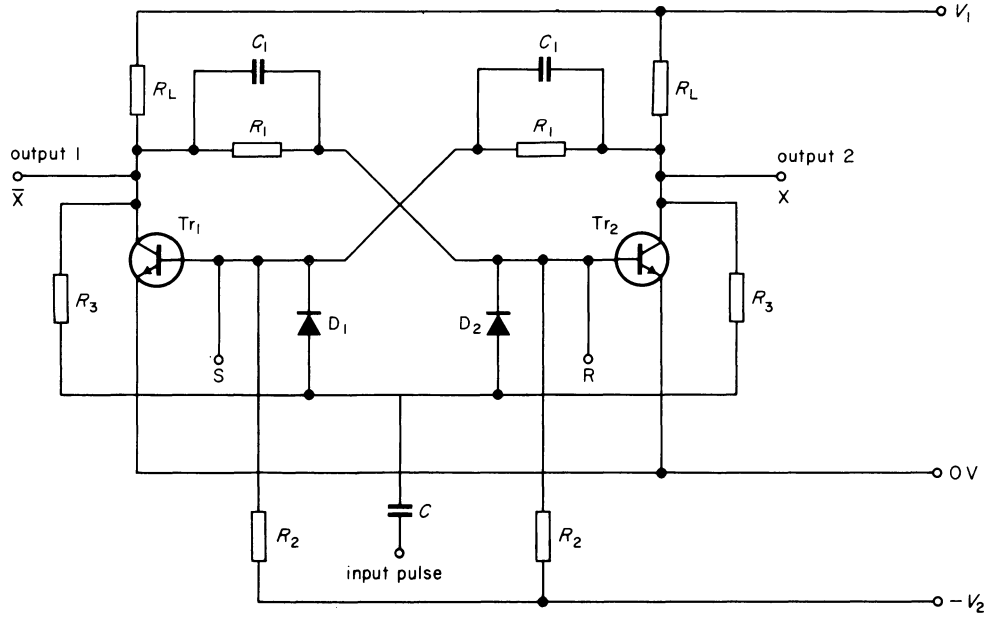


Figure 9.9

Figure 9.9 shows a typical circuit diagram of a practical *bistable multivibrator*. Initially this circuit is designed such that when one transistor is saturated, the other one is cut off. If Tr_1 is saturated, its collector voltage is approximately zero volts; therefore, the base of Tr_2 will be held at some negative voltage due to the potential-divider action of R_1 and R_2 between Tr_1 collector and the $-V_2$ supply rail. Tr_2 is cut off, and its collector voltage will nearly be V_1 (less the voltage drop across R_L). The choice of R_1, R_2 and $-V_2$ should also ensure that Tr_1 base voltage is positive enough to keep Tr_1 saturated. The circuit is now in the first of its two stable states and if the collector voltage of Tr_2 represents binary '1' and that of Tr_1 represents binary '0', this circuit can be used to store a binary digit or to count in binary.

When a positive input pulse is applied, the capacitor C forms a differentiating circuit with the input resistance of the transistors and a short rise-time pulse is produced as shown in figure 9.10,

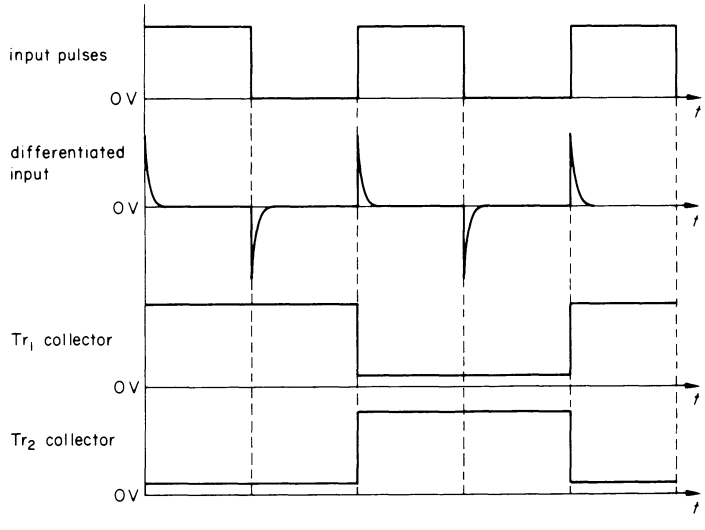


Figure 9.10

which is the ideal waveform for fast switching. The diodes D_1 and D_2 block any negative pulses and are also used to *steer* the positive pulse to the base of the *off* transistor. As Tr_1 is saturated, its collector-base junction is forward-biased, thus reverse-biasing D_1 through R_3. However, as Tr_2 is cut-off, its collector-base junction is reverse-biased, thus forward-biasing D_2 through R_3. Consequently, the first positive pulse passes through D_2 and switches on Tr_2. The collector voltage of Tr_2 then falls to zero volts, thereby cutting off Tr_1. The circuit is now in the second of its two stable states, with Tr_2 saturated and Tr_1 cut off. Note that in this state the output X is a '0' and the complemented output $\bar{X}$ is a '1'. Each time an input pulse is applied, the circuit changes state as shown in figure 9.10 and the output counts in binary. The capacitors C_1 strapped across resistors R_1 are used to speed up the switching time of the circuit.

In practice, two further inputs are used: the *Set* input (S) and the *Reset* input (R). If a positive pulse is applied on the *Set* input, Tr_1 will always saturate and Tr_2 will be cut off, thereby giving an output '1'; that is, the output is set to '1'. Similarly, a positive pulse on the *Reset* input always resets the output to '0'.

Figure 9.11 shows the block diagram of a decade counter using four bistable multibivrators. Initially, all the bistables are reset to zero. The first input pulse switches B_1; B_1 output goes to '1'; and B_1 complemented output goes to '0' (this voltage change at the complemented output is negative, and so it is blocked by the steering diodes of B_2). Hence, after the first pulse, the counter reads 0001. The second pulse switches B_1 output to '0'; and the accompanying positive change at the $\bar{X}$ output of B_1 switches B_2 output to '1'; while the negative change at the $\bar{X}$ output of B_2 cannot switch B_3. The counter now reads 0010; that is, decimal 2. In this way, without the feedback from B_4 output, the counter would count to binary 1111 (that is, decimal 15) after fifteen input pulses and would reset to 0000 on the sixteenth input pulse. To make the counter cycle on ten input pulses (that is, to operate as a decade

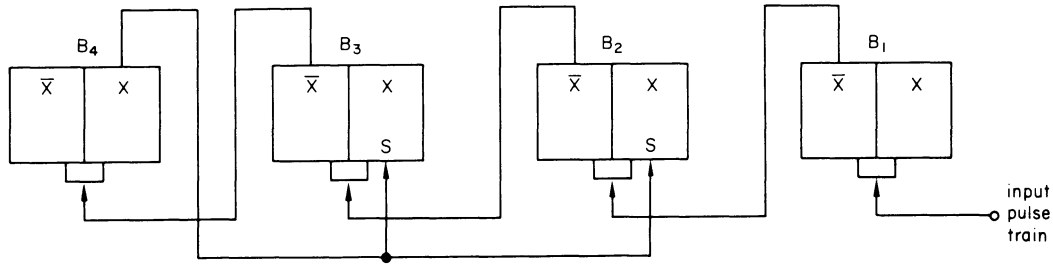


Figure 9.11

counter) the output of B_4 is used to set B_3 and B_2, thus simulating the action of six input pulses. Thus on the eighth input pulse, the counter first reads 1000, then feedback occurs and the reading changes to 1110. After the ninth pulse, the counter reads 1111, and resets to 0000 after the tenth pulse. In practice, the counter can be made cyclic on any number between nine and fifteen by connecting the feedback line to appropriate bistables.

9.5 Schmitt-trigger circuits

(a) Figure 9.12 shows the circuit diagram of a 'Schmitt'-trigger circuit. Describe the action of this circuit and hence, state two uses for it.

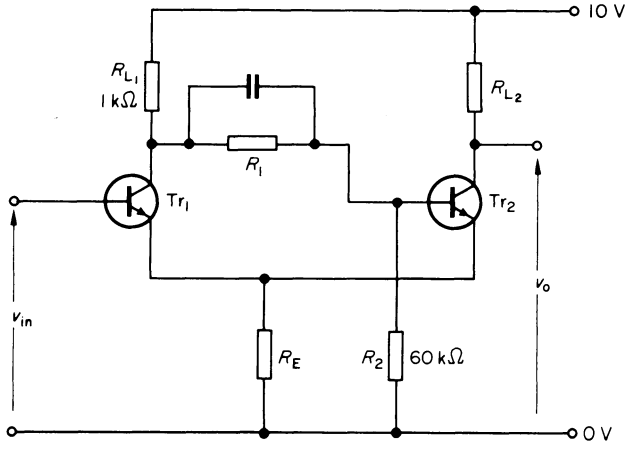


Figure 9.12

(b) In the circuit of figure 9.12, using the component values given, determine the remaining component values and the 'lower trigger potential' (LTP) given the following data
Minimum current gain of the transistors $h_{FE} = 50$
Emitter current of Tr_2 *when conducting = 7* mA
Base-emitter voltage of 'on' transistor $V_{BE(on)} = 0{\cdot}5$ V
Collector-emitter voltage of 'on' transistor $V_{CE(sat)} = 0{\cdot}2$ V
Upper trigger potential (UTP) = 4 V

(H.N.C.)

(a) This circuit is a special form of emitter-coupled bistable multivibrator that is switched between two stable states by the amplitude of the input voltage applied.

In the circuit of figure 9.12, Tr_2 is saturated because of the positive voltage applied to its base by the potentiometer R_{L_1}, R_1 and R_2. This is the first stable state, and the output on the collector of Tr_2 is low.

The circuit remains in this first state until the input voltage on Tr_2 base exceeds the combined voltage V_{E_2} (across R_E) and $V_{BE(on)}$, when Tr_1 switches on. This voltage is known as the upper trigger potential (UTP). As collector current now flows in Tr_1, the collector voltage falls and thereby reduces the positive voltage on the base of Tr_2. Simultaneously, the addition of the Tr_1 emitter current to the Tr_2 emitter current flowing through R_E results in the common V_E voltage rising rapidly. The combined effect of Tr_2 base voltage falling and emitter voltage rising quickly cuts off Tr_2, and the output voltage at Tr_2 collector goes high.

The circuit remains in this second state until the input voltage on Tr_1 base falls to a value that is lower than the combined voltage V_{E_1} (across R_E) and $V_{BE(on)}$, when Tr_1 switches off. This voltage is known as the lower trigger potential (LTP). With the cessation of collector current, V_{C_1} rises rapidly and carries with it the base potential of Tr_2, with the result that Tr_2 switches on again and rapidly self-biases to saturation. Note that V_{E_1} is less than V_{E_2} as the value of emitter current at which LTP is calculated is lower than the corresponding value for the UTP, the input voltage at LTP usually not being large enough to saturate Tr_1. In practice, the values of UTP and LTP can be varied or made equal by suitable choice of component values.

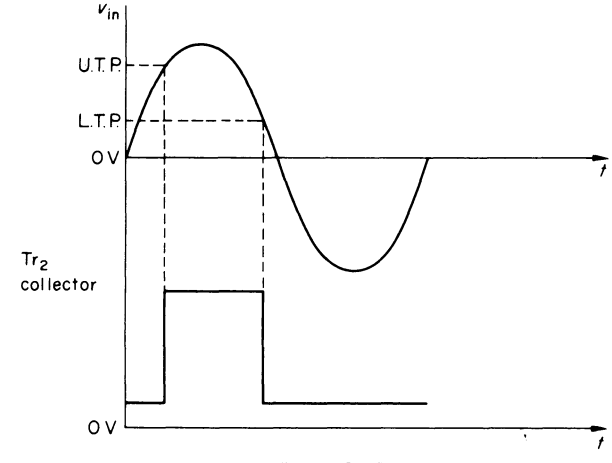


Figure 9.13

The waveforms in figure 9.13 illustrate the action of the circuit for a sinusoidal input. The circuit can be used either as a level detector to discriminate between two given input levels, or as a

pulse shaper to produce a rectangular pulse output from a smaller, distorted, or sinusoidal input.

(b) At the UTP, Tr_1 base voltage is 4 V; therefore its emitter voltage is $4 - V_{BE(on)} = 3{\cdot}5$ V, and $R_E = (3{\cdot}5)/7 = 0{\cdot}5$ kΩ. As Tr_2 is saturated, its collector voltage is $3{\cdot}5 + V_{CE(sat)} = 3{\cdot}7$ V; and therefore, assuming $I_C = I_E$, $R_L \approx (10 - 3{\cdot}7)/7 = 0{\cdot}9$ kΩ. The base current of Tr_2, $I_{B_2} = 7/50 = 0{\cdot}14$ mA, also the current I_2 through R_2 is $4/60 = 0{\cdot}067$ mA. The voltage drop across R_{L_1} and R_1 is then given by

$$(I_2 + I_{B_2})(R_{L_1} + R_1) = (10 - 4) = 6$$

$$(R_{L_1} + R_1) = \frac{6}{(0{\cdot}14 + 0{\cdot}067)} = 29 \text{ k}\Omega$$

and $R_1 = 28$ kΩ

At the LTP, the current I_3 through R_{L_1} has two components: the collector current I_{C_1} of Tr_1, and the current I_4 through R_1 and R_2. Assuming $I_{C_1} = I_{E_1}$, I_{C_1} is approximately equal (in milliamps) to $V_{E_1}/(0{\cdot}5)$; while I_4 is given by

$$V_{C_1}/(R_1 + R_2)$$

which (in milliamps)

$$= V_{C_1}/88$$

However, I_3 is also given by

$$(V_{CC} - V_{C_1})/R_{L_1}$$

which (in milliamps)

$$= (10 - V_{C_1})$$

therefore

$$10 - V_{C_1} = \frac{V_{E_1}}{0{\cdot}5} + \frac{V_{C_1}}{88} \qquad (9.3)$$

Also, the emitter voltage V_{E_1} of Tr_1 is the same as the emitter voltage V_{E_2} of Tr_2; that is, $V_{B_2} - V_{BE(on)} = (60/88)V_{C_1} - 0{\cdot}5$ volts. Substituting this value for V_{E_1} in equation 9.3

$$10 - V_{C_1} = \frac{120V_{C_1}}{88} - 1 + \frac{V_{C_1}}{88}$$

$$V_{C_1} = 11 \times (88/209) = 4{\cdot}6 \text{ V}$$

Neglecting I_4 (which is only $V_{C_1}/88 = 0{\cdot}05$ mA)

$$I_{C_1} = (10 - 4{\cdot}6)/R_{L_1} = 5{\cdot}4 \text{ mA}$$

As I_{C_1} is approximately equal to I_{E_1}

$$V_{E_1} = I_{E_1} \times R_E = 5{\cdot}4 \times 0{\cdot}5 = 2{\cdot}7 \text{ V}$$

therefore

$$\text{LTP} = V_{E_1} + V_{BE(on)} = 2{\cdot}7 + 0{\cdot}5 = 3{\cdot}2 \text{ V}$$

9.6 Operational amplifier as an inverter

An inverter comprises a high gain amplifier of gain A, an input resistor R_1 and a feedback resistor R_0. The input is V_1 and the output is V_0. Derive an expression relating input and output.

If the input and feedback resistors are equal for a nominal gain of unity, what is the value of A for an error of 1 per cent in the inversion?

(TT5)

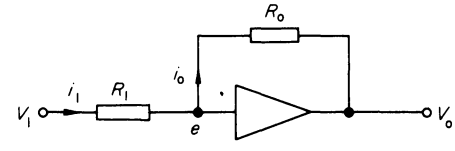


Figure 9.14

The amplifier shown in figure 9.14 is known as an operational amplifier. It usually has an overall phase shift of 180° and a very high input resistance. Therefore, assuming the input current to the amplifier to be negligible

$$i_1 = i_0$$

$$\frac{V_1 - e}{R_1} = \frac{e - V_0}{R_0}$$

Also

$$V_0 = -Ae$$

therefore

$$\frac{V_1}{R_1} + \frac{V_0}{AR_1} = \frac{-V_0}{AR_0} - \frac{V_0}{R_0}$$

$$\frac{V_0(1 + 1/A + R_0/AR_1)}{R_0} = \frac{-V_1}{R_1}$$

$$V_0 = \frac{-V_1R_0}{R_1[1 + (1/A)(1 + R_0/R_1)]}$$

When $R_0 = R_1$

$$\frac{V_0}{V_1} = \frac{-1}{1 + 2/A}$$

$$= -(1 + 2/A)^{-1}$$

Using the binomial expansion to one place

$$V_0/V_1 = -(1 - 2/A)$$

In practice

$$V_o/V_1 = -1$$

therefore the percentage error $= \frac{2}{A} \times 100 = 1$

Thus

$$A = 200$$

9.7 Operational amplifier as a summer and integrator

(a) Show from first principles that an operational amplifier may be used to perform the functions of summation and integration.

(b) It is required to add three voltages V_1, V_2 and V_3 using an operational amplifier which has an infinite input impedance and infinite gain. The input resistors each have values of 100 kΩ. *Calculate the value of the feedback resistor such that the output is equal to $V_1 + V_2 + V_3$. If the gain of the amplifier were only −200, calculate the exact value of the feedback resistor such that the output remains unchanged.*

(c) Why are differentiators not often employed in practical analogue computer circuits?

(H.N.C.)

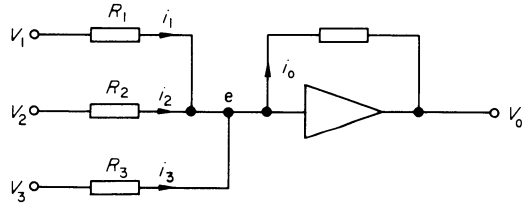


Figure 9.15

(a) In figure 9.15 as the amplifier has infinite input impedance, it will take no input current. Also, as it has infinite gain, its input will be virtually at earth potential. Therefore

$$i_1 + i_2 + i_3 = i_o$$

$$V_1/R_1 + V_2/R_2 + V_3/R_3 = V_o/R_o \qquad (9.4)$$

and

$$V_o = -V_1R_o/R_1 - V_2R_o/R_2 - V_3R_o/R_3$$

Therefore the output voltage is the sum of all the input voltages, if all the resistors are equal.

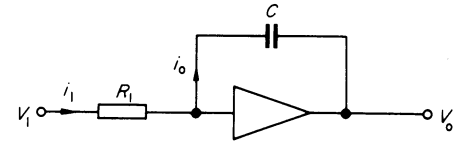


Figure 9.16

Similarly, in figure 9.16, $i_1 = i_o$, therefore

$$\frac{V_1}{R_1} = -C\frac{dV_o}{dt}$$

$$V_o = -\frac{1}{CR_1}\int V_1\,dt$$

Therefore, the output voltage of this circuit is the integral of the input voltage.

(b) As shown in part (a) for $V_o = V_1 + V_2 + V_3$, all the resistors must be equal; therefore, the feedback resistor must be 100 kΩ.

When the amplifier has a finite gain, equation 9.4 becomes

$$\frac{V_1 - e}{100} + \frac{V_2 - e}{100} + \frac{V_3 - e}{100} = \frac{e - V_o}{R_o} \qquad (9.5)$$

Substituting $V_0 = -200\,e$ in equation 9.5

$$V_1 + V_2 + V_3 = -V_o(100/R_o + 1/2R_o + 3/200)$$

Hence, to obtain

$$-V_o = V_1 + V_2 + V_3$$

$$\frac{201}{2R_o} + \frac{3}{200} = 1$$

$$R_o = \frac{201 \times 200}{2 \times 197} = 102\ \text{k}\Omega$$

(c) Differentiators are not often used in analogue computers because any noise on the input signal appears as a much larger proportion of the output signal, as their output is proportional to the slope of the input voltage.

9.8 Exercises

Exercise 9.1

What is meant by the expression 'time constant of a circuit containing resistance and capacitance in series'?

The operating time of a process timer is governed by the discharge of a 2 μF capacitor through a 1 MΩ resistor. If the capacitor discharges from 100 V to 50 V during the timing period, determine this time either graphically or by calculation.

Sketch the connection diagram of any simple process timer working on this principle and briefly explain its operation.
(Answer: 1·38 s) (ET5)

Exercise 9.2

In the circuit shown in figure 9.17, $(R_1 + R_2) = 20\ k\Omega$.

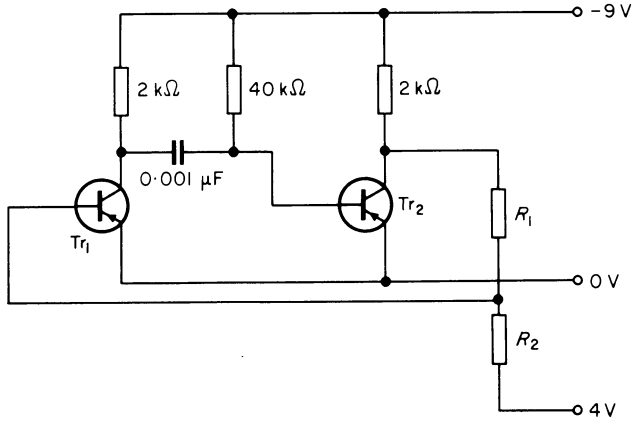


Figure 9.17

Determine their values if the base of Tr_1 is 1·5 V positive with respect to its emitter when Tr_2 is saturated and also calculate the values of the collector currents of Tr_1 and Tr_2.

Show where a sharp positive pulse can be applied to change the state of the transistors, and trace the sequence of events until the transistors are restored to their original condition.
(Answers: 7·5 kΩ, 12·5 kΩ, 4·5 mA, 4·3 mA) (H.N.C.)

Exercise 9.3

Describe the operation of the monostable multivibrator circuit shown in figure 9.18.

Given that both transistors have a current gain $h_{FE} = 50$ and negligible $V_{BE(on)}$ when conducting, and that the collector current of Tr_2 is 8 mA, determine the height and width of the output pulse, proving any formulae used.
(Answers: 7·7 V, 6·5 ms) (H.N.C.)

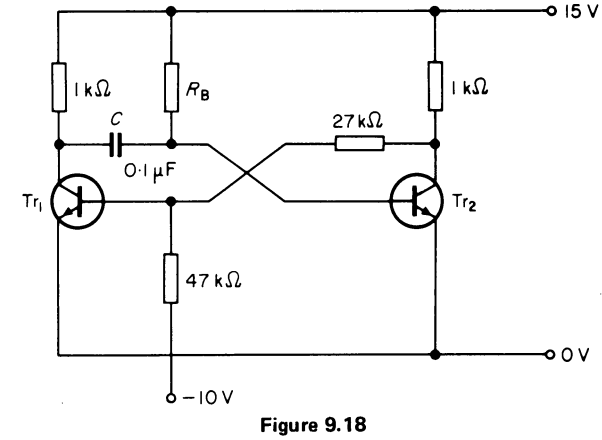


Figure 9.18

Exercise 9.4

What is meant by binary counting and what advantage has it over decimal counting? Convert 157 into binary form.

The circuit shown in figure 9.19 is one stage of a binary counter. Explain in detail the action of the circuit and sketch the output waveform if positive-going trigger pulses of adequate amplitude and duration at a repetition rate of 500 per second are applied. Explain how a number of such stages form a binary counter.
(ET5)

Exercise 9.5

Give a circuit diagram of a commercial bistable multivibrator circuit and explain its operation, commenting on the purpose of each component.

With the aid of a block diagram, explain how four such circuits can be used as (a) a decade counter and (b) a counter cyclic on thirteen pulses.
(H.N.C.)

Exercise 9.6

Sketch a circuit diagram for and explain the action of a 'Schmitt'-trigger circuit using either valves or transistors.

Explain briefly with the aid of a block diagram the use of a 'Schmitt'-trigger circuit in industrial equipment.
(ET5)

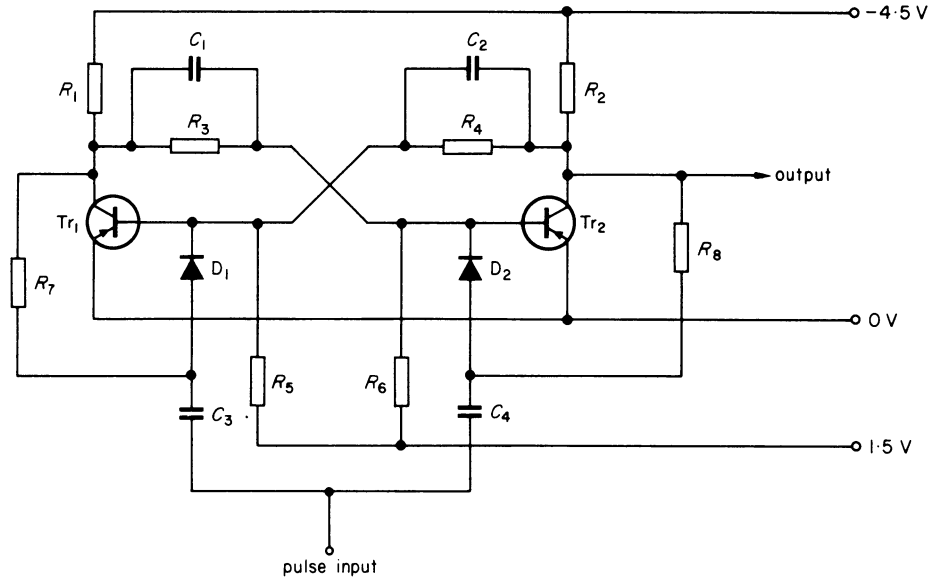


Figure 9.19

Exercise 9.7

(a) Draw and explain the action of a transistor 'Schmitt'-trigger circuit.

(b) Design a 'Schmitt'-trigger circuit using *npn* transistors with a minimum common-emitter current gain of 40. The available supply voltage is 12 V. The circuit is to change state when the input is rising and passing through 3 V. Assume that the base-emitter and collector-emitter saturation voltages are 0·4 and 0·2 V respectively. Estimate the value to which the input voltage must fall for the circuit to revert to its original state. (*Hint:* Assume I_E = 10 mA.)
(Answer: 2·1 V) (I.E.R.E.)

Exercise 9.8

A d.c. amplifier has an input resistance of 1 MΩ and an open circuit voltage gain of −400. The amplifier is to be used in an analogue sign changer with input and feedback resistors of 1 MΩ. Determine the percentage error in this operation due to the finite values of input resistance and gain.
(Answer: 0·74) (U.L.C.I.)

Exercise 9.9

(a) Show from first principles that an operational amplifier can be used to perform differentiation.

(b) An operational amplifier used as a summer has infinite input impedance and infinite gain. If its input resistors are 200 kΩ, 500 kΩ and 1 MΩ; with corresponding input voltages of 2 V, 1 V, and 5 V; and a feedback resistor of 1 MΩ, determine its output voltage. If the gain of the amplifier is reduced to −100, determine the percentage change in output voltage.
(Answers:−17 V, 8·3 per cent)

10 Boolean algebra and logic circuits

10.1 Diode logic gates

Draw and explain the action of logic circuits which perform the functions (a) OR and (b) AND. Clearly indicate the polarities and type of logic used. Construct truth tables for three input OR and AND circuits.

(ET5)

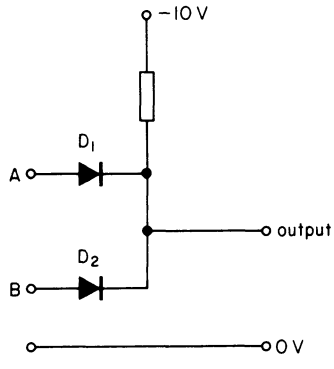


Figure 10.1a

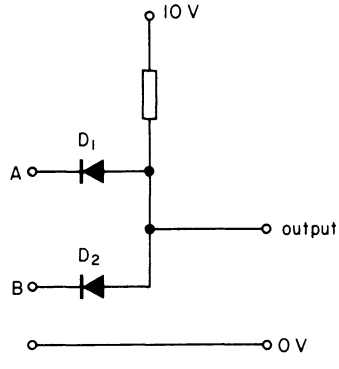


Figure 10.1b

Considering the circuit of figure 10.1a, let 5 V be equivalent to binary '1' and 0 V be equivalent to binary '0'. When A and B are both at 0 V, both diodes are forward-biased; and, assuming ideal diodes, the output will be 0 V. If A goes to 5 V, instantaneously both diodes would conduct. When D_2 is conducting, however, the output voltage is 0 V, which still leaves D_1 forward-biased. Therefore, D_1 conducts and raises the output voltage to 5 V, which cuts off D_2. Similarly, if B goes to 5 V while A is still at 0 V, the output is raised to 5 V and D_1 is cut off. When both A and B go to 5 V, both diodes conduct, and the output voltage is again 5 V.

The logic used in this example is referred to as *positive logic* because the voltage used to represent binary '1' is more positive than that used to represent binary '0'. Therefore, this circuit performs the logical OR function using positive logic: that is, it gives an output '1' if A OR B OR *both* are '1'.

If the logic levels are interchanged so that 5 V = '0' and 0 V = '1', the circuit is said to use *negative logic*. It would now perform the logical AND function: that is, it gives an output '1' only when A AND B are '1'.

In figure 10.1 b, using positive logic, when A and B are at 0 V the output is 0 V. If A goes to 5 V, D_2 still conducts and keeps the output at 0 V, which reverse biases D_1. Similarly, if B goes to 5 V while A is still at 0 V, the output still remains at 0 V and D_2 is cut off. However, when both inputs go to 5 V, both diodes conduct and the output is raised to 5 V. Therefore, this circuit performs the AND function for positive logic or the OR function for negative logic.

A truth table is a tabular method of expressing the logical function of a circuit: that is, the circuit output is given for all possible input combinations. Tables 10.1a and 10.1b show the truth tables for three input OR and AND circuits respectively.

Table 10.1a

INPUTS			OUTPUT
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Table 10.1b

INPUTS			OUTPUT
A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

10.2 Transistor logic gates

(a) Define positive logic.

(b) State the main disadvantage of diode-resistor logic.

(c) Draw the circuit diagram of a logic AND gate suitable for cascade operation and explain what is meant by 'fan-out' of such a circuit, indicating the factors upon which it depends.

(ET5)

(a) Positive logic has already been defined in section 10.1.

(b) The main disadvantage of diode-resistor logic is that, as the diodes have a finite forward resistance, there is a finite voltage drop through each gate. Thus, the high logic level falls and the low level increases, which limits the number of gates that can be used in cascade. Other disadvantages are the relatively low switching speed and the high power dissipation in the load resistor.

(c)

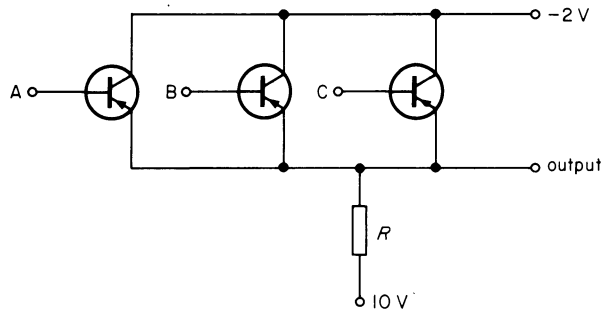


Figure 10.2

Figure 10.2 shows the circuit diagram of a transistor AND gate using positive logic (that is 5 V = '1' and 0 V = '0'). Each input uses a transistor that is connected as an emitter follower. When all the inputs are at 0 V, all the transistors are saturated and the output voltage will be at 0 V plus the small base-emitter (on) voltage; that is, a '0' output. If any of the inputs go to the 5 V level, the corresponding base-emitter diode is reverse biased, because with the output clamped at 0 V that transistor is cut off. If, however, all the inputs go to 5 V, all the transistors saturate again, and the output level rises to 5 V plus the base-emitter voltage of the transistor. The circuit thus performs the logical AND function.

The *fan-out* of a circuit is defined as the maximum number of identical circuits which can be supplied from the circuit without serious deterioration in its performance. In this circuit the fan-out is mainly determined by how much current the transistors can accept from the following gates without seriously affecting the output level. When only one transistor is saturated, as the base currents from the following transistors must all flow through that transistor, the logical '0' level changes, and this limits the fan-out of the circuit. The fan-out will therefore depend upon the transistor parameters and the value of the load resistor.

10.3 Venn diagrams

(a) Using Venn diagrams verify the Boolean expression

$A + BC = (A + B)(A + C)$

(b) Define the logic terms OR and NOT and draw R.T.L. circuits which provide these functions.

(c) Show how simple logic gates may be used to satisfy the truth table 10.2.

Table 10.2

INPUTS		OUTPUT
A	*B*	*S*
0	0	0
1	0	1
0	1	1
1	1	0

(ET5)

(a)

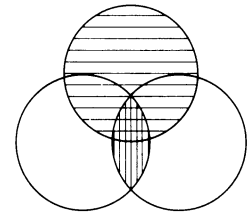


Figure 10.3a

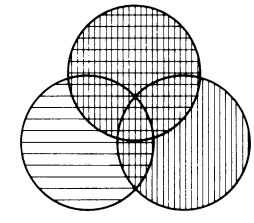


Figure 10.3b

Figure 10.3a shows the Venn diagram for $(A + BC)$ where the horizontal shading represents A, and the vertical shading represents B AND C; therefore, A OR BC is represented by all the shaded area. Figure 10.3b shows the Venn diagram of $(A + B)(A + C)$, where the horizontal shading represents $(A + B)$ and the vertical shading represents $(A + C)$; therefore, the cross-hatch shading represents $(A + B)$ AND $(A + C)$, which is the same net area as in figure 10.3a. Consequently, the two expressions are identical.

(b) Logical OR implies that an output '1' is obtained if any of the inputs is a '1'; that is, A OR B OR C OR any combination of them. Logical NOT implies that the output is always the opposite of the input; that is, NOT the input. Therefore, an input '1' gives an output '0' and vice versa.

Figure 10.4a shows the circuit diagram of a two-input OR gate and figure 10.4b shows that of an inverter.

(c) From the truth table 10.2, an output '1' is required for the input combinations shown in rows 2 and 3. Therefore

$$S = A\bar{B} + \bar{A}B$$

The required logic diagram is shown in figure 10.5.

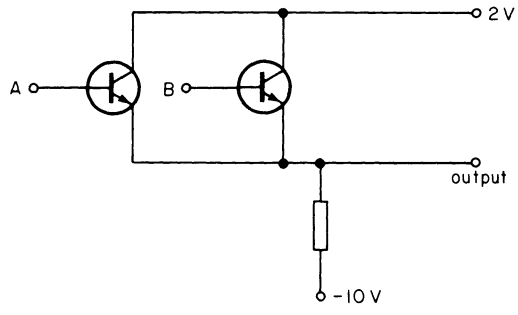


Figure 10.4a

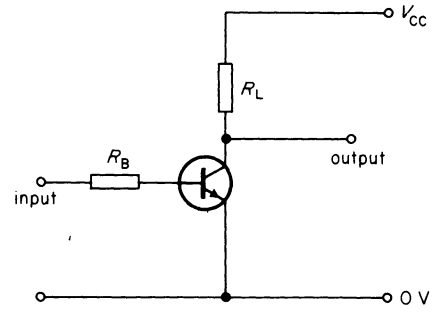


Figure 10.4b

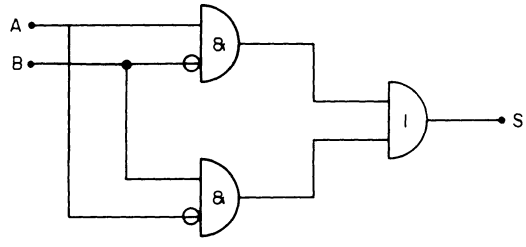


Figure 10.5

10.4 Logic design from truth table

(a) From the truth table 10.3 give a Boolean expression for the output.

Table 10.3

A	*B*	*C*	OUTPUT
0	1	1	0
0	1	0	0
1	0	1	1
1	1	0	1
0	0	0	0
1	0	0	0
1	1	1	1
0	0	1	0

(b) Using Boolean algebra simplify the expression determined in (a).

(c) Draw a logic diagram for the simplified expression given in (b).

(TT5)

From the truth table the output X is

(a) $X = A\bar{B}C + AB\bar{C} + ABC$

(b) $X = A\bar{B}C + AB(C + \bar{C})$

$= A\bar{B}C + AB$

$= A(B + \bar{B}C)$

$= A(B + C)$

(c)

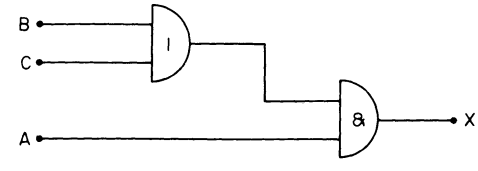


Figure 10.6

Figure 10.6 shows the logic diagram for $X = A(B + C)$.

10.5 De Morgan's theorems

(a) State De Morgan's theorems for two quantities A and B. Hence draw logic diagrams using NAND gates only for the logic functions NOT, OR and AND.

(b) Simplify the following Boolean expression and also find its minimum complementary form

$$X = AB\bar{C} + A\bar{B}\bar{C} + \bar{A}BC + ABC + A\bar{B}C$$

$$\bar{A}\bar{B} = \bar{A} + \bar{B} \qquad (10.1)$$

$$\overline{A + B} = \bar{A}\bar{B} \qquad (10.2)$$

Equations 10.1 and 10.2 illustrate De Morgan's theorems for two variables A and B. Note that these give the rules for obtaining the

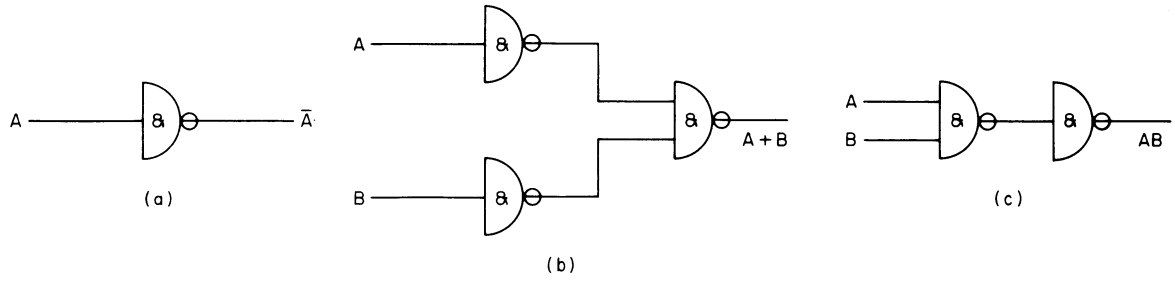


Figure 10.7

complement of a complete Boolean expression which are (i) complement each variable in the expression and (ii) change all logical multiplication signs to logical addition signs and vice versa.

For the NOT function

$$X = \bar{A}$$

which is a one input AND gate.

For the OR function

$$X = A + B = \overline{\overline{A + B}}$$
$$= \bar{\bar{A}}\bar{\bar{B}}$$

For the AND function

$$X = AB = \bar{\bar{A}}\bar{\bar{B}}$$

The corresponding logic diagrams are shown in figures 10.7a, 10.7b and 10.7c.

(b) $X = AB\bar{C} + ABC + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}BC$

$= AB(\bar{C} + C) + A\bar{B}(\bar{C} + C) + \bar{A}BC$

$= AB + A\bar{B} + \bar{A}BC = A(B + \bar{B}) + \bar{A}BC$

$= A + \bar{A}BC$

$= A + BC$

therefore

$$\bar{X} = \overline{A + BC}$$
$$= \bar{A}(\bar{B} + \bar{C})$$

10.6 Resistor-transistor logic

(a) With the aid of a circuit diagram, explain the operation of a resistor-transistor NOR logic element.

(b) Show, in logic form, how one or more such elements may be used together to produce a logic AND function, a logic OR function and a logic NOT function.

(TT5)

(a)

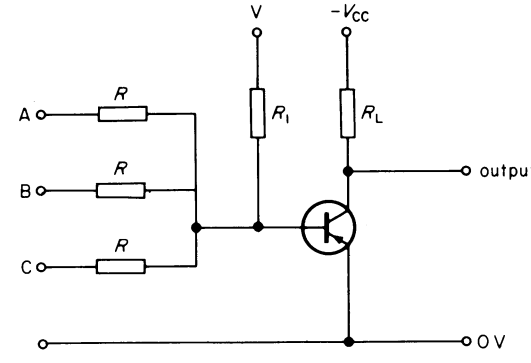


Figure 10.8

Figure 10.8 shows the circuit diagram of a R.T.L. NOR gate where $-V_{CC} \equiv$ '1' and 0 V $\equiv$ '0'. When all the inputs are at 0 V, the base of the transistor must then be held positive by the positive supply. Therefore, the transistor is cut off and the output voltage is V_{CC} volts. If any input goes to $-V_{CC}$ volts, the choice of the values of R and R_1 must be such that the base voltage of the transistor is made sufficiently positive to saturate it, and thereby cause the output to rise to approximately 0 V. Similarly, if more than one input goes to $-V_{CC}$ volts the base will tend to go more negative and keep the transistor saturated. Hence, the circuit performs the NOR function using negative logic; if the logic levels were reversed, the circuit would perform the NAND function.

(b) For the AND function

$$X = AB$$

therefore

$$\bar{X} = \overline{\bar{A}\bar{B}} = \bar{A} + \bar{B}$$

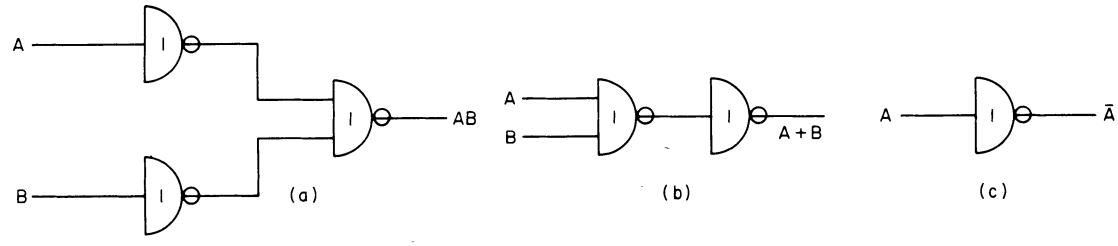


Figure 10.9

Also

$$X = \bar{\bar{X}} = \overline{\bar{A} + \bar{B}}$$

For the OR function

$$X = A + B$$

therefore

$$X = \bar{\bar{X}} = \overline{\overline{A + B}}$$

For the NOT function, $X = \bar{A}$, which is simply a one input NOR gate.

Figures 10.9a, 10.9b and 10.9c show the corresponding NOR logic diagrams for the AND, OR and NOT functions.

10.7 Logic design from Boolean expression

(a) With the aid of logic drawings for the following two circuits construct a truth table to show that they are equivalent.

Circuit 1: Inputs B and C to an OR gate whose output is AND gated with input A to give output X;

Circuit 2: Two AND gates with separate inputs B and C share input A. The outputs of these gates enter an OR gate to give output Y.

(b) Draw the logic diagram of the following expression and using Boolean algebra with all working shown, simplify the expression and then draw the single logic element which it represents.

$$X = A[\overline{\bar{B} + \bar{A}(C + \bar{B}\bar{C})}]$$

(TT5)

(a) Figures 10.10a and 10.10b show the logic diagrams of circuits 1 and 2, and the corresponding truth tables are shown in table 10.4.

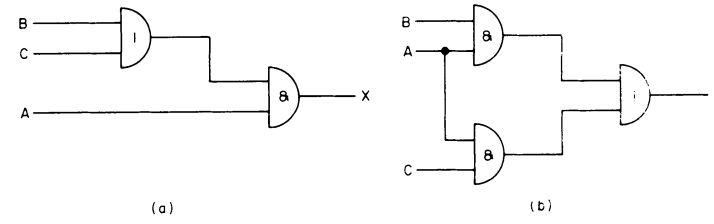


Figure 10.10

Table 10.4

A	B	C	$B+C$	AB	AC	$X=A(B+C)$	$Y=AB+AC$
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	0	1	1	1
1	1	0	1	1	0	1	1
1	1	1	1	1	1	1	1

Therefore, as the X and Y columns are identical, $X = Y$.

(b) Figure 10.11 shows the logic diagram to obtain X.

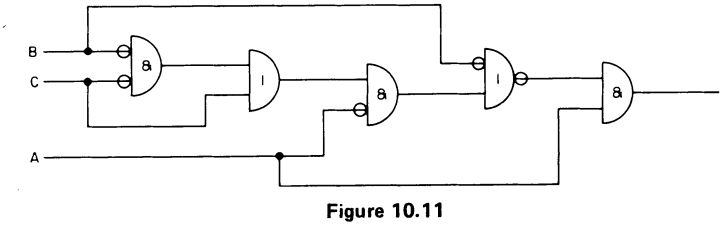


Figure 10.11

$$X = A[\overline{\bar{B} + \bar{A}(C + \bar{B}\bar{C})}] = A\{B[A + \bar{C}(B + C)]\}$$

$$= AB(A + B\bar{C} + \bar{C}\bar{C})$$

(as $C\bar{C} = 0$)

$$= AAB + ABB\bar{C}$$

$$= AB(1 + \bar{C})$$

$$= AB$$

Hence, this is the AND gate function.

10.8 Karnaugh maps

The permissible states in a safety system are expressed in the logic function

$$f = \bar{A}\bar{C} + B\bar{C} + \bar{A}BC + ABC$$

By means of a Karnaugh map, or other suitable means, simplify this expression and draw a block diagram to realise it using (a) any combination of AND, OR and NOT gates and (b) NAND gates only.

(ET5)

Using Boolean algebra

$$f = \bar{A}\bar{C} + B\bar{C} + BC(A + \bar{A})$$

$$= \bar{A}\bar{C} + B\bar{C} + BC$$

$$= \bar{A}\bar{C} + B(\bar{C} + C)$$

$$= B + \bar{A}\bar{C}$$

The Karnaugh map for f is shown in figure 10.12.

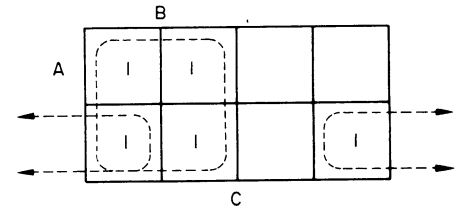


Figure 10.12

From this map

$$f = B + \bar{A}\bar{C} = \overline{\overline{B + \bar{A}\bar{C}}}$$

$$= \overline{\bar{B}\bar{A}\bar{C}}$$

Figure 10.13 shows the logic diagrams to obtain f in (a) AND, OR, and NOT logic and (b) NAND logic.

10.9 Simplification of Boolean expressions

(a) Simplify the Boolean function

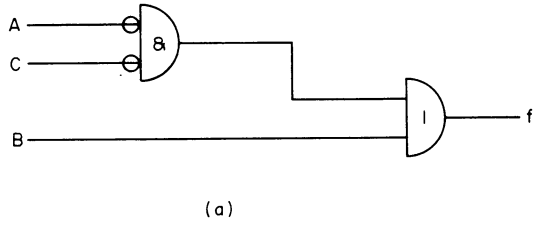
$$f = AD + A\bar{B}\bar{C} + \bar{B}C\bar{D} + \bar{A}CD + \bar{A}BC\bar{D}$$

(b) Find the minimum complementary expression.

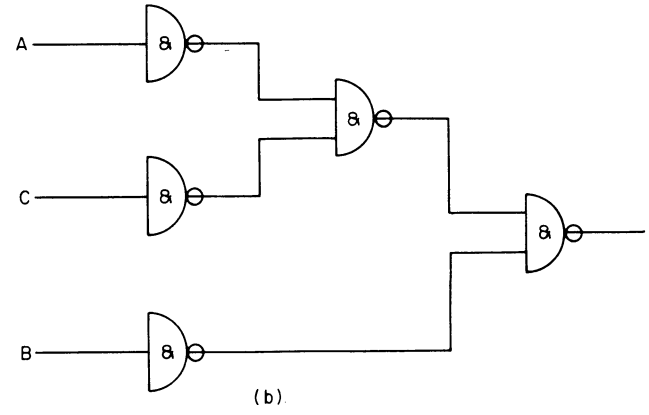
(c) Using De Morgan's theorem find another expression representing the function f.

(d) Using AND, OR and NOT gates draw logic diagrams showing how the expressions obtained in (a) and (c) can be derived from inputs A, B, C, and D.

(U.C.L.I.)



(a)



(b)

Figure 10.13

(a)

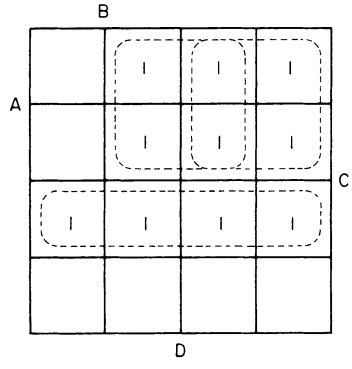


Figure 10.14

The Karnaugh map for f is shown in figure 10.14, from which

$f = AD + A\bar{B} + \bar{A}C$

(b) The expression for $\bar{f}$ is obtained from the blanks on the Karnaugh map, that is

$$\bar{f} = \bar{A}\bar{C} + AB\bar{D} \qquad (10.3)$$

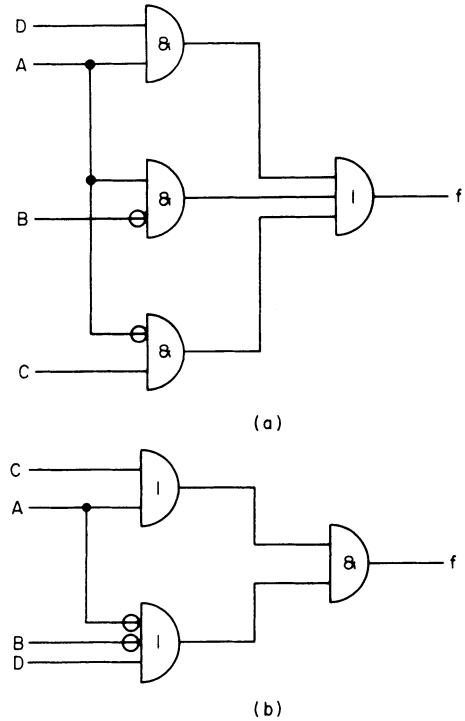


Figure 10.15

(c) Using De Morgan's theorem on expression 10.3

$f = \overline{\bar{f}} = \overline{\bar{A}\bar{C} + AB\bar{D}} = (A + C)(\bar{A} + \bar{B} + D)$

(d) Figures 10.15a and 10.15b show logic diagrams for the two expressions for f.

10.10 Diode-transistor and transistor-transistor logic gates

With the aid of circuit diagrams, describe the operation of (a) a diode-transistor (D.T.L.) NAND gate (b) a transistor-transistor (T.T.L.) NAND gate.

(a)

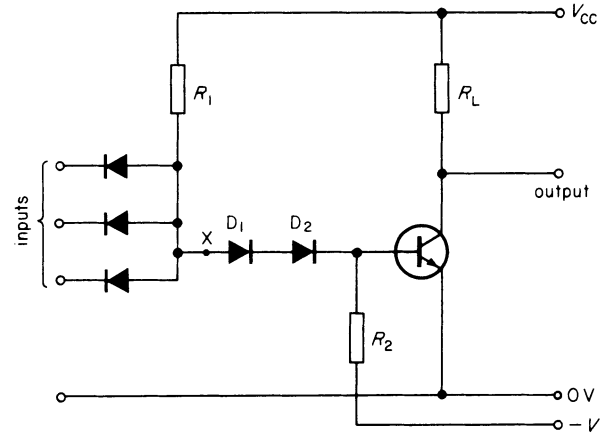


Figure 10.16

Figure 10.16 shows the circuit diagram of a D.T.L. NAND gate. Assume the following logic levels, binary '1' is approximately V_{CC} and binary '0' is $V_{CC(sat)}$ which can be considered to be 0 V.

When all the inputs are '1', all the input diodes are cut off, and a current flows through R_1, D_1 and D_2 and R_2 making the base voltage of the transistor sufficient to saturate it. Therefore, the output voltage is approximately 0 V, that is binary '0'.

If any one or more of the inputs goes to 0 V, the corresponding diode conducts and the voltage at point X is V_D volts, where V_D is the voltage drop across a forward-biased diode. Again a current flows through D_1, D_2 and R_2 making the base voltage of the transistor $-V_D$ volts, which cuts it off. Therefore, the output rises to the binary '1' level. Thus, the circuit performs the NAND function.

(b) Figure 10.17 shows the basic circuit diagram of a T.T.L. NAND gate; in which the input diodes of the D.T.L. gate are replaced by the multi-emitter transistor Tr_1.

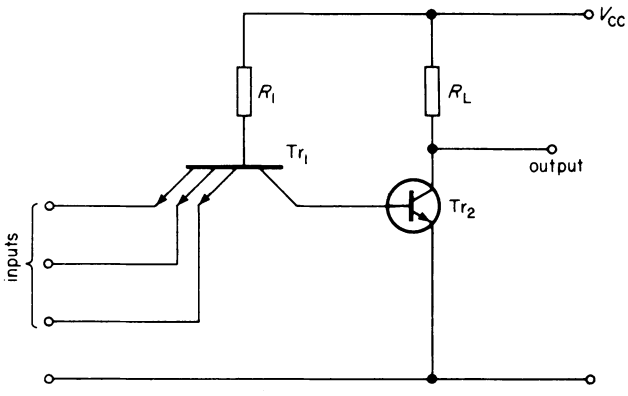


Figure 10.17

If all the inputs are at the '1' level, all the base-emitter diodes of Tr_1 are reverse-biased. However, the base-collector junction is forward-biased and current flows through R_2, across the base-collector junction and into the base of Tr_2, saturating it. The output voltage thus drops to the '0' level.

If any of the inputs go to the '0' level, the corresponding base-emitter diode becomes forward-biased and saturates Tr_1. Its collector voltage falls to $V_{CE(sat)}$ which is insufficient to switch on Tr_2. Therefore Tr_2 is cut off and the output voltage rises to the '1' level. Thus, the circuit performs the NAND function.

10.11 Use of logic gates

Explain why it is preferable to use only one type of gate in a logic circuit. The logic circuit shown in figure 10.18 is required to be changed into a circuit containing only one type of logic gate.

(a) Determine the logic equation for the circuit.

(b) By use of a suitable mapping technique, or otherwise, obtain a simplified expression.

(c) Draw a logic circuit to realise the simple expression using only NOR gates.

(ET5)

The advantages of using only one type of logic gate are

(1) relatively low cost for bulk buying;

(2) ease of interchangeability, hence easy maintenance;

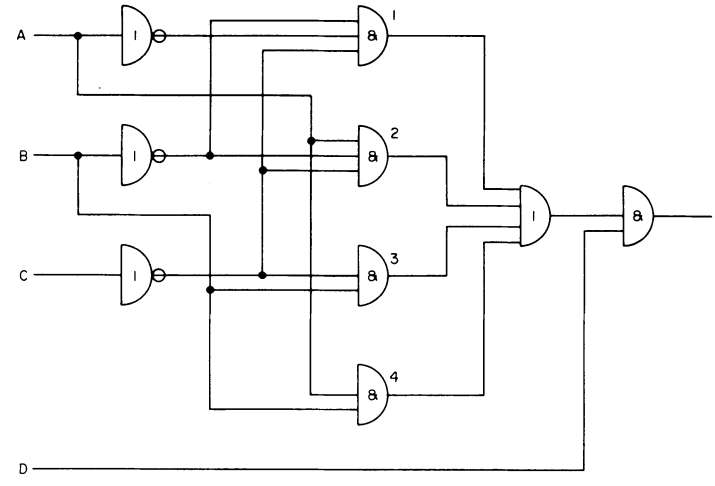


Figure 10.18

(3) logic levels will remain nearly constant throughout the circuit.

(a) Output from AND gate 1 = $\bar{A}\bar{B}C$
Output from AND gate 2 = $A\bar{B}\bar{C}$
Output from AND gate 3 = $B\bar{C}$
Output from AND gate 4 = AB

therefore

$$f = D(\bar{A}\bar{B}C + A\bar{B}\bar{C} + B\bar{C} + AB)$$
$$= \bar{A}\bar{B}CD + A\bar{B}\bar{C}D + B\bar{C}D + ABD$$

(b) The map of f is shown in figure 10.19.

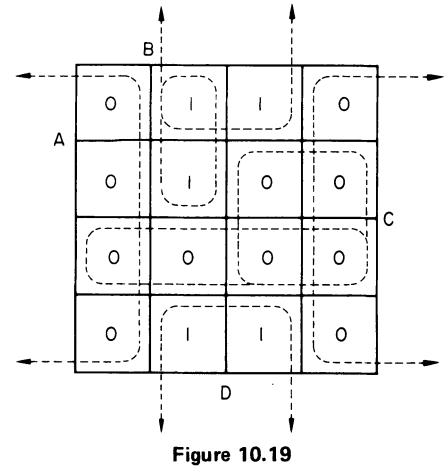


Figure 10.19

From the map

$$f = \bar{C}D + ABD$$

(c) Using De Morgan's theorems on the expression for f

$$f = \overline{\overline{C} + \overline{D} + \overline{A} + \overline{B} + \overline{D}}$$

Also, as $f = \bar{\bar{f}}$

$$f = \overline{\overline{\overline{\overline{\overline{\overline{\overline{C} + \overline{D} + \overline{A} + \overline{B} + \overline{D}}}}}}}$$

This expression requires seven NOR gates. To obtain a logic circuit using fewer gates, consider the minimal expression for $\bar{f}$ obtained from considering the '0's in figure 10.19.

$$\bar{f} = \bar{D} + \bar{A}C + \bar{B}C$$

therefore

$$f = D(A + \bar{C})(B + \bar{C})$$

But

$$f = \bar{\bar{f}} = \overline{\overline{\bar{D} + \overline{A + \bar{C}} + \overline{B + \bar{C}}}}$$

The logic circuit for this expression is shown in figure 10.20 and uses only five NOR gates.

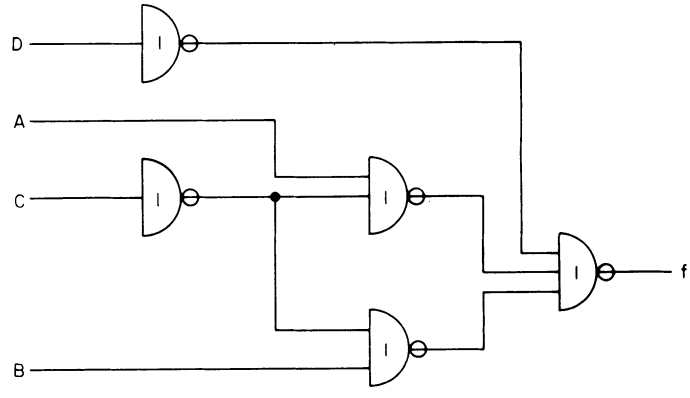


Figure 10.20

10.12 Exercises

Exercise 10.1

Draw logic circuits which perform the functions of (a) AND and (b) OR and explain their action. Polarities and the type of logic used must be clearly indicated. Explain the limitations of your circuits.

With the aid of a block diagram explain the use of these devices in a simple system. (At least three logic elements must be included.

(ET5)

Exercise 10.2

Draw and explain the operation of a semiconductor diode AND logic element for use with positive-going logic. Is this circuit still an AND if negative-going logic is used? If not, what is it?

(TT3)

Exercise 10.3

Explain, using suitable diagrams, the operation of diode logic circuits for performing the AND and OR functions, using (a) positive-going logic and (b) negative-going logic. What are the major disadvantages of diode logic compared with resistor-transistor logic?

(TT5)

Exercise 10.4

Explain briefly why Boolean algebra is used in the design of modern digital systems.

By means of (a) Boolean algebra and (b) truth tables, prove the following Boolean equations

$$A + \bar{A}B = A + B \qquad \bar{A} + \bar{B} + \bar{C} = \overline{ABC}$$

(TT5)

Exercise 10.5

Prove the following Boolean relationship by means of a truth table

$$\bar{P} + \bar{Q} = \overline{PQ}$$

(U.L.C.I.)

Exercise 10.6

Prove the following relationships using Venn diagrams

$$(\bar{A} + \bar{B})(A + B) = A\bar{B} + \bar{A}B$$

$$(A + \bar{B})(A + C) = A + \bar{B}C$$

Exercise 10.7

Develop equations to determine the minimum number of components for a logic circuit to satisfy the truth table 10.5.

Table 10.5

INPUTS			OUTPUT
A	*B*	*C*	*D*
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Draw the necessary logic diagram.
(Answer: $B\bar{C} + \bar{B}C$)

Exercise 10.8

The truth table 10.6 gives the output X that is required in a particular automated process for various combinations of its four inputs A, B, C and D.

Table 10.6

A	*B*	*C*	*D*	*X*
1	1	1	1	1
1	1	1	0	1
0	0	1	1	1
0	0	1	0	1
0	0	0	1	1
0	0	0	0	1
All other combinations				0

(a) Express the output as a Boolean function of the inputs in canonical form.

(b) Using the techniques of Boolean algebra reduce the function to a minimal.

(c) Verify your result using a Karnaugh map.

(d) Draw the logic diagram using the minimum number of AND, OR and NOT elements.

(Answer: $\bar{A}\bar{B} + ABC$) (I.E.R.E.)

Exercise 10.9

Write the Boolean equation given by the truth table 10.7 and show how a circuit containing NAND gates only can be connected to perform the required operation.

Table 10.7

INPUTS			OUTPUT
X	*Y*	*Z*	*F*
1	1	1	0
1	1	0	0
1	0	1	0
1	0	0	1
0	1	1	0
0	1	0	1
0	0	1	0
0	0	0	1

(Answer: $\overline{\overline{X\bar{Z}}}\,\overline{\overline{Y\bar{Z}}}$) (U.C.L.I.)

Exercise 10.10

(a) Simplify the Boolean expression

$f = A\bar{B}\bar{D} + AB\bar{C}\bar{D} + ABC\bar{D} + \bar{A}\bar{B}\bar{D} + \bar{A}BC\bar{D}$

(b) Find the minimum complementary expression and draw the corresponding logic diagram.

(Answers: $f = \bar{B}\bar{D} + A\bar{D} + C\bar{D}$ $\quad \bar{f} = D + \bar{A}\bar{B}\bar{C}$)

11 Principles and applications of thyristors

11.1 Operation of the thyristor

Describe using appropriate diagrams the operation of a controlled semiconductor rectifier (thyristor). Sketch the anode characteristics of the device and indicate curves for (a) zero gate current (b) normal forward gate current.

Draw a circuit diagram showing how a single thyristor can be used to control a unidirectional load current. Assume a sinusoidal load supply voltage. Discuss the merits and limitations of the method of gate control used.

(ET4)

The thyristor is a four layer *pnpn* device which has three terminals known as the anode, the cathode and the gate. These are shown in figure 11.1a and the circuit symbol is shown in figure 11.1b.

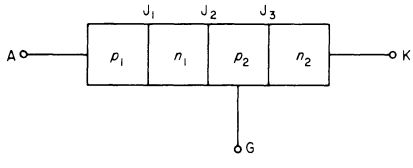


Figure 11.1a

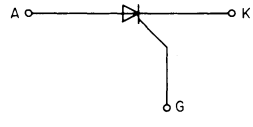


Figure 11.1b

If the thyristor is forward biased (that is, with the anode at a positive voltage with respect to the cathode) junction J_2 is reverse-biased, so that the thyristor is in its blocking state with only leakage current flowing. If the anode-cathode voltage is increased to such a value as to cause the current carriers to produce more carriers by collision, avalanche breakdown of J_2 occurs, and this value of anode-cathode voltage is known as the breakover voltage V_{BO}. A second method of causing breakdown of J_2 at lower anode-cathode voltages, is to inject a small current into the gate terminal. This causes a regenerative action (as the thyristor is effectively composed of a $p_1n_1p_2$ and an $n_2p_2n_1$ transistor: see section 11.2) which produces breakdown of J_2 and a correspondingly high anode current, as the thyristor is now in its conducting state. Once the thyristor has broken down, the gate current can be removed and the anode current will remain high. The only method of bringing the thyristor back to its blocking state is to reduce the anode current below a critical value known as the 'holding' or 'maintenance' current, and this is usually achieved either by reducing the anode-cathode voltage to zero or by making it negative.

When the thyristor is reverse biased, junctions J_1 and J_3 are reverse biased, and only a small leakage current flows until the reverse voltage is large enough to cause avalanche breakdown of junctions J_1 and J_3.

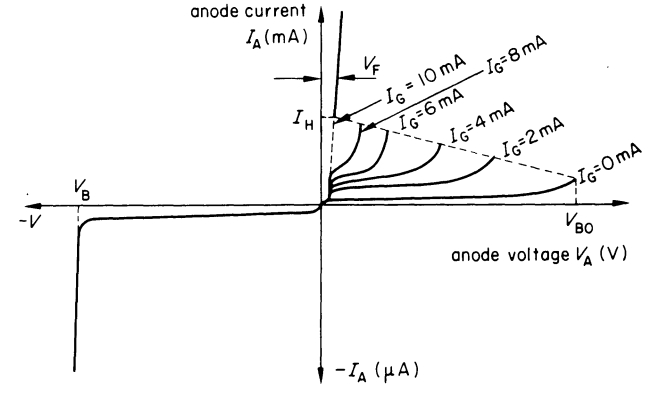


Figure 11.2

Figure 11.2 shows a typical set of anode characteristics for a thyristor. The forward breakover voltage V_{BO} and reverse breakdown voltage V_B can be up to 250 V for thyristors of planar construction, and up to 2000 V for those using a mesa construction, while the corresponding maximum current ratings are 2 A and 1000 A respectively. Note that increasing the forward voltage increases the anode current (mA) slightly until breakover occurs. I_H is the holding current, and this can be as low as 20 mA for small thyristors. V_F, which can be as low as 1 V, is the forward voltage-drop across the thyristor when it is in the conduction state. Note that V_{BO} drops with increasing gate current, blocking ceasing when I_G = 10 mA; after which the thyristor acts as a diode.

Figure 11.3 shows the basic circuit diagram of a single thyristor controlling a unidirectional load current. On the positive half-cycle of the input voltage, the thyristor will fire at some value V_{BO} corresponding to the gate current I_G. On the negative half-cycle, the thyristor will block. Hence, the output will be pulses of voltage, each pulse being a fraction of one half-cycle.

The main advantage of this method is its simplicity. The series

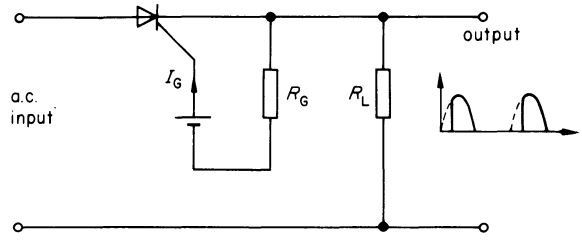


Figure 11.3

resistor R_G must be included, however, so that the maximum gate-cathode power is not exceeded. Also, the thyristor can be fired only in the first half of the positive half-cycle; that is, the maximum firing angle is 90°.

11.2 Two-transistor analogy of thyristor and a.c. control of gate

(a) Using the two-transistor analogy of the thyristor, determine an expression for the forward current of the device. Hence, state the condition for the thyristor to switch from the blocking to the conduction state.

(b)

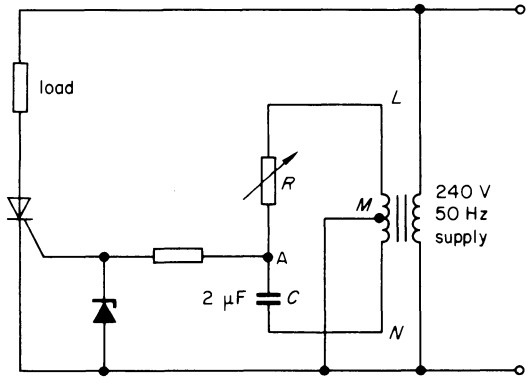


Figure 11.4

Figure 11.4 shows a thyristor employing a.c. phase-shift control on its gate. Determine the firing angle when R = 1000 Ω, proving any formulae used. State the purpose of the Zener diode in this circuit.

(H.N.C.)

(a) The two-transistor analogue of the thyristor is shown in figure 11.5.

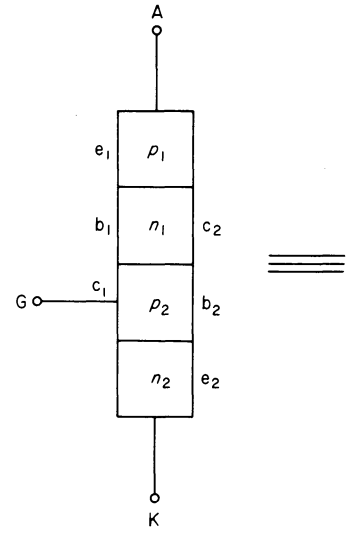


Figure 11.5a

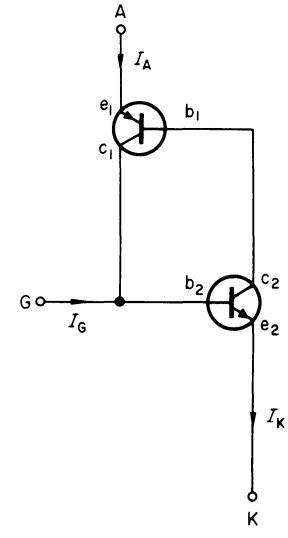


Figure 11.5b

From this

$$I_{B_1} = (1 - \alpha_1)I_A - I_{CBO_1} \qquad (11.1)$$

where α_1 is the common-base current gain of the $p_1n_1p_2$ transistor and I_{CBO_1} is the corresponding leakage current.

$$I_{C_2} = \alpha_2 I_K + I_{CBO_2} \qquad (11.2)$$

where α_2 is the common-base current gain of the $n_2p_2n_1$ transistor and I_{CBO_2} is the corresponding leakage current.

But

$$I_K = I_A + I_G$$

and

$$I_{C_2} = I_{B_1}$$

therefore equating equations 11.2 and 11.1

$$\alpha_2 I_A + \alpha_2 I_G + I_{CBO_2} = (1 - \alpha_1)I_A - I_{CBO_1}$$

that is

$$I_A = \frac{\alpha_2 I_G + I_{CBO_1} + I_{CBO_2}}{1 - \alpha_1 - \alpha_2}$$

Thus when $(\alpha_1 + \alpha_2) = 1$, I_A will tend to infinity. In practice, this corresponds to the conduction state of the thyristor. Usually, the critical condition is brought about by increasing the current gain α_2, which increases with increase of the current density at junction J_2. This is increased when gate current is injected, and thus causes the thyristor to breakover.

(b) In the circuit of figure 11.4, the phase of the voltage at point A shifts through 180° as R is varied from infinity down to zero.

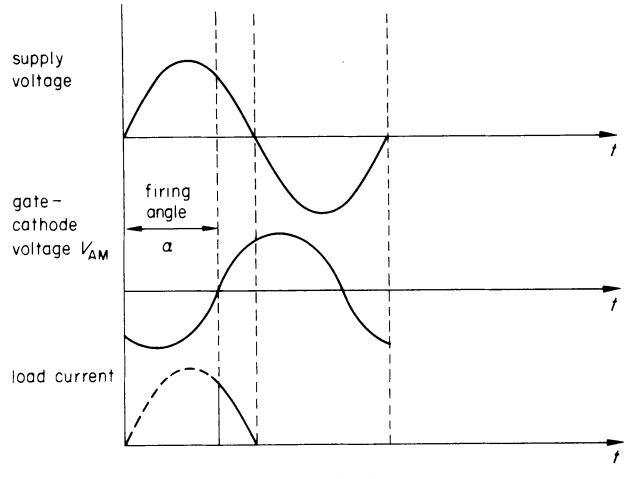


Figure 11.6

Figure 11.6 shows sketches of the supply voltage, gate-cathode voltage, and load current, for a given firing angle α. By varying R from zero to infinity, α can be varied from 0° to 180°. At 180°, the thyristor never fires, and the circuit is said to be fully phased-back.

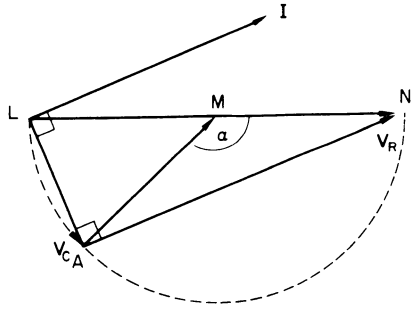


Figure 11.7

Figure 11.7 shows the phasor diagram of the phase-shift circuit (neglecting the loading effect of the gate circuit). As V_R and V_C are always mutually at right angles, the locus of point A is a semi-circle of diameter LN. The firing angle α is the phase shift of V_{AM}. From figure 11.7

$$\angle \text{LMA} = (180 - \alpha)$$

$$\angle \text{MLA} = \angle \text{MAL (isosceles triangle)}$$
$$= \alpha/2$$

Therefore in triangle LAN

$$\tan \alpha/2 = V_R/V_C = IR/IX_C = R/X_C = \omega CR$$

therefore

$$\alpha/2 = \tan^{-1} \omega CR$$

or

$$\alpha = 2 \tan^{-1} \omega CR = 2 \tan^{-1} 2\pi 50 \times 2 \times 10^{-6} \times 10^3$$
$$= 64°$$

The Zener diode protects the gate-cathode junction from excessive forward voltages on the positive half-cycle and on the negative half-cycle shunts the current from the cathode gate circuit.

11.3 Thyristor inverse parallel a.c. controller

Sketch a typical thyristor characteristic and hence explain the meaning of the terms (a) forward breakover voltage; (b) reverse breakdown voltage; (c) maintenance current.

Draw the basic circuit diagram for a phase-controlled inverse parallel a.c. controller. Such a controller is used to supply a resistance furnace of 10 Ω resistance from a 400 V r.m.s. supply. Calculate the power supply to the furnace if the delay angle is 90°.

(ET5)

The first part of this question has been answered in section 11.1.

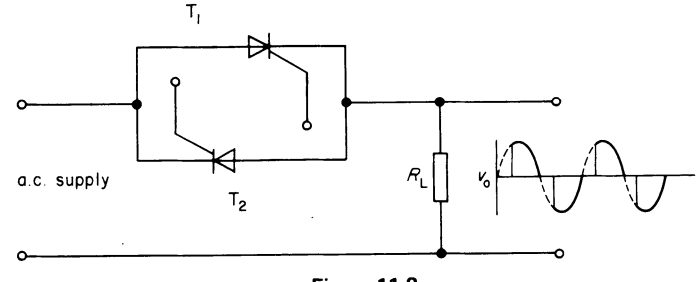


Figure 11.8

Figure 11.8 shows the circuit diagram of a phase-controlled inverse parallel a.c. controller using two thyristors. The gate waveforms to T_1 and T_2 will be exactly 180° out of phase: on the positive half-cycle of the input voltage, T_1 fires at an angle θ°; while on the negative half-cycle, T_2 fires at an angle $(180 + \theta)$°, giving the output waveform shown.

r.m.s. load voltage

$$V_{r.m.s.} = \left[(1/\pi)\int_{\pi/2}^{\pi} 400\sqrt{(2)}\sin\omega t\, d^2(\omega t)\right]^{1/2}$$

$$= 400\left[(1/\pi)\int_{\pi/2}^{\pi}(1-\cos 2\omega t)\, d(\omega t)\right]^{1/2}$$

$$= 400/\sqrt{2} \text{ volts}$$

Power supplied to the furnace

$$P = \frac{1}{10}\left(\frac{400}{\sqrt{2}}\right)^2$$

$$= 8 \text{ kW}$$

11.4 Pulse firing of thyristors

Give reasons why pulse firing of controlled rectifiers is often preferred to other methods.

Draw the diagram of a circuit which will produce a delayed pulse or pulse train suitable for firing a silicon-controlled rectifier and explain how the circuit operates.

Sketch a curve showing how the average output voltage of a controlled rectifier system varies with firing delay angle. Explain the shape of the curve.

(ET5)

Pulse firing of silicon-controlled rectifiers has the following advantages

(1) The thyristor may be fired anywhere in the positive half-cycle of anode supply.

(2) The thyristors may be coupled to the gate circuit by a transformer, so that

(a) electrical isolation is provided between the power side and the control circuitry;

(b) several gate circuits can be supplied simultaneously;

(c) pulses in one direction may fire one thyristor while pulses in the opposite direction may fire another.

(3) Pulse powers can be very high, so ensuring reliable firing of the thyristor under all conditions and allowing for a decrease in the output of the firing circuit because rated gate power dissipation is determined by the average power supplied.

(4) A chain of pulses may be generated and synchronised to the anode supply, when a continuous firing signal is required.

(5) Pulses have fast rise-times, and are thus ideal waveforms for firing thyristors.

Circuits whose outputs are ideal for firing thyristors include the astable multivibrator and the blocking oscillator, and these have already been examined in chapter 8.

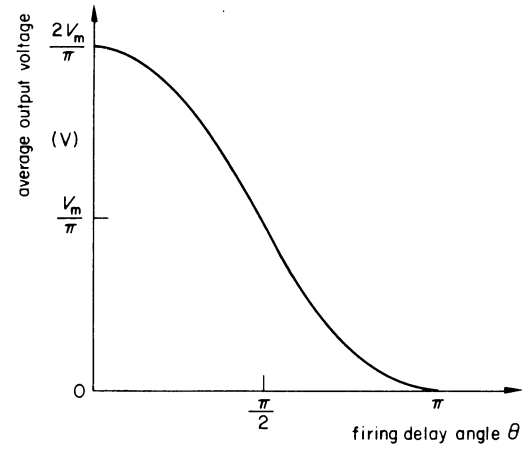


Figure 11.9

Figure 11.9 shows a sketch of the graph of average output-voltage against firing-delay angle. To explain the shape of this, consider its equation

$$V_{av} = (1/\pi)\int_{\theta}^{\pi} V_m \sin\omega t\, d(\omega t)$$

$$= (1/\pi)_{\theta}^{\pi}[-V_m\cos\omega t]$$

$$= V_m(1+\cos\theta)/\pi$$

where θ is the firing-delay angle. Hence the graph is that of $\cos\omega t$ against ωt with each point on it lifted by 1.

11.5 Thyristor speed-control

(a) With the aid of a circuit diagram, explain how thyristors can be used to control the speed of a d.c. series motor.

(b) A thyristor has the relationship $V_{BO} = 480 - 20I_G$ between the breakover voltage V_{BO} volts and the d.c. gate current I_G mA. If this thyristor is employed in the circuit of figure 11.10, derive an expression for the mean load current and hence calculate

its maximum and minimum values and the corresponding values of I_G. What are the main limitations of using the device in the circuit shown?

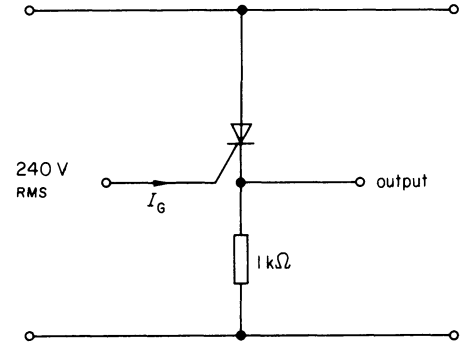


Figure 11.10

(H.N.C.)

(a) Figure 11.11 shows a circuit for speed control of a d.c. series motor; the motor takes negligible current until the thyristor fires.

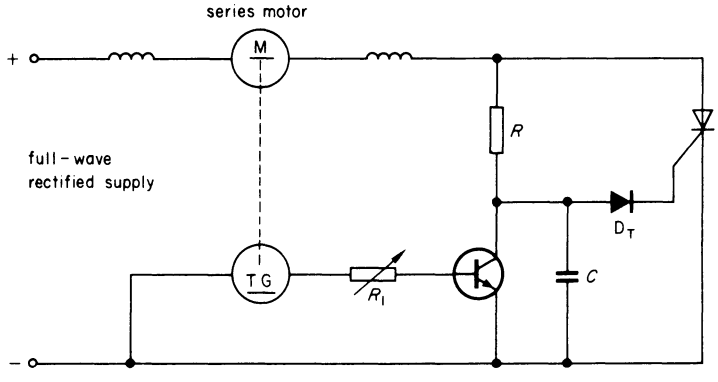


Figure 11.11

Firing takes place when the capacitor C has charged high enough to drive sufficient gate current through the trigger diode D_T and the gate-cathode circuit to cause breakover. Note that the charging time of the capacitor depends upon how hard the transistor conducts; which, in turn, depends upon the base current, and hence upon the setting of R_1. R has little effect on the charging rate as the collector voltage of the transistor has little effect on the collector-current after conduction has commenced.

If it is required to maintain a constant-speed drive, feedback through the tachogenerator is used. If the load increases and the motor speed tends to fall, the output voltage from the tachogenerator falls, the transistor base and collector currents decrease, and thus there is more charging current available for the capacitor. It therefore charges to the critical value faster, and the thyristor fires earlier in the cycle, thus increasing the voltage supply to the motor and restoring the speed to its original level.

(b) Mean current taken is

$$I_{\text{d.c.}} = \frac{1}{2\pi}\int_{\omega t}^{\pi} \frac{240\sqrt{2}\sin\omega t}{1000}\,\text{d}(\omega t)$$

$$= 120\sqrt{2}(1+\cos\omega t)/\pi \text{ mA} \qquad (11.3)$$

The thyristor breaks over when

$$V_{BO} = 240\sqrt{2}\sin\omega t = 480 - 20I_G \qquad (11.4)$$

The maximum current occurs when $\cos\omega t = 1$ or $\omega t = 0$.

From equation 11.4, the corresponding gate current $I_{Gmax} = 24$ mA. From equation 11.3, the minimum load current = $120\sqrt{2}/\pi$ = 54 mA. The limitations of d.c. gate control have been dealt with in section 11.1.

11.6 Spurious firing of thyristors

Describe in detail the two methods by which a thyristor is triggered spuriously in practice and hence state typical precautions taken to prevent these kinds of triggering.

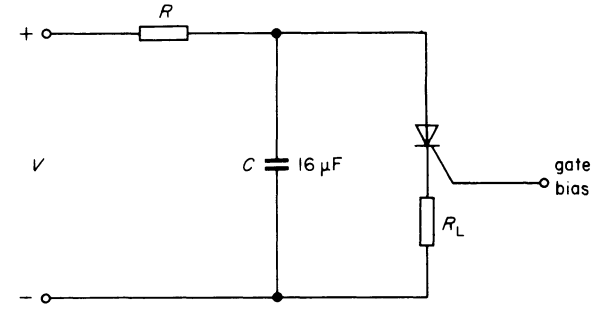


Figure 11.12

Figure 11.12 shows a thyristor with a fixed bias connected across a capacitor C, which is allowed to charge up via a large valued resistor R. The bias is arranged so that the rectifier fires when the voltage across the capacitor is 150 V and stops conducting when

the capacitor voltage is 75 V. Derive an expression for the power dissipated in R_L in each operation and calculate its value when R_L = 100 Ω, stating any assumptions made.

(H.N.C.)

It has been shown in section 11.2 that for a thyristor to be triggered into the high-conduction region

$$\alpha_1 + \alpha_2 = 1$$

This condition is brought about in practice by increasing the current across J_2 as the current gain α_2 increases with it.

If the thyristor is blocking and there is a voltage transient on the supply (that is, a voltage rise that is rapid, though the actual size of the change may be small), a charging current will flow through the internal junction capacitances, and this current can make $\alpha_1 + \alpha_2 = 1$ and trigger the thyristor. To prevent this, a series resistor-capacitor combination is connected in parallel with the thyristor to reduce the rate of increase in anode voltage and thereby make the charging current negligibly small.

Similarly, if the temperature of the thyristor is increased, the leakage current (which increases exponentially with temperature) can increase to such a level as to make $\alpha_1 + \alpha_2 = 1$ and thus to trigger the thyristor. To prevent this, adequate cooling must be provided; and this may be either in the form of a heat sink for the smaller thyristors, or of forced air or water cooling for the high-rated thyristors.

Energy stored in a capacitor = $0{\cdot}5CV_1^2$, where V_1 is the voltage across the capacitor C. If the capacitor discharges through resistor R_L to V_2 volts in t seconds, energy loss from the capacitor = $0{\cdot}5(V_1^2 - V_2^2)$. Therefore power dissipation in resistor R_L in this time is

$$P = 0{\cdot}5C(V_1^2 - V_2^2)/t \qquad (11.5)$$

In the following analysis assume that thyristor switching actions occur instantaneously and that the forward voltage-drop across the thyristor is negligible. Then time taken for C to discharge from 150 V to 75 V is

$$75 = 150 \exp(-t/16 \times 10^{-6} \times 100)$$

$$625t = \log_e 2$$

$$t = 1{\cdot}11 \text{ ms}$$

Substituting in equation 11.5

$$P = \frac{0{\cdot}5 \times 16 \times 10^{-6}(150^2 - 75^2)}{1{\cdot}11 \times 10^{-3}}$$

$$= 121{\cdot}6 \text{ W}$$

11.7 Triac theory and application

What is a triac? Sketch a set of I/V characteristics for a triac and explain its operation.

Explain with the aid of a circuit diagram how a triac can be used to control the current through an a.c. load.

A triac is a four layer *pnpn* device having the circuit symbol shown in figure 11.13.

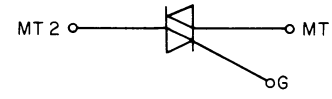


Figure 11.13

MT2 is known as main terminal 2 (corresponds to the anode of a thyristor) and is normally the case of the device. MT1 is main terminal 1 (corresponds to the cathode) and G is the gate. Triacs can be designed to turn on with either polarity of gate to MT1 voltage and with either polarity of applied voltage between MT1 and MT2. Thus, it can conduct large currents in either direction, and it is similar to two thyristors operating in inverse parallel connection.

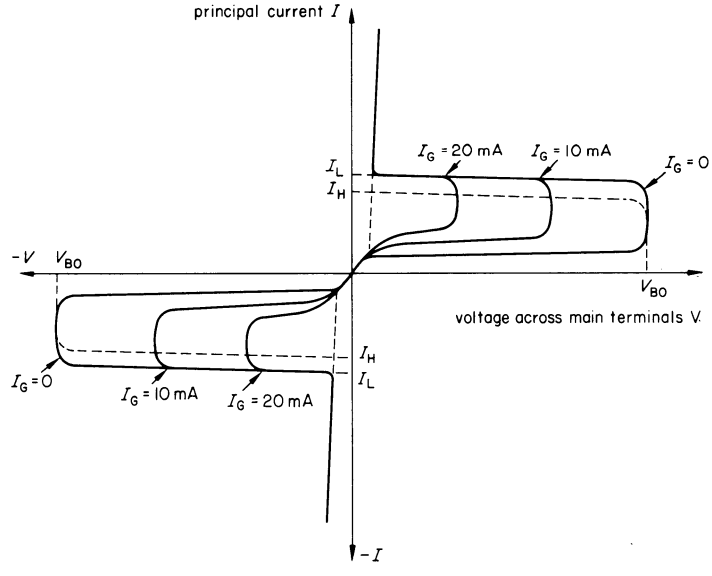


Figure 11.14

Figure 11.14 shows a typical set of *I/V* characteristics for a triac. Note that, as with the thyristor, a high breakover voltage is

required in the forward direction with no gate current applied. The situation in the reverse direction is approximately the same: as the gate current is increased, the breakover voltage decreases. However, in this direction, the gate current must be maintained until the principal current exceeds a critical value I_L, which is known as the *latching current*. Once this value is exceeded the gate current can be removed, as the triac is then in its high conduction state and will remain so until the principal current falls below a second critical value I_H which is lower than I_L and is known as the *holding current*. The reverse characteristics are nearly identical. Triacs are normally of a mesa construction and have ratings up to 200 A, 1000 V.

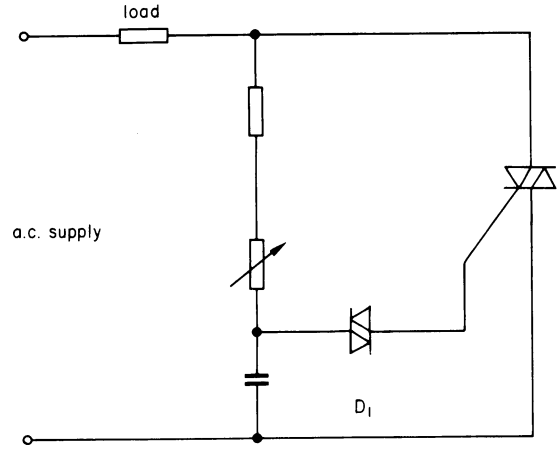


Figure 11.15

Figure 11.15 shows a simple circuit for controlling the a.c. current through the load. The trigger circuit that is used depends mainly upon the application to which the triac is being put. The essential point is that the gate turn-on current and the latching current must both have minimum levels. As there is a spread in gate turn-on currents, a bidirectional diode (*diac*) is used to ensure that the triac conducts at the same value of supply voltage each time. The diac detects both polarities, and provides a voltage threshold that must be overcome before gate current can flow. Note that, in this circuit, gate current is positive when MT2 is positive and negative when MT1 is negative, so that the possibility of positive gate current with negative MT2 (which is an undesirable operating mode) is eliminated. The triac will turn off each time the principal current goes through zero and the gate will regain control.

11.8 Exercises

Exercise 11.1

Explain briefly the basic principles of operation of a controlled semiconductor rectifier (thyristor).

Describe two advantages in triggering the gate with voltage pulses and explain why a train of pulses may be required for each cycle of anode supply when the load is inductive.

(ET4)

Exercise 11.2

(a) Explain with the aid of a sketch and suitable graphs, the principle of operation of a silicon controlled rectifier.

(b) Draw a circuit diagram of a typical application of a silicon controlled rectifier and explain its operation.

(TT5)

Exercise 11.3

Explain in detail the principle of operation of a silicon controlled rectifier and describe with the aid of circuit diagrams at least two different practical applications.

(I.E.R.E.)

Exercise 11.4

A thyristor has the relationship $V_b = 500 - 20/_g$ between the breakdown voltage V_b and the gate current I_g mA.

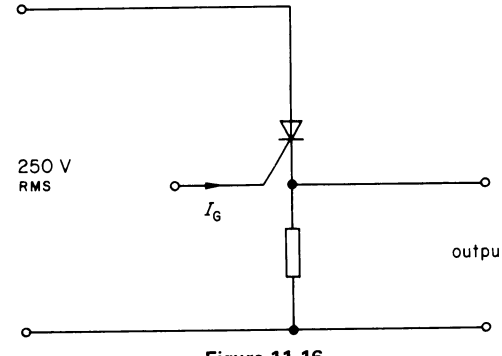


Figure 11.16

This thyristor is employed in the circuit of figure 11.16. Derive an expression and plot a graph showing how this current varies with the gate current I_g. What are the main limitations of using this device in the circuit of figure 11.16?

(I.E.R.E.)

Exercise 11.5

Show with the aid of a circuit diagram how a rectifier bridge and a silicon controlled rectifier can be used to regulate the alternating current through a load resistor R_L when the input to the bridge is a sinusoidal voltage. Briefly mention any advantages and disadvantages of the method of gating used for the silicon controlled rectifier.

Devise an expression for the r.m.s. current in the load resistor R_L in terms of the silicon controlled rectifier firing angle. Plot a graph of the current in R_L against the rectifier firing angle.

(I.E.R.E.)

Exercise 11.6

Sketch an *I/V* characteristic of a triac, indicating typical voltage and current values.

(U.L.C.I.)

Exercise 11.7

(a) Draw a circuit diagram to show how two thyristors may be used to provide full-wave rectification using either (i) a biphase arrangement or (ii) a bridge circuit arrangement. Indicate clearly how the control signal is applied to the gates.

(b) A controlled full-wave rectifier is used to regulate the power dissipated in a resistance furnace. Determine the percentage of maximum possible power delivered to the furnace if the firing angle is delayed by 45°.

(c) What would be the effect on the load-voltage waveform of highly inductive resistors in the furnace?

(Answer: 90·9 per cent) (ET5)

Exercise 11.8

(a) A single-phase half-wave controlled rectifier is to be used to regulate the current through a resistive load of 100 Ω from a sinusoidal supply of 240 V r.m.s. Determine the average load current if conduction is delayed by 90°.

(b) If this resistive load is exchanged for an inductive load having a resistance of 100 Ω, sketch typical waveforms of load current and voltage to a common time-scale and for the same conduction angle. What protective device is normally added to this circuit?

(c) Sketch a circuit diagram showing how the gate of a thyristor can be a.c. controlled from the anode supply. State the theoretical limits of the range of conduction angle.

(Answer: 0·54 A)

(ET4)

12 Photoelectric devices and solid state manufacturing techniques

12.1 Photoemissive cell and control circuit

Sketch a circuit diagram of a simple alarm circuit incorporating a photoemissive cell operating from a d.c. supply. Sketch the characteristics, on suitably labelled axes, of the cell used in the circuit.

Explain the operation of the circuit and show how an indication of supply voltage failure may be obtained.

(ET4)

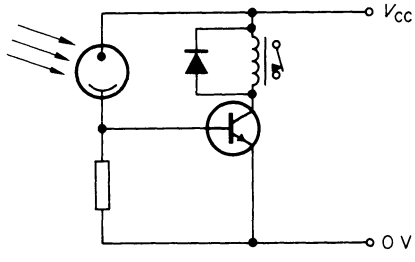


Figure 12.1

Figure 12.1 shows a simple alarm circuit employing a photoemissive cell being used to control the base current of a transistor. When the light shines on the cell, the base current is high enough to cause a sufficient collector current flow to energise the relay; but as the alarm circuit uses a normally-closed contact, no alarm is given. When the light reaching the photocell is interrupted however, the base current and collector current fall considerably, thus de-energising the relay and operating the alarm. The diode is used to protect the transistor from the voltage spikes that are caused by the inductive load when the transistor switches off.

Figure 12.2 shows the characteristics of a vacuum photoemissive cell. As can be seen, after the initial rise of anode current further increase in anode voltage has negligible effect on the current, but changes in incident light on the photocell cause a relatively large change in anode current. If a gas-filled cell is used, the same currents can be achieved by smaller amounts of light. Larger anode currents, however, are not possible as they would cause damage to

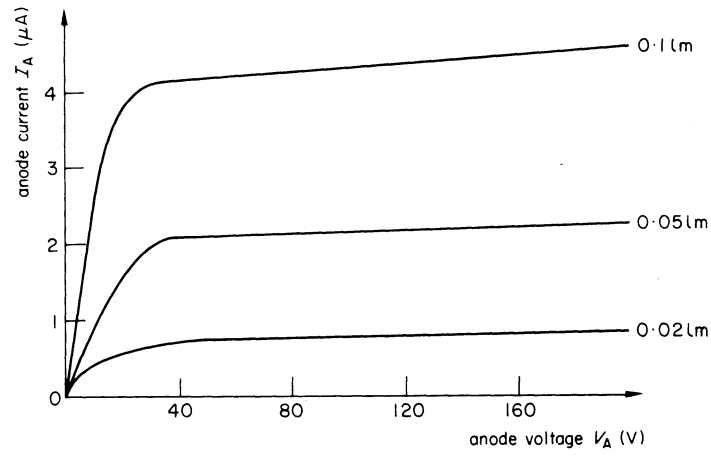


Figure 12.2

the cathode because of positive ion bombardment. Note that in this circuit if the supply voltage fails, the contacts will close, and the alarm will be raised; hence, this is a fail-safe system.

The cathode of a photoemissive cell emits electrons when light falls upon it. A common material used for such a cathode is caesium-antimony, which is sensitive to all visible wavelengths except the far red ones. The cathode is normally made in the shape of a half-cylinder, and the anode is in the form of a metal rod which is of small diameter so that it does not interrupt the light falling on the cathode. In some cells the anode may consist of a length of wire in the shape of a loop or rectangle which is placed in front of the cathode. Both anode and cathode are then enclosed in a single evacuated tube.

12.2 Photoconductive cell and photodiode

Describe the construction and principle of operation of either (a) a photoconductive cell or (b) a photodiode.

Sketch the current/voltage characteristics of the cell described and show how it can be used to control the collector current of a transistor in a simple counter circuit. What simple precaution is necessary when using a relay as a collector load?

(ET4)

Figure 12.3a shows the construction of a photoconductive cell and figure 12.3b shows the corresponding circuit symbol. The photoconductive materials most commonly used are cadmium sulphide and cadmium selenide; the former has a spectral response

Figure 12.3a

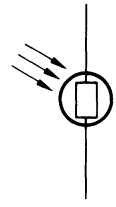


Figure 12.3b

similar to that of the human eye, and the latter has one that matches the light output of an incandescent lamp or neon discharge tube. When light falls on the photoconductive material, which is a semiconductor, the energy contained in the light breaks more of the covalent bonds, thereby causing the formation of more hole-electron pairs. The overall effect is an increase in the conductivity of the cell as a result of the decrease in its electrical resistance. The semiconductor material is deposited on an insulating substrate with the electrodes evaporated on to its surface through a mask, and the whole is then enclosed in an evacuated glass envelope. The meandering pattern of the semiconductor film is used to increase the cross-sectional area available in the limited length, thereby decreasing the resistance of the cell and allowing a higher current and power rating. The *dark* resistance of the cell can be up to 10 MΩ, reducing in daylight to less than 1 kΩ. Typical characteristics are shown in figures 12.4a and 12.4b.

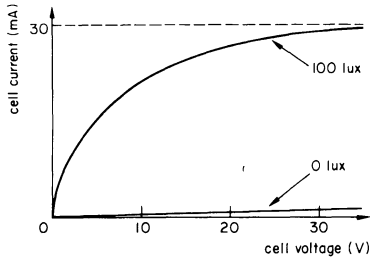


Figure 12.4a

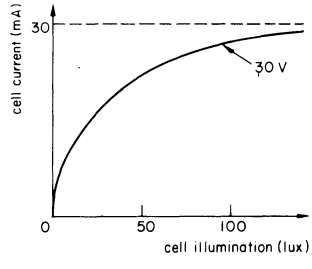


Figure 12.4b

Figure 12.5 shows a simple circuit for operating a counter, alarm system, automatic street-lighting control, or any similar process.

When light falls on the cell, the transistor base current is high; hence the transistor collector current is also high and the relay is energised, thereby opening its normally-closed contacts. When the light is interrupted, the base and collector currents fall, and the

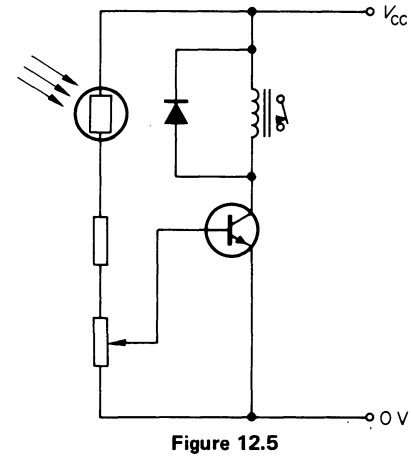


Figure 12.5

de-energised relay recloses its contacts, thereby operating the counter. The diode across the relay coil is used to prevent the back e.m.f. from the coil damaging the transistor. The advantages of the type of cell used in figure 12.5 are (1) high sensitivity, (2) high power rating, (3) non-polarisation, (4) robust construction, (5) low cost, (6) good response to infra-red light.

The construction of a photodiode is similar to the conventional *pn* diode, except that the diode outer casing is left transparent near the junction, so that light may fall on the junction. The photodiode is always reverse-biased so that the only current flowing is the leakage current, and this is about 10 μA for a germanium diode. When light falls upon the junction, more hole-electron pairs

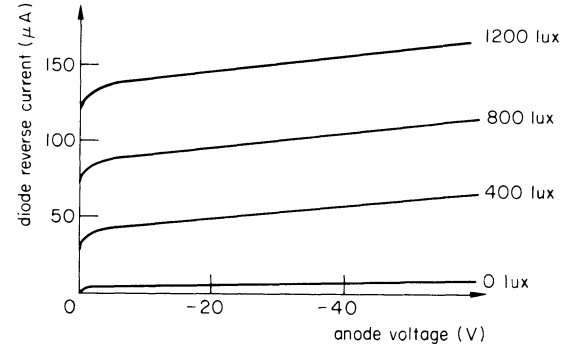


Figure 12.6a

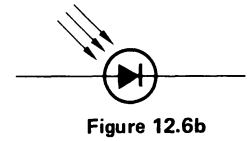


Figure 12.6b

are formed and the leakage current increases. Typical characteristics for a photodiode at constant temperature are shown in figure 12.6a and the appropriate symbol is shown in figure 12.6b. This photodiode could replace the photoconductive cell in figure 12.5 and the circuit would operate in a similar manner.

12.3 Photovoltaic cell and control circuit

(a) Describe the principle of operation of a photovoltaic cell and sketch a typical current/illumination curve.

(b) The circuit outlined in figure 12.7 shows how this type of cell may be used as part of an on/off circuit. Explain how the circuit functions and describe two of the factors governing the choice of R_1.

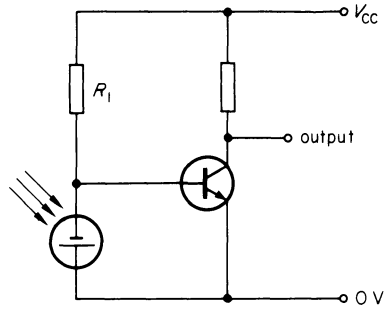


Figure 12.7

(ET4)

(a) Silicon photovoltaic cells consist of a thin piece of *n*-type silicon into which a *p*-type impurity is diffused to a depth of between 0·5 and 1 μm. This shallow layer allows light to fall on the *pn* junction with negligible loss in energy. If no external bias is applied to the *pn* junction, hole–electron pairs are formed when light falls on the junction region. The holes so formed diffuse into the *p*-type material and the electrons into the *n*-type material. These extra majority carriers on each side of the junction cause the electrode attached to the *p*-type to become positive with respect to the electrode connected to the *n*-type; that is, an e.m.f. is generated across the terminals. When an external load is connected across the terminals, the photovoltaic e.m.f. tends to fall.

Figure 12.8a shows a typical current/illumination curve and figure 12.8b shows typical current/voltage characteristics.

(b) In the circuit of figure 12.7, when light is falling on the cell, the photovoltaic e.m.f. is sufficient to bias the base negatively, thereby cutting off the transistor and giving an output voltage of

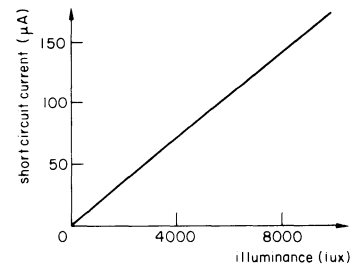


Figure 12.8a

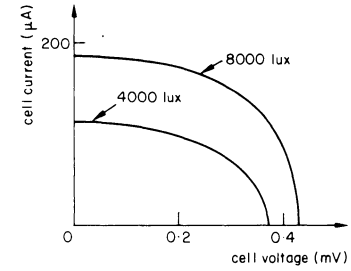


Figure 12.8b

V_{CC}. When no light falls on the cell, the base will be biased positively and the transistor will saturate, thus giving an approximately zero output-voltage.

When the transistor is cut off, R_1 must have a high value so as to limit the current flow through the cell and so keep the base of the transistor negative. However, when light does not fall on the cell, R_1 must have a value low enough to permit the flow of sufficient base current to saturate the transistor.

12.4 Phototransistor and light-emitting diode

(a) Describe the principle of operation of a phototransistor and sketch a typical set of current/voltage characteristics.

(b) Describe the construction and principle of operation of a light-emitting diode (LED) and state practical applications of this device.

(a) A phototransistor has essentially the same construction as a normal transistor, but it is designed so that light can fall on to the base region. Most modern phototransistors are silicon planar transistors, as their performance is far less dependent on temperature than is that of germanium transistors.

In the *npn* phototransistor, the collector is biased positively with respect to the emitter so that the base-collector junction is reverse-biased. Thus, when no light falls on the base, only normal leakage current flows, and this is very small. However, when light falls on the base, more hole–electron pairs are formed in this region, and the current arising from these is amplified by transistor action.

Figure 12.9a shows the current/voltage characteristic of a phototransistor, for which the circuit symbol is shown in figure 12.9b. Hence, a relay coil can be used as the collector load of this device to give a simple light-activated system that can be used either as an alarm or for counting.

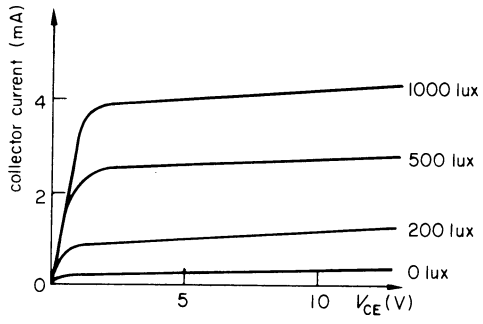


Figure 12.9a

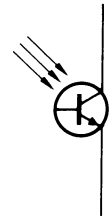


Figure 12.9b

(b) There are two main types of semiconductor *pn* light-sources: gallium arsenide, which emits infra-red light; and gallium arsenide-phosphide (GaAsP) which emits visible light. The principle of operation of these devices is that in any forward-biased junction diode, recombination of holes and electrons occurs at the junction when forward current flows. When a hole-electron recombination occurs, the energy released by the electron returning to the valence band appears as a quantum of electromagnetic radiation. The frequency of this radiation is determined by the width of the forbidden-energy gap between the highest valence band and the lowest conduction band. The semiconductor must have an energy gap between 1·5 and 3 eV for visible light emission. If the gap is narrower than 1·55 eV, infra-red emission will occur. To enable light to escape from the device special geometries have to be employed in manufacture if the bulk of the material is not to re-absorb it. Basically, this means providing a large junction area and arranging the emitting surface so that total internal reflection does not occur. This is not easy with the high refractive-indexes of most semiconductors.

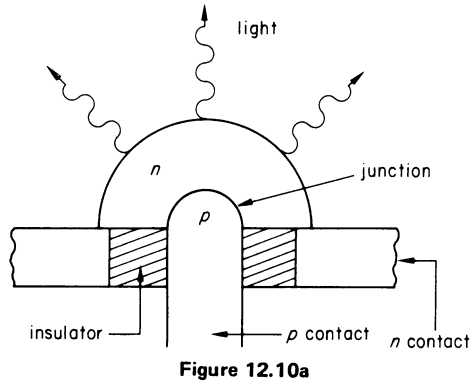


Figure 12.10a

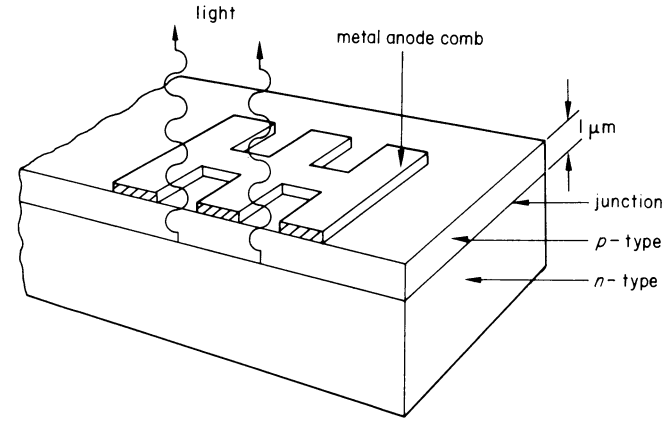


Figure 12.10b

Figures 12.10a and 12.10b show two types of LED structure which have been used in practice to allow the light to escape.

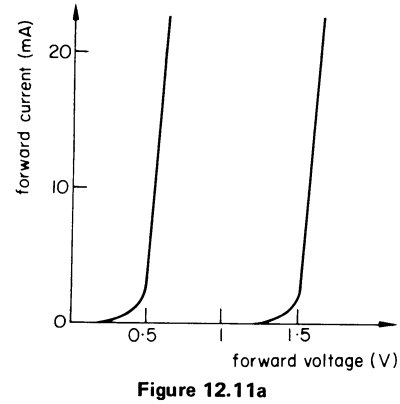


Figure 12.11a

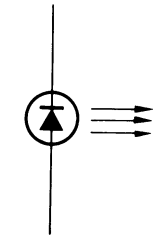


Figure 12.11b

Figure 12.11a shows the characteristics of a silicon diode and an LED, the only difference being that the forward-voltage drop of an LED is about 1·6 V. The symbol for the LED is shown in figure 12.11b.

The most common application of LEDs is in alpha-numeric readouts where they are arranged in a *dot matrix* or *bar matrix* to form the figure or character. They are normally laid out on a single slice of semiconductor material, the whole chip being then enclosed in a package similar to an integrated circuit, except that the packaging compound is transparent.

The advantages of LED readouts are (1) small size (typically 5 mm), (2) long life, (3) high reliability, (4) compatibility with all types of drive circuit, (5) ability to run from a large range of

supply voltages from 2 V upwards. Difficulty in reading from distances of more than two or three metres is one possible disadvantage, and another is the fact that at present the cheapest devices emit only red light, so there is a consequent increase in cost if amber or green is required.

12.5 Alloy-junction and planar transistors

(a) Describe with a sketch the construction of either (i) a planar transistor or (ii) an alloy junction transistor.

(b) State four differences in the electrical properties between (i) a germanium alloy-junction transistor and (ii) a silicon planar epitaxial transistor of comparable size. Why is silicon used more than germanium in the construction of modern transistors?

(ET4)

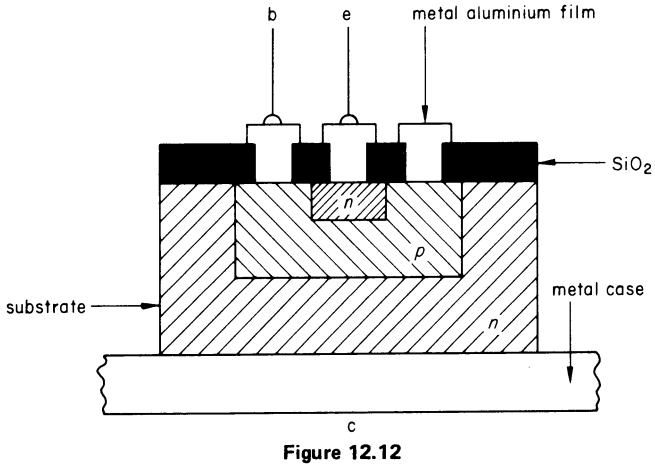


Figure 12.12

(a) Figure 12.12 shows the construction of a silicon planar transistor. To manufacture this, a polished slice of *n*-type silicon (substrate) is put into a furnace in which the temperature is approximately 1200°C and steam is passed over it for several hours. This causes a layer of silicon dioxide (SiO_2) to be formed on the surface. A window is then cut through this SiO_2 layer by a photochemical process. The surface is first coated evenly with a photoresist liquid which has the property of hardening when exposed to ultraviolet light. A mask is next placed on the surface to prevent the ultraviolet light from reaching the area required for the base, and the slice is then exposed to the ultraviolet light. The surface is now washed to remove the unhardened photoresist and the SiO_2 layer is thereby exposed in the base area; after which, the remaining photoresist is further hardened by baking the slice. A strong acid is now used to etch away the exposed area of SiO_2 to provide direct access to the silicon, and then the remainder of the hard photoresist is removed from the slice.

The slice is again placed in an oven, this time with a trivalent impurity, usually boron, that evaporates and diffuses into the exposed portion of the silicon to the required depth of three or four micrometres to form the *p*-type base region. A new SiO_2 layer is next formed over the slice. The whole photolithographic process is then repeated with a suitable mask to form the *n*-type emitter region, but this time using an impurity of the pentavalent type, usually phosphorus; and a further SiO_2 layer is then formed over the slice.

The process is repeated yet again to etch windows through the SiO_2 layer to the base and emitter, and a thin layer of aluminium wire is then alloyed to these regions. Finally, fine gold or aluminium wire is connected to each aluminium layer to form the transistor leads. The whole transistor is then encapsulated in a metal case, which is often in direct electrical contact with the collector.

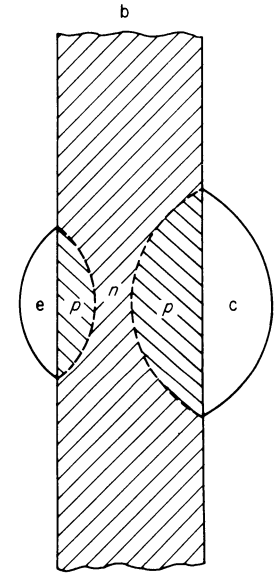


Figure 12.13

The construction of the alloy-junction transistor is shown in figure 12.13. This method is normally used for germanium *pnp* transistors. Two pellets of trivalent material, usually indium, are placed in a jig on each side of an *n*-type germanium wafer of

typical dimensions 3 x 15 x 0·3 mm. The collector pellet is normally about three times larger than the emitter pellet. The whole assembly is then heated to about 500°C. The indium melts and dissolves some germanium from the wafer, which is then allowed to cool and recrystallise. Hence, two regions of *p*-type material are formed as shown. Finally, connections are made to both regions; the base connection is made to a nickel tab that has been previously bonded to the base region during the heating process; and the whole assembly is then encapsulated.

(b) Silicon transistors have the following advantages over germanium transistors

(1) lower leakage currents;

(2) higher reliability as the SiO_2 layer prevents the ingress of dirt or moisture to the pellet over a long period;

(3) higher operating frequencies, above 1 GHz;

(4) the planar process is well suited to mass-production techniques and allows much closer tolerances to be obtained;

(5) higher current gains are possible with the planar process;

(6) lower noise factors.

Silicon is used more than germanium in the planar process because germanium does not readily lend itself to this process, only low yields of transistors being obtainable and these of relatively low current gains.

12.6 Construction of planar epitaxial transistor

Describe the steps taken in constructing a silicon npn epitaxial planar transistor, using sketches as necessary. Briefly explain why this transistor will have the following electrical properties

(i) high collector-to-emitter breakdown voltage;
(ii) low collector-to-emitter leakage current;
(iii) low collector-to-emitter saturation voltage.

(ET4)

Figure 12.14 shows the construction of a silicon planar epitaxial transistor. In this transistor, a heavily doped n^+ substrate is used, and this acts as a low resistivity foundation. A high resistivity *n* epitaxial layer is then grown as a crystal formation on the substrate in a special reactor, and a *p*-type base region is diffused into the *n* epitaxial layer by the photolithographic process described in section 12.5. The emitter region and the base and emitter contacts are also subsequently formed by the photolithographic process. Note that the transistor is now essentially contained in the epitaxial

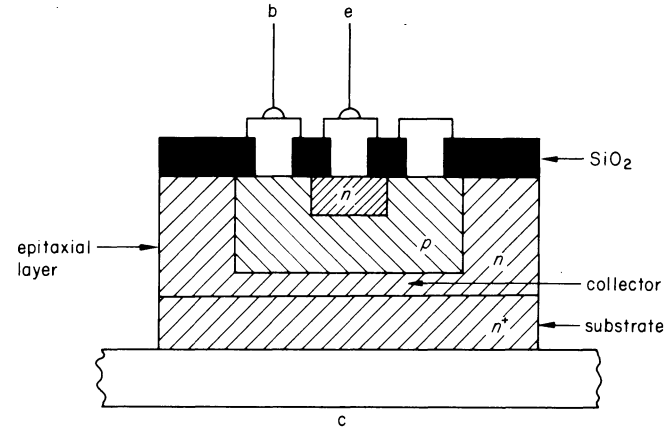


Figure 12.14

layer, and that the substrate is no more than a low-resistance back contact to take the mechanical stress that would otherwise be borne by the thin collector-region. Note also that practical dimensions for the thickness of substrate, epitaxial layer, and collector are respectively 200 μm, 10 μm and 5 μm.

In the planar epitaxial transistor, the epitaxial layer makes possible two normally-conflicting requirements (1) a high collector-to-emitter breakdown voltage resulting from the high collector resistivity; (2) a low collector-to-emitter saturation voltage resulting from the very low resistance of the thin collector. Also, as the material is silicon, there are relatively few minority carriers in the base region, and the collector-to-emitter leakage current is therefore low.

12.7 Formation of capacitors, resistors and diodes, on an integrated circuit

(a) Explain with appropriate sketches how (i) a capacitor, (ii) a resistor, (iii) a diode can be formed on a silicon slice in the manufacture of an integrated circuit.

(b) Describe any method which can be used to isolate electrically each component on the wafer.

(ET4)

(a) Figure 12.15 shows the construction of a resistor in an integrated circuit. The foundation of the integrated circuit is again a slice of heavily doped *p*-type silicon, about 200 μm thick, which forms the substrate. The additional *n*- and *p*-type regions are then successively diffused into the *p* substrate by the photolithographic process. The final *p*-type region has a high resistivity; and, when

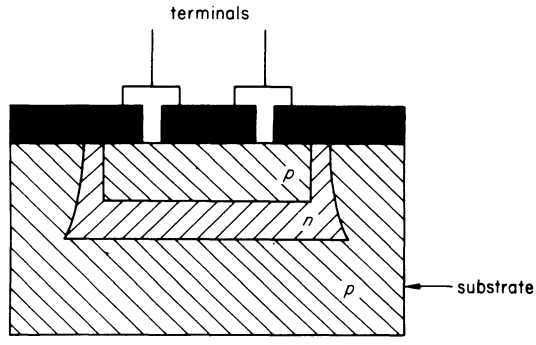


Figure 12.15

contacts are formed at each end of it, a resistor is obtained whose resistance depends on the amount of doping, length and width of the p layer. In practice, there is an upper limit of 50 kΩ which is fixed by the available area. Such resistors have an accuracy of 20 per cent and this is determined by the accuracy with which the width can be defined.

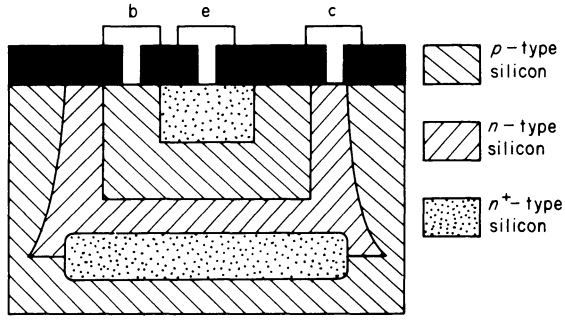


Figure 12.16

Figure 12.16 shows the construction of an integrated circuit bipolar *npn* transistor. The foundation is again the heavily doped p substrate, and the n epitaxial layer is grown on the substrate. The base and emitter regions are again diffused in by the photolithographic process. Note that in this transistor, a heavily doped n^+ *buried* layer is added to the collector in such a way that it shunts the thin collector-layer, thus reducing the effective collector-resistance and allowing very low collector-emitter saturation voltages. An n^+ region may also be diffused into the collector region at the contact terminal in order to give a better contact at the surface.

To form a diode, various p and n regions could be used. However, one main method is to use a transistor with the base and collector contacts connected together to form the p-type anode while the emitter is used as the cathode.

As all practical junction diodes have a finite capacitance, any diode can be used as a capacitor. The diode is reverse-biased to reduce resistive loss and its capacitance value C then depends upon the applied voltage V; approximately, C is proportional to $V^{-\frac{1}{3}}$. Capacitors are often formed by using a transistor with its emitter and collector regions shorted together so that the two transistor-junction capacitances are in parallel. Capacitors are also formed by using the surface oxide as dielectric, with an n^+ region electrode on one side and an aluminium layer electrode on the other. The capacitance per unit area is smaller for this type of capacitor but they have higher operating voltages, and changes in this voltage have negligible effect on the capacitance value.

(b) The most common method of isolating components electrically is to connect the p substrate to the most negative potential in the circuit. In this way, components effectively have a reverse biased diode between each other, and this provides the necessary isolation.

12.8 Enhancement-type MOST and bipolar transistors in integrated circuits

(a) Describe using appropriate sketches how either (i) an enhancement-type MOST or (ii) a bipolar transistor can be fabricated in integrated form.

(b) Briefly explain why high-value resistors and capacitors are not included in monolithic integrated circuitry.

(ET4)

(a) The fabrication of a bipolar transistor has been described in section 12.6.

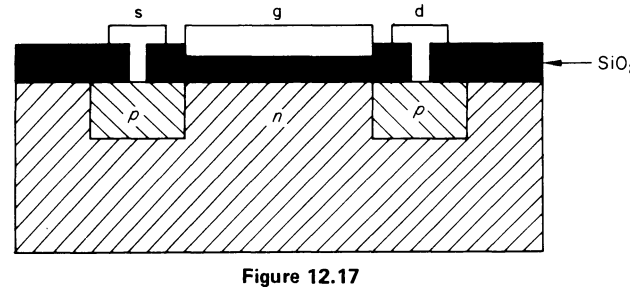


Figure 12.17

Figure 12.17 shows the construction of an integrated circuit p-channel enhancement-type MOST. Note that in this transistor, the source and drain diffusions are made directly into the n-type

substrate. This is possible because, as the channel is induced, no separate isolation diffusion is necessary. The gate isolation is provided by the surface oxide layer, which is carefully grown to an accurate thickness (0·1 μm) as this affects the value of mutual conductance g_{fs}. The photolithographic process is essentially the same as that used in the manufacture of bipolar transistors.

If the MOST has to be used with bipolar transistors on the same chip, the *n* region first has to be diffused into the *p* substrate before the source and drain regions are formed.

(b) High-value resistors are not included in monolithic integrated circuits because of the extra surface area which would be required; the practical limit is about 50 kΩ. To achieve this, practical resistors are often meandered as shown in figure 12.18 in order to provide the required value in as small an area as possible.

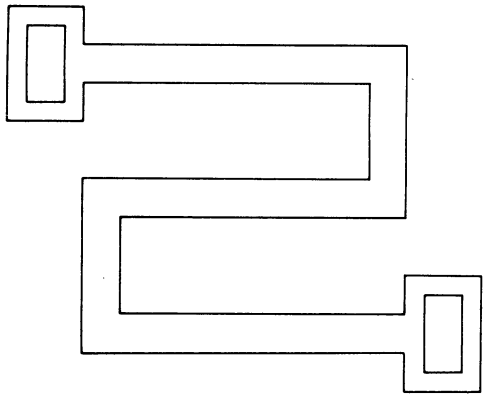


Figure 12.18

As most capacitors are formed using reverse-biased diodes, their values are restricted to the picofarad range.

12.9 Exercises

Exercise 12.1

How do photoemissive, photoconductive, and photovoltaic cells differ from each other in their principle of operation? Sketch on suitably labelled axes, typical characteristic curves for (a) vacuum and (b) gas-filled photoemissive cells and explain why the characteristics of the gas-filled cell differ from those of the vacuum type.

Draw a load line on one set of characteristics and indicate the change in anode voltage produced by a given change in illumination.

(ET4)

Exercise 12.2

An electromagnetic counter and a photocell with their associated circuitry are to be used to count the number of objects passing along a conveyor belt. Draw a simple circuit and explain its action. Briefly explain the action of the type of photocell you choose.

(ET4)

Exercise 12.3

With the aid of a circuit diagram, explain the operation of a photoelectric cell and amplifier for the indication of smoke density and incorporating an audible alarm. Show how zero and full-scale deflection would be checked and adjusted. Indicate the type of photocell you would use giving reasons for your choice.

(ET5)

Exercise 12.4

Photocells are used in many applications where protection of operating personnel is required. Briefly describe one such system.

Explain what is meant by a fail-safe circuit. Draw such a circuit for the system you have described and explain how fail-safe operation is achieved.

(ET5)

Exercise 12.5

Sketch the circuit and explain the operation of a photoelectric counting system. How are the effects of background light and stray reflection minimised?

State the characteristics of photoelectric devices used for (a) high-speed counting and (b) colour-selective counting.

(ET5)

Exercise 12.6

Draw a circuit diagram and explain the operation of a photoelectric furnace-temperature indicator and controller. Discuss the required characteristics of the photosensitive device and show how the desired value of temperature could be adjusted.

(ET5)

Exercise 12.7

(a) Compare and contrast the characteristics of a number of different types of photocell which are commonly available.

(b) A motorised trolley must follow a painted track on a factory floor. Its sensor head incorporates a lamp and two photocells which respond to the light reflected from the track. Show

how a system might be devised so that the trolley follows the track. Comment on any special problems which might be encountered.

(I.E.R.E.)

Exercise 12.8

Describe briefly the function and operation of each of the following (i) a photoemissive cell, (ii) a photoconductive cell, (iii) a photovoltaic cell, (iv) a phototransistor.

(I.E.R.E.)

Exercise 12.9

Write brief notes and include a simple diagram of three of the following techniques used in the manufacture of integrated circuits (i) diffused-collector process, (ii) triple-diffusion method, (iii) epitaxial process, (iv) oxide-isolation process, (v) thermo-compression bonding process.

(I.E.R.E.)

Exercise 12.10

Briefly describe how the following may be produced in an integrated circuit form (i) a resistor, (ii) a capacitor, (iii) a transistor, (iv) a field-effect transistor (FET).

(I.E.R.E.)

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