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Rong Wu
Johan H. Huijsing
Kofi A. A. Makinwa

Precision Instrumentation Amplifiers and Read-Out Integrated Circuits

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Rong Wu
e-mail: rongwu.grace@gmail.com

Kofi A. A. Makinwa
e-mail: k.a.a.makinwa@tudelft.nl

Johan H. Huijsing
e-mail: j.h.huijsing@tudelft.nl

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To my parents and Zhiyu

Preface

Sensors are ubiquitous in our lives and indispensable in many applications, e.g., process control, weighing scales, environmental monitoring, and temperature measurement. They can be found in wafer steppers, weighing scales, mobile phones and automobiles, etc. While these sensors convert the physical signals into electrical domain, their output voltage are small, in the millivolt-level, such as thermocouples and bridge transducers (thermistor bridges, Hall sensors and load cells). Therefore, they need amplifiers to boost such signals to levels compatible with the input ranges of typical Analog-to-Digital Converters (ADCs). To achieve sufficient signal-to-noise ratio, the input referred error of the amplifier should be reduced to a low enough level that means the amplifier must have low thermal and $1/f$ noise, high accuracy, and low drift. Achieving all these is quite challenging in today's mainstream CMOS technology whose inherent precision is limited by $1/f$ noise, component mismatch, gain error, and drift. A further challenge is to achieve good power efficiency since many sensor systems are battery-powered. This is also essential for precision temperature measurement to restrict local self-heating errors.

This book describes the use of power-efficient techniques to mitigate low frequency errors, resulting in interface electronics with high accuracy, low noise, and low drift. Since this book is mainly about techniques for eliminating low frequency errors, it describes the nature of these errors and the associated dynamic offset cancelation techniques used to mitigate them. It then shows how these techniques can be applied to operational amplifiers. Then these techniques are extended to current-feedback instrumentation amplifiers (CFIAs) which are well suited for bridge readout. Since the main disadvantage of CFIAs is their limited gain accuracy, the available techniques to improve this are discussed, such as resistor-degeneration, dynamic element matching, etc. The advantages and disadvantages of each of these techniques are analyzed.

Later, it presents the architecture design and implementation of a CFIA, in which a new technique (offset reduction loop) is proposed to suppress the chopper

ripple without causing noise folding. An improved version CFIA of the first CFIA is described, which maintains the noise performance of the first design and also achieves high gain accuracy without trimming. This is obtained by dynamic element matching and another proposed new technique (gain error reduction loop).

The basic architecture of the first CFIA is then combined with an ADC to build a readout IC. The system-level design of the readout IC together with implementation details and measurement results are presented. The CFIA and the ADC collaborate at system level to achieve an optimum performance. Measurement results show that the realized readout IC achieves state-of-the-art offset and drift performance.

Contents

Chapter 1
Introduction

This thesis describes the theory, design and realization of precision instrumentation amplifiers and read-out ICs for interfacing bridge transducers and thermocouples. The goal of the work is to investigate power-efficient techniques to eliminate low frequency (LF) errors in the read-out electronics, so as to achieve high accuracy, low noise and low drift while preserving low power consumption.

In this chapter, the motivation and objectives of this work are described, then an overview of prior art read-out electronics is given. This is followed by a description of a challenging application: the read-out of a precision thermistor bridge intended for high resolution temperature measurements in wafer steppers. Finally, the highlights and organization of the thesis are presented.

1.1 Motivation

A sensor can be defined as a device that forms the interface between non-electrical physical domains and the electrical domain. Examples of such physical domains are the thermal, magnetic, mechanical, radiant and chemical domains. Sensors are ubiquitous in our lives and indispensable in many applications, e.g. process control, weighing scales, environmental monitoring, and temperature measurement. They can be found in wafer steppers, weighing scales, mobile phones and automobiles, etc. For example, there are more than 300 sensors in a modern car and the overall value of the market is expected to grow from $9.9 billion in 2009 to $16.1 billion in 2014 [1].

While these sensors convert the physical signals into electrical domain, their output voltage are small, in the millivolt-level, such as thermocouples and bridge transducers (thermistor bridges, Hall sensors and load cells). This thesis focuses on the design of the interface electronics for such sensors.

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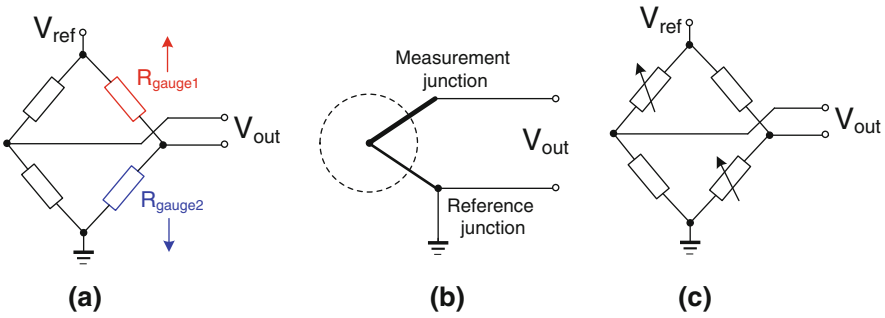

Fig. 1.1 Examples of bridge transducers and thermocouples **a** Load cell **b** Thermocouple **c** Thermistor bridge

Load cell
A load cell is a sensor that is used to convert a force into an electrical signal. It usually consists of a number of strain gauges configured in a Wheatstone bridge (Fig. 1.1a). Through a mechanical arrangement, the sensed force deforms the strain gauge, thus changing its electrical resistance. A recent report has shown that the global load cell market is forecast to reach $1.5 billion dollars by 2015 [2].

Thermocouple
A thermocouple consists of two wires made of different metals that are joined at one end, called the measurement junction. At the other end of the conductors, a reference junction is formed (Fig. 1.1b). If the measurement and the reference junctions are at different temperatures, a voltage appears across the two terminals that is a function of this temperature difference. Thermocouples are widely used in industrial manufacturing environments.

Thermistor Bridge
A thermistor is a resistor whose value varies significantly with temperature. To measure temperature, they are usually configured in a Wheatstone bridge structure (Fig. 1.1c). Compared to thermocouples, thermistor bridges exhibit higher sensitivity and lower noise, thus they are widely used in precision temperature measurement applications, such as temperature control and compensation systems.

Hall Sensors
The principle behind the Hall Effect is that a magnetic field induces a voltage between two points on the sides of a current-carrying conductor. A Hall sensor is thus a four terminal device which can be modeled as a Wheatstone bridge. Hall sensors can be used for contactless current sensing, since they are sensitive to the induced magnetic field instead of the target (current) itself. Besides current-sensing, they are also widely used for position measuring, speed detection and proximity switching applications.

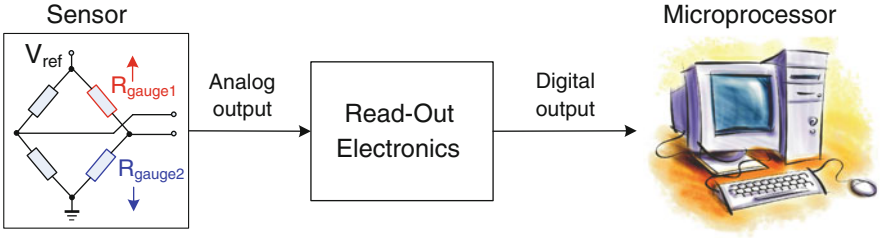

Fig. 1.2 Read-out electronics bridging the analog and digital worlds

1.2 Overview of Read-Out Electronics for Sensors

The electrical information produced by the sensor is usually an analog signal and thus needs to be converted to a robust digital signal for further signal processing [3, 4]. The system that converts the analog signal from the sensor to the digital domain is called a *sensor read-out system*. Figure 1.2 shows a typical strain gauge readout system. The analog output signal of the strain gauge is processed by the read-out electronics and converted into a digital signal.

Given the broad applications of thermocouples and bridge transducers it is important to investigate and improve the quality of their read-out electronics and this will be the main goal of this thesis. Load cells, thermocouples, thermistor bridges and Hall sensors typically output LF small signals in the millivolt-range. Therefore, they need amplifiers to boost such signals to levels compatible with the input ranges of typical Analog-to-Digital Converters (ADCs) (Fig. 1.3). A single integrated chip on which both the preamp and the succeeding ADC is implemented is called a *read-out IC*.

Although the differential output voltage of the sensor V_{id} can be as small as a few millivolts (Fig. 1.3), the common-mode (CM) voltage V_{CM}, depending on the application, may be much larger and may even vary by a few volts during the period of operation. Furthermore, the CM voltage of thermocouples may equal one of the supply rails, usually ground. To accommodate this variable CM voltage, an *Instrumentation Amplifier* (IA) is generally used for sensor read-out applications. To accurately process the millivolt-level signal from the sensor, the input referred error of the IA should be at the microvolt- or nanovolt-level. To cope with CM variations of a few volts, the IA should have a common-mode rejection ratio (CMRR) greater than 120 dB. Furthermore, it should have high input impedance so as not to attenuate the sensor signal or load the sensor. This amplifier is very critical since it determines the overall performance of the read-out IC. *To sum up*, the main functions of this amplifier are to

1. Amplify the weak differential voltage (V_{id})
2. Reject the sensor common-mode voltage (V_{CM}) (CMRR $>$ 120 dB)
3. Be capable of handling CM voltages near the rails
4. Provide high input impedance for bridge read-out

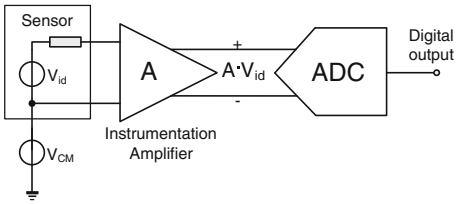

Fig. 1.3 Read-out IC for bridge transducers that consists of an instrumentation amplifier and an ADC

As the amplifier is used to detect a small differential signal, its input-referred error (due to noise and offset) must be reduced well below the minimum signal amplitude. Since most sensor applications operate near DC with a bandwidth of a few Hz, 1/*f* noise is the dominant noise source. Although bipolar technology is well known for its low offset and low 1/*f* noise [5], nowadays, CMOS is the preferred technology because of its low cost and the powerful capability of digital signal processing. However, amplifiers realized in CMOS technology have nonidealities such as offset and 1/*f* noise. The worst-case offset can be as large as 10 mV, while the 1/*f* noise corner frequency can be a few tens of kHz. This problem can be solved with dynamic offset cancellation techniques. The first MOS chopper operational amplifier was reported in [6]. Later, CMOS amplifiers with microvolt offset levels have been achieved [7–10] and amplifiers with 1/*f* noise corner frequency of a few Hz [12, 13] and even a few tens of mHz [14] have been reported.

Besides offsetgain error is another dominant source of error. It is usually determined by component mismatch and has typical values of ± 1 % in a standard CMOS process. Furthermore, the amplifier's gain should have very low temperature drift, so that it can be used for temperature measurement applications (e.g. for the read-out of thermocouple and thermistor bridge). Instrumentation amplifiers meeting such specifications (low noise, low offset and low drift) are further classified as *precision instrumentation amplifiers*. The succeeding ADC converts the amplified analog output to the digital domain, while maintaining the signal-to-noise-ratio from the precision instrumentation amplifier.

To conclude, achieving low thermal and 1/*f* noise, high accuracy and low drift is quite challenging in today's mainstream CMOS technology whose inherent precision is limited by 1/*f* noise, component mismatch, gain error and drift. A further challenge is to achieve good power efficiency since many sensor systems are battery-powered. This is also essential for precision temperature measurement to restrict local self-heating errors.

This thesis addresses these challenges in two ways. First, it presents the design of two *stand-alone* precision instrumentation amplifiers which can be independently used in many practical systems to drive an external ADC. Second, it describes the design of a read-out IC that combines the instrumentation amplifier and the ADC into one chip, so as to provide a digital output.

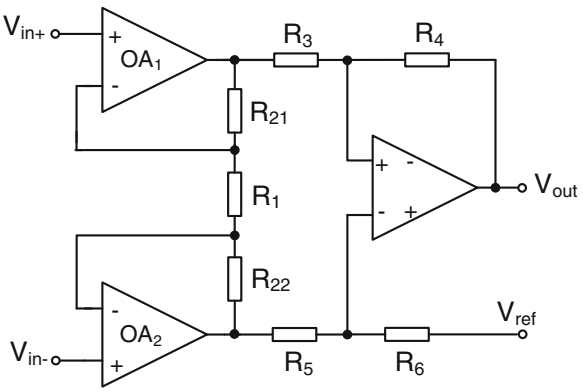

Fig. 1.4 Bridge instrumentation amplifier realized by three operational amplifiers

1.3 Instrumentation Amplifier Topologies

Instrumentation amplifiers can be built in several ways. The commonly used topologies are the classic three-opamp, switched-capacitor, capacitively-coupled, current-mode and current-feedback instrumentation amplifiers (IAs).

1.3.1 Three-Opamp Topology

The three-opamp IA uses voltage feedback to obtain a gain determined by resistors [15]. Figure 1.4 shows a fully-differential three-opamp IA in which the first stage is a fully-differential amplifier with a gain of $(R_{21} + R_1 + R_{22})/R_1$ and the second stage is a differential amplifier.

The CMRR of the three-opamp IA is determined by the product of the finite gain of its first stage, and the finite CMRR of its second stage. The latter is determined by the matching of the feedback resistors R_3–R_6, which usually leads to a CMRR of about 80 dB [16]. Furthermore, it can not sense the supply rails because the input CM level of the amplifier must be set within its output voltage range. This topology is also not very power-efficient, as it requires the use of two high-gain opamps. However, it exhibits high input impedance and good linearity over a wide input and output range. If a differential output is required, the first stage can be used alone, which is known as the "two-opamp" topology.

1.3.2 Switched-Capacitor Topology

The switched-capacitor (SC) IA uses capacitors as the feedback elements [17, 18]. A fully-differential SC IA is shown in Fig. 1.5. When clock Φ_1 is high, the input signal is sampled on capacitor C_1, while the integration capacitor C_2 is reset. When

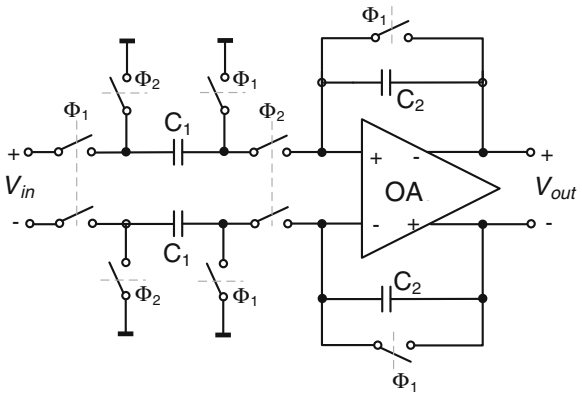

Fig. 1.5 Switched-capacitor instrumentation amplifier

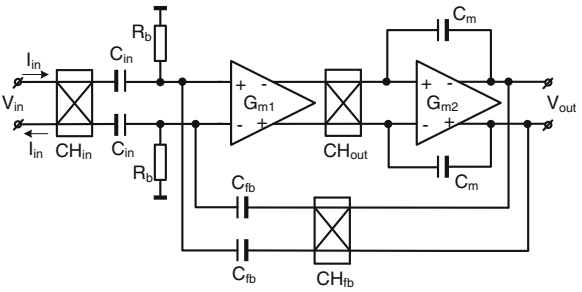

Fig. 1.6 Capacitively-coupled instrumentation amplifier

clock Φ_2 is high, the charge stored on C_1 is transferred to C_2. The closed-loop gain of the IA is determined by C_1/C_2. With careful layout, this gain can achieve 0.1 % gain error and low drift over temperature. Furthermore, this topology accommodates a large CM input range since the input sampling capacitors block DC. However, it can not provide a continuous signal and the sampling procedure of the SC amplifier increases noise level due to noise folding. The noise associated with sampling is the well-known *kT/C* noise [19]. To reduce noise, input capacitor C_1 needs to be increased. However, this results in a decrease in the input impedance due to the switching impedance of input capacitors [20].

1.3.3 Capacitively-Coupled Topology

A recent development is the continuous-time capacitively-coupled (and chopped) IA [12, 21]. As shown in Fig. 1.6, it employs an input chopper (polarity reversing switch) to convert the input DC signal into an AC signal, which can be transported via the capacitors. An output chopper then converts the amplified AC signal back to DC. Since capacitors block DC signals, this topology exhibits a rail-to-rail input CM range. Furthermore, it is very power-efficient since it has a continuous-time

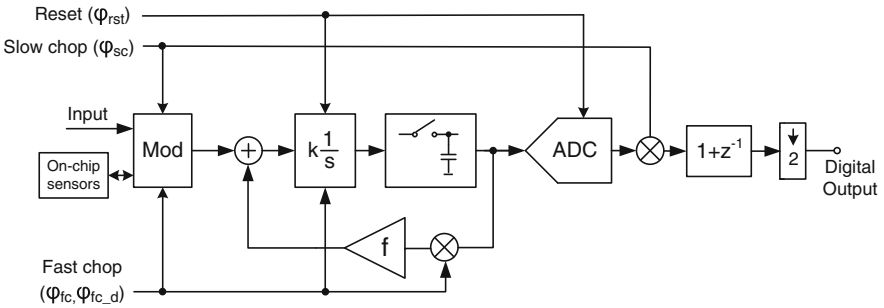

Fig. 1.7 Block diagram of an improved capacitively-coupled analog-to-digital interface [22]

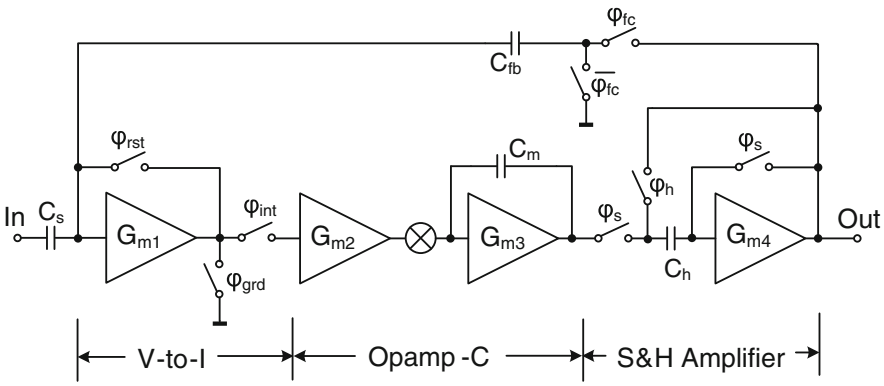

Fig. 1.8 A closed-loop capacitive-feedback sampler [22]

signal path and its power consumption is mainly dominated by G_{m1}. Its input impedance is typically in the order of several MΩ, determined by the impedance of the input capacitors at the chopping frequency. This can be increased to a few tens of MΩ by using an impedance boosting technique [21]. The disadvantage of this topology is that the switched-chopper capacitor causes spikes (or glitches) and more noise at the amplifier output.

An improved capacitively-coupled analog-to-digital interface was reported in [22]. As shown in Fig. 1.7, it consists of a sampler and a sigma-delta (ΔΣ) ADC. The sampler employs a closed-loop capacitively-coupled topology consisting of a V-to-I converter, a G_m-C integrator followed by a sample-and-hold amplifier (Fig. 1.8). Unlike [12, 21] in which the input chopper precedes the input capacitors, here, the input chopper is shifted in the sensor. The sampler (Fig. 1.8) directly processes the modulated sensor signal, thus its input capacitor *C*s provide high input impedance and also store the offset for coarse offset cancellation. The residual offset, 1/*f* noise of the interface electronics (mainly from the ADC) and the mismatch of the input capacitors are then eliminated by nested chopping that chops the complete read-out chain.

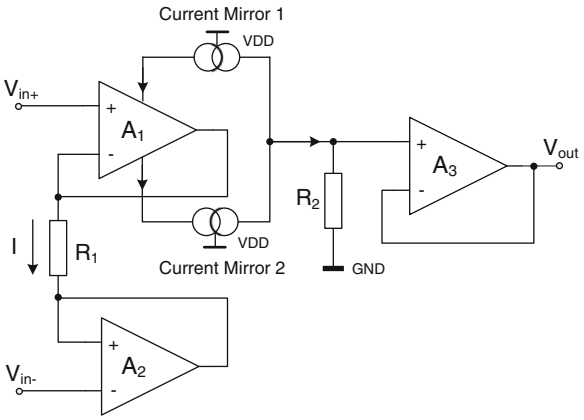

Fig. 1.9 Current-mode instrumentation amplifier

The presence of the sampler (Fig. 1.8) means that this circuit can not be, used as a stand-alone IA with a continuous-time output signal. This implies that capacitively-coupled IAs is more compatible with a SC sampled ADC. With proper timing, sampling of the spikes at the IA output [21] can be avoided and the non-continuous signal path [22] is not an issue for a SC sampled ADC.

1.3.4 Current-Mode Topology

Figure 1.9 shows a current-mode instrumentation amplifier [23–26]. The feedback around the input amplifiers A_1 and A_2 forces the input voltage across the resistor R_1. The current through this resistor is mirrored by precision current mirrors and converted into a voltage by R_2, and then buffered by the output opamp A_3. The CMRR of this topology depends on the matching of the current-mirrors and the DC precision of the current mirrors is essential for the overall offset, gain accuracy, drift and linearity. Since the matching of an impedance-boosted current mirror is still insufficient for the required DC precision, thin-film resistor-degenerated current mirrors [26] is used and a CMRR larger than 120 dB is achieved. However, precise thin-film resistors are not always available in CMOS technology.

1.3.5 Current-Feedback Topology

Figure 1.10 shows a current-feedback instrumentation amplifier (CFIA). The input transconductor G_{m2} and feedback transconductor G_{m3} convert the input and feedback voltages into corresponding currents. Their difference is then nulled by the gain of G_{m1}. The overall feedback ensures that the output currents of G_{m2} and G_{m3} cancel and thus the amplifier's gain is given by

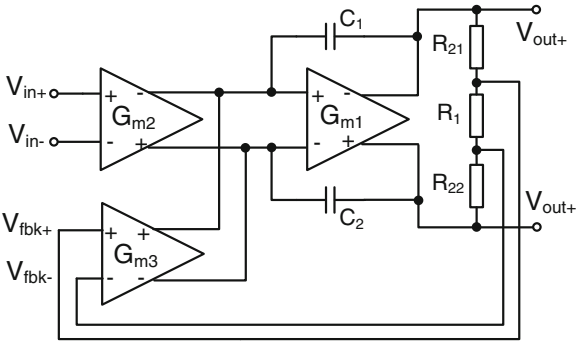

Fig. 1.10 Current-feedback instrumentation amplifier

$$Gain = \frac{G_{m2}}{G_{m3}} \frac{R_1 + R_{21} + R_{22}}{R_1} \tag{1.1}$$

The CFIA is well suited for bridge read-out. First, compared to the three-opamp topology, it achieves higher CMRR, because the input transconductor G_{m2} isolates the input CM level by converting the input differential voltage to a differential current [27]. Its CMRR is mainly determined by the CMRR of G_{m2} and can be made greater than 120 dB. Second, it is capable of handling input CM voltages that include either of the supply rails [16]. Third, it is more power efficient because it can be seen as a merged version of the three-opamp topology [28], in which the output stages are shared.

Compared to the switched-capacitor IA, the CFIA avoids noise folding. Furthermore, the CFIA has higher input impedance than the capacitively-coupled topology, and it does not produce output glitches. The CFIA is thus more suitable for use as a stand-alone IA.

The main disadvantage of the CFIA is its limited gain accuracy. From (1.1), assuming the open-loop gain of the CFIA is high enough and that precision external feedback resistors (R_1, R_{21} and R_{22}) are used, the CFIA's closed-loop gain accuracy is mainly determined by the matching between the input and feedback transconductors (G_{m2} and G_{m3}). Furthermore, the linear range of a CFIA is often limited by the input and feedback transconductors to several tens of mV. Although this limited input range is not a problem for many bridge applications, extending it will make the CFIA useful for other applications.

The first part of the thesis will focus on the design of improved CFIAs, while their major disadvantages–limited gain accuracy, limited input range and nonlinearity will be addressed.

1.4 Current-Feedback Instrumentation Amplifier

The first CFIA was introduced by Analog Devices [29] in 1971, and was implemented in bipolar technology. Later, the current-feedback concept was again described by Huijsing in 1981 [30] and by Säckinger in 1987 [31]. In 1984, a

bipolar CFIA used in low-power biomedical applications was reported by Hamstra [32]. In 1993, Dool described another bipolar CFIA with a CM input range that included the negative rail [16].

The first CFIA implemented in CMOS technology was presented in 1987 by Steyaert for medical applications [33]. Although amplifiers in CMOS technology typically has larger offset and 1/*f* noise than these in bipolar technology, the existence of good MOS switches means that both these non-idealities can be mitigated by dynamic offset cancellation techniques. Later, in 2004, Chan introduced a CFIA that employs dynamic offset cancellation techniques to achieve low offset (16 μV) and low 1/*f* noise [34].

Recently, several CFIAs have been reported [8, 11, 35] which achieve offsets less than 5 μV or even less than 2 μV. Table 1.1 summaries the performance of these CFIAs. Since power efficiency is an important design criterion in this work, the noise efficiency factor (NEF) [33] is used to evaluate the power efficiency of these CFIAs. It relates the amplifier's noise PSD and supply current, as given by:

$$NEF = V_n\sqrt{\frac{2I_{tot}}{\pi \cdot V_t \cdot 4kT \cdot BW}}, \tag{1.2}$$

where V_n is the input-referred noise voltage, I_{tot} is the supply current of the amplifier, V_t is the thermal voltage which equals kT/q, and BW is the amplifier bandwidth.

As seen from Table 1.1, although these CFIAs all achieve offsets of a few μV, they consume significant amount of power (NEF > 24). Unlike noise, the offset does not have a direct trade-off with power consumption. This means that it should be possible to achieve low offset with low power.

Through a new technique (an offset reduction loop, ORL) [28], a precision CFIA is presented in this thesis that achieves microvolt-offset with 3 × improved power efficiency (NEF = 8.8) compared to [8]. Moreover, its 1/*f* noise corner is in the mHz range, which has not been achieved by previous stand-alone CMOS amplifiers.

As mentioned before, the main disadvantage of the CFIA is its limited gain accuracy, which is determined by the mismatch of the input and feedback transconductances. If precision feedback resistors are used, in the worst-case, this mismatch can be as large as 2 %. To reduce this mismatch, resistor-degeneration was used [11, 35], since with careful layout, or by trimming, resistors can be made to match better than transistors. As a result, a gain error of 0.1 % has been achieved [11, 35]. However, resistor degeneration leads to a significant loss in power efficiency (NEF = 43 [35] and 153 [11]). Moreover, trimming the degeneration resistors [11] increases production cost. This thesis presents a power-efficient CFIA that achieves high gain accuracy without trimming. By using dynamic element matching and a gain error reduction loop (GERL) [36], it achieves an *untrimmed* gain error of 0.06 % in a power efficient manner (NEF = 11.2).

Table 1.1 Performance of low-offset CFIAs

	Witte [8]	Pertijs [35]	Witte [11]
Year	2009	2010	2008
Supply voltage	5 V	3.0 to 5.5 V	2.8 to 5.5 V
Supply current	325 μA	1.7 mA	850 μA
Input noise PSD	42 nV/$\sqrt{}$Hz	27 nV/$\sqrt{}$Hz	136 nV/$\sqrt{}$Hz
CMRR	130 dB	142 dB	140 dB
Gain error	0.05 % (Untrimmed) (Relative)	±0.1 % (Untrimmed) (Absolute)	±0.1 % (trimmed) (Absolute)
Offset	<2.5 μV	<2 μV	<5 μV
GBW	640 kHz	800 kHz	1 MHz
NEF [33]	29.2	43	153

1.5 Read-Out ICs

The second part of the thesis is devoted to the design of a read-out IC. It consists of a precision instrumentation amplifier followed by an ADC. The IA provides high input impedance and relaxes the offset and noise requirements of the ADC.

Since the read-out IC acts as an ADC, a figure of merit (FOM) [37] is used to evaluate its power efficiency. This FOM relates the read-out IC's resolution and bandwidth with its the power consumption, as given by

$$FOM = \frac{Power}{2 \cdot BW \cdot 2^{ENOB}} \tag{1.3}$$

where BW is the bandwidth of the ADC, ENOB is the effective number of bits, defining as

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{1.4}$$

where SNDR is the Signal-to-Noise-Distortion-Ratio. Note that including ENOB in the formula takes into account the distortion introduced by the ADC.

Many precision read-out ICs have been reported, which achieve more than 20-bit resolution, low offset and gain drift (<15 ppm/°C) [38–42]. They are intended for precision instrumentation and measurement applications. To achieve such high resolution within a small bandwidth (<250 Hz), a delta-sigma (ΔΣ) ADC is a good choice. This is due to the fact that the resolution of Nyquist-rate ADCs is limited by component matching, while ΔΣ ADCs apply over-sampling technique which trades speed for resolution. Furthermore, with noise shaping, ΔΣ ADCs can easily achieve a resolution higher than 18-bit [43].

Figure 1.11 shows the block diagram of a ΔΣ ADC. It consists of a single-loop ΔΣ modulator and a decimation filter. The ΔΣ modulator consists of a loop filter, performing the noise-shaping, a low resolution quantizer, which is over sampled

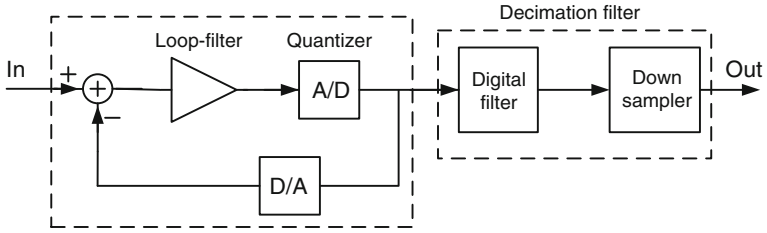

Fig. 1.11 Block diagram of a ΔΣ ADC

and a digital-to-analog converter (DAC). The oversampling ratio (OSR) is defined as OSR $= f_s/2f_b$, where f_s is the sampling rate and f_b is the signal bandwidth. The ΔΣ modulator shapes the frequency response of the quantization errors in such a way that the quantization error is reduced in the frequency band of interest, while it is increased outside that band. Therefore, high resolution can be obtained in a relatively small bandwidth. Since most of the quantization noise is shifted to higher frequencies, it is necessary to eliminate the high frequency noise by using a decimation filter.

For instrumentation applications, the input signal is a low-frequency or DC signal, so the ΔΣ ADC typically operates in 'single-shot' mode, which means that it powers up, produces a single conversion result and finally powers down again to save power. This type of ΔΣ ADCs are called *incremental* ΔΣ ADCs. Their main characteristics are:

1. The loop filter and the decimation filter are reset at the beginning of a conversion.
2. The modulator does not operate continuously, but runs for a limited number of N clock cycles, producing a bitstream of N bits.

Incremental ΔΣ ADCs provide very precise conversion with accurate gain, high linearity and low offset [44]. A first-order ΔΣ modulator for instrumentation applications was already introduced by Van der Plassche in 1978 [45], which achieve 6-bit resolution reference to 1 V. In 2006, Quiquempoix reported a 22-bit third-order incremental ADC reference to 5 V [44]. It achieves a 2 μV offset, 2 ppm gain error and 4 ppm INL with a FOM of 4.8 pJ/conv.

However, since bridge sensors typically produce millivolt-level signals, they need precision IAs to boost the sensor signals to the typical ADC input range of a few volts (Fig. 1.3). The IA is the most challenging and power consuming part, since it determines the noise and accuracy performance of the read-out IC [39].

The IAs in previous precision read-out ICs generally employ switched-capacitor (SC) or two-opamp IA topologies. For instance, Analog Devices reported a read-out IC in 1997 [38] that used a SC IA, as shown in Fig. 1.12. Due to the sampling in the SC amplifier, its noise level increases due to noise folding. Furthermore, an additional input buffer was necessary to provide high input impedance for bridge read-out. To satisfy the noise specification, this read-out IC

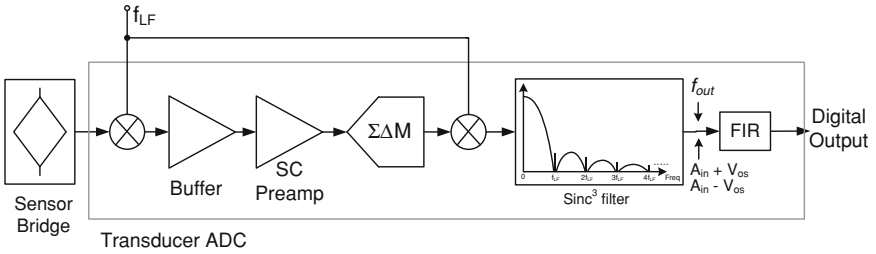

Fig. 1.12 Block diagram of the read-out IC in [39]

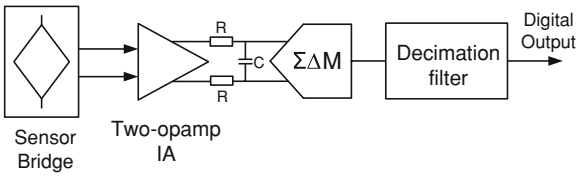

Fig. 1.13 Block diagram of read-out IC in [39]

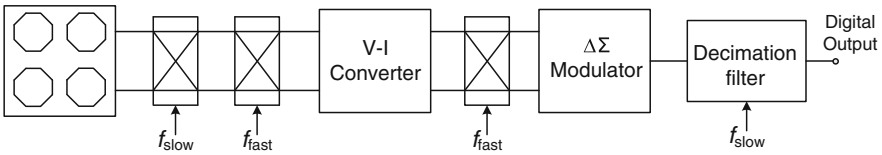

Fig. 1.14 Block diagram of hall sensor interface in [46]

results in a high power consumption of 80 mW to achieve an 18-bit resolution with 10 mV full scale. The ADC is realized with a second-order incremental ΔΣ ADC. System-level chopping is employed to chop the entire analog signal path at a slow frequency of f_{LF} [38]. The subsequent digital decimation filter creates notches to suppress the modulated offset due to chopping. Overall, it achieves an offset drift in the level of 10 nV/°C. The FOM of the total read-out IC is 43,000 pJ/Conv.

In 2000, Cirrus Logic described a read-out IC [39], shown in Fig. 1.13. It consists of a two-opamp IA and a fourth-order incremental ΔΣ ADC. This architecture is also not particularly power efficient, since the two-opamp IA requires two high-gain amplifiers, thus resulting in a high power consumption of 40 mW to achieve a 19-bit with 28 mV full scale in a BW of 128 Hz (FOM = 164pJ/Conv).

A Hall sensor interface for compass application was reported by van de Meer et al. in 2005 [46] and its block diagram is shown in Fig. 1.14. It consists of a voltage-to-current converter (VIC), whose differential current output is digitized by a first-order sigma-delta modulator. The output of the modulator is averaged over an entire spinning-current cycle by a decimation filter. To achieve high

linearity over a wide dynamic range, the VIC consists of two opamps, each with a DC gain of over 120 dB. This Hall sensor interface achieves 120 dB resolution and less than 50nV offset with a consuming 21 mW.

Recently released read-out ICs from Analog Devices [40], Cirrus Logic [41] and Texas Instruments [42], still use the SC or two-opamp IAs. That is part of the reason why these read-out ICs are not very power efficient. The FOM of [40–42] are 135, 9,000 and 172 pJ/Conv, respectively.

CFIAs, in contrast, provide superior power efficiency, since they avoid noise folding and share output stages. Furthermore, the CFIAs exhibit high CMRR [8, 16] and rail-to-rail sensing capability [16, 35]. In order to show the potential of CFIAs in read-out IC applications, this thesis presents the design of a read-out IC [47] that combines a CFIA and an ADC. In this work, various dynamic cancellation techniques are used to eliminate the $1/f$ noise, offset, gain error and drift. Moreover, digital signal processing on the output of the ADC is explored to improve the CFIA's gain accuracy and gain drift. The CFIA and the ADC can then collaborate together to achieve optimum performance. Compared to the state-of-the-art [40], the proposed read-out IC achieves 10 × better offset (50 nV), comparable gain drift (1.2 ppm/°C) and better power efficient (FOM = 111 pJ/Conv).

1.6 Targeted Sensor Applications and Challenges

As a test-case, the challenging task of developing interface electronics for a precision thermistor bridge was attempted. It is intended for use in wafer steppers where μK-level temperature resolution is required [28].

In wafer steppers, thermal expansion is an important source of error and so control loops are used to stabilize the temperature, and consequently the dimensions of critical mechanical components. The mechanical stability requirements on these components translate into allowable temperature drifts in the order of 100 μK per minute. To measure such slow drifts with sufficient resolution, the total noise of the sensor read-out system should be less than 1μK (3σ) from 21.1 °C to 22.9 °C, i.e. a 1.8°C range (equivalent to a 21-bit resolution) when measured in a bandwidth ranging from 3 to 50 mHz.

Since the goal is to prevent temperature drift, the absolute accuracy of the temperature measurement system may be much worse than its 1 μK resolution. Thus absolute accuracy is established by periodic system-level calibrations. To maintain accuracy during the (minute-long) intervals between calibrations, the thermistors, as well as the interface electronics used to read them out should be characterized by low LF noise, with $1/f$ noise corners in the order of only a few mHz. In addition, the read-out electronics must have low offset and gain drift (a few ppm/°C) to maintain system accuracy over temperature.

Compared to other temperature sensors such as thermocouples, negative temperature coefficient (NTC) thermistors are well suited for high-resolution temperature measurements because they can achieve high sensitivity, low thermal

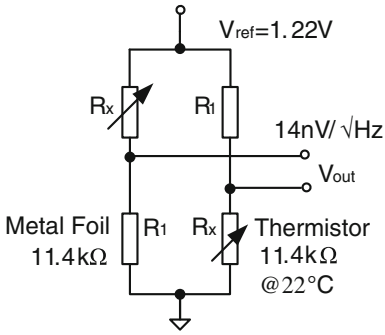

Fig. 1.15 Dual thermistor bridge

noise, low 1/*f* noise corners (in the mHz range for high quality parts), and good long-term stability (about 1 mK/year) [48].

In order to double the sensitivity, a double thermistor bridge consisting of two thermistors and two metal foil resistors is shown in Fig. 1.15. In our case, the resistance of the thermistor (R_x in Fig. 1.15) is 11.4 kΩ at 22°C, the same as the resistance of the metal foil resistors (R_1 in Fig. 1.15). Therefore, the bridge output is zero at a temperature of 22°C. Due to the tolerance of its components, the bridge has a gain error of ± 0.5 %. When biased by a band-gap reference at 1.22 V, the common-mode voltage of the bridge is 0.61 V and its sensitivity is 27 mV/°C. Thus, over the required 1.8°C range, the output range of the bridge is ± 24.3 mV.

Being only at the millivolt level, the output of the thermistor bridge should be amplified before it is digitized or processed further. This requires the use of a low-noise instrumentation amplifier followed by an ADC. The challenges associated with the design of the read-out electronics are discussed below.

The first challenge is the required resolution: 0.33 μK (1σ) in a 1.8°C range in a bandwidth ranging from 3 mHz to 50 mHz. Together with the sensitivity of the bridge (27 mV/°C), this translates into an input-referred noise density requirement of 31 nV/$\sqrt{}$Hz for the whole system. The thermal noise level of the thermistor bridge is 14 nV/$\sqrt{}$Hz, and so the amplifier's white noise density was chosen to be at roughly the same level, i.e. 16 nV/$\sqrt{}$Hz. To achieve high power efficiency, the amplifier's noise should be white in the bandwidth of interest, which means that the amplifier's 1/*f* noise corner frequency must be below 3 mHz. To justify such low noise specifications, the amplifier must also have high CMRR (>120 dB) and PSRR (>120 dB).

The second challenge is the need for the amplifier to accommodate different input and output CM voltages. Since the bridge is biased at 1.22 V, the input CM is at 0.61 V. While the output CM is at 2.5 V, since the amplifier's output is to be digitized by an ADC with a 0–5 V input range.

Thirdly, since the sensor and the read-out electronics are calibrated as a single system, the read-out electronics should exhibit very low offset and gain drift (a few ppm/°C) to maintain system accuracy over temperature. Thus, the read-out electronics aims to achieve gain and offset drift less than 1 ppm/°C and 10 nV/°C, respectively.

Table 1.2 Typical sensor specifications and targets of the read-out IC

	Strain Gauge	Thermo-couple	Thermistor bridge	Hall sensor	Target of read-out electronics
Resolution	20-bit (±10 mV)	18-bit (±2 mV)	21-bit (±48 mV)	20-bit (±50 mV)	20-bit (±40 mV)
Noise PSD	√	√	14 nV/√Hz	√	16 nV/√Hz
1/*f* noise corner	√	√	<3 mHz	√	1 mHz
BW	5 Hz	√	√	√	5 Hz
Gain drift	√	√	1 ppm/°C	√	1 ppm/°C
Gain error	0.02 %	√	√	√	0.02 %
Offset	√	√	√	50 nV	50 nV
Offset drift	√	√	10 nV/°C	√	10 nV/°C
Supply current	√	√	300 μA	√	<300 μA

Note for sensor specifications, only the most challenging one is shown in each row, while the other two are represented with '√'

The final challenge involves self-heating. For the thermistor read-out application in wafer steppers, the read-out electronics and the thermistor bridge are located in the vacuum environment of a wafer stepper where heat sinking is a significant problem. The power consumption of the interface electronics should not be larger than that of the bridge (a few hundreds of μA) to restrict local self-heating errors.

To make the interface electronics not only useful for thermistor bridge, but also applicable for other voltage-out sensors, e.g. strain gauge and thermocouple and Hall sensors, as shown in Table 1.2, the read-out IC was also designed to achieve the same gain accuracy as stain gauges: less than 0.02 % [49]. Since Hall sensor output with zero field conditions is less than 50 nV, in order to accurately process sensor output, the interface electronics must have an offset less than 50 nV [46]. Furthermore, the read-out IC is designed to have a bandwidth of 5 Hz, to make it useful for some strain gauges applications. Thus, the targeted noise specification is a noise PSD of 16nV/√Hz from 3 mHz to 5 Hz, which corresponds to a 20-bit resolution reference to ±40 mV.

In summary, the low noise, low drift and low power qualities of the read-out electronics presented in this thesis are beyond the capability of current available interface electronics. These qualities make the demanding thermistor read-out application in wafer steppers possible. In addition, the read-out electronics also can be used for interfacing strain gauge, thermocouples and Hall sensors.

Although this research work is targeted for sensor applications, the new techniques developed in this work also can be applied to other applications, such as general purpose operational amplifiers, general purpose CFIAs and general purpose read-out ICs.

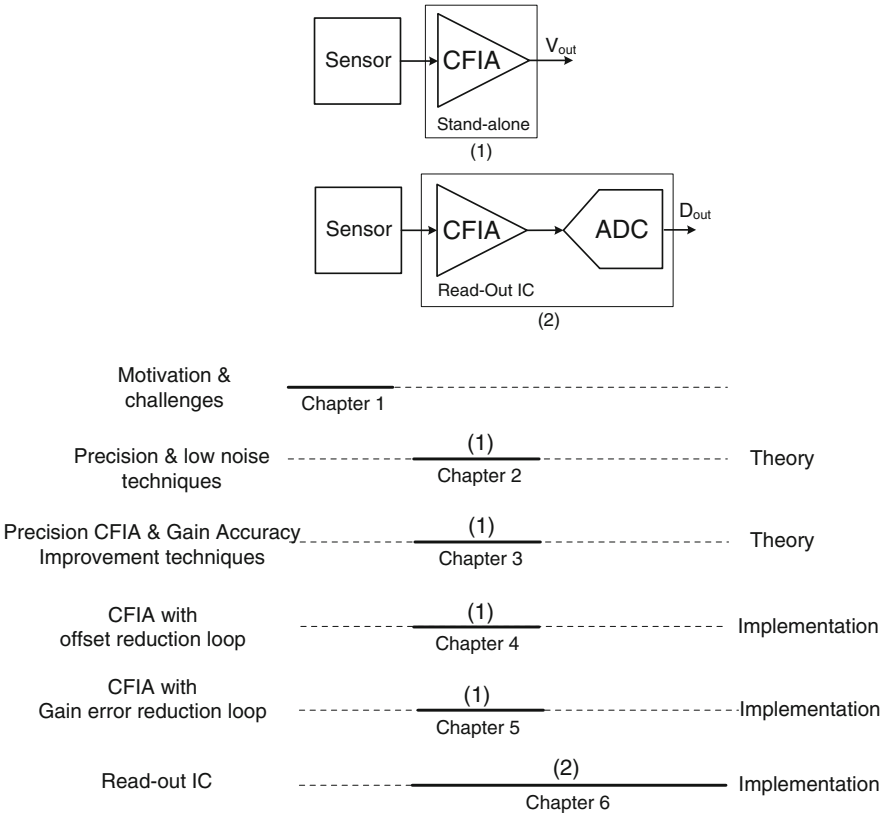

Fig. 1.16 Organization of the thesis

1.7 Organization of the Thesis

This thesis has been divided into seven chapters. The organization of the thesis is illustrated in Fig. 1.16. It is divided into two parts. The first part is indicated as (1) in Fig. 1.16: the design of precision stand-alone IAs for bridge interfacing. The second part is indicated as (2) in Fig. 1.16: the design of a read-out IC that combines the IA and an ADC. The outlines for each chapter are discussed as follows.

Since this thesis is mainly about techniques for eliminating low frequency errors, Chap. 2 describes the nature of these errors and the associated dynamic offset cancellation techniques used to mitigate them. It then shows how these techniques can be applied to operational amplifiers.

In Chap. 3, these techniques will be extended to CFIAs. Since the main disadvantage of CFIAs is their limited gain accuracy, this chapter discusses the available techniques to improve this, such as resistor-degeneration, dynamic

element matching, etc. The advantages and disadvantages of each of these techniques are analyzed.

Chapter 4 presents the architecture design and implementation of a CFIA. A new technique (offset reduction loop) is proposed to suppress the chopper ripple without causing noise folding. This CFIA achieves low offset, low thermal and 1/*f* noise and simultaneously, low power consumption. A 1/*f* noise corner of 1 mHz is achieved at a noise PSD of 15nV/$\sqrt{}$Hz with a NEF of 8.8.

Chapter 5 discusses an improved version CFIA of the first CFIA described in Chap. 4. It maintains the noise performance of the first design and also achieves high gain accuracy without trimming. This is obtained by dynamic element matching and another proposed new technique (gain error reduction loop). It achieves less than 3 μV offset, and 0.06 % untrimmed gain error in a power efficient manner (NEF = 11.2). These results show that the CFIA achieves state-of-the-art performance in terms of offset, 1/*f* noise, gain accuracy and power efficiency.

The basic architecture of the CFIA discussed in Chap. 4 is then combined with an ADC to build a read-out IC. Chapter 6 discusses the system-level design of the read-out IC together with implementation details and measurement results. The CFIA and the ADC collaborate at system-level to achieve an optimum performance. Measurement results show that the realized read-out IC achieves state-of-the-art offset and drift performance.

In Chap. 7, the main conclusions of the thesis are presented. Special sections have been included to highlight the original contributions of this thesis and some recommendations for future work are made.

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Chapter 2
Dynamic Offset Cancellation Techniques for Operational Amplifiers

At low frequencies, offset, 1/*f* noise and drift are the dominant error sources of operational amplifiers. This is especially true in CMOS technology. This chapter reviews precision techniques that can be used to achieve low 1/*f* noise and low offset in operational amplifiers.

There are three types of CMOS offset cancellation techniques: trimming, chopping, and auto-zeroing. Trimming is usually performed during production to eliminate offset. Auto-zeroing is a sampling technique in which the offset is measured and then subtracted in subsequent clock phases. Chopping, on the other hand, is a continuous-time modulation technique in which the signal and offset are modulated to different frequencies. Due to the modulated offset and 1/*f* noise, a chopper ripple appears at the amplifier output. Since chopping and auto-zeroing are dynamic techniques that continuously reduce offset, they also remove low frequency 1/*f* noise as well as offset drift over temperature or time.

In auto-zeroing amplifiers, the residual offset is mainly caused by charge injection and clock feed-through. While in chopper amplifiers, the residual offset is mainly caused by demodulated clock feed-through spikes. Several techniques can be used to counteract these non-idealities.

Later in this chapter, several dynamic-offset-compensation techniques used in operational amplifiers will be discussed, e.g. ping-pong auto-zeroing, offset stabilization, and specifically, chopper offset stabilization of a low-frequency path in a multi-path amplifier. To suppress chopper ripple, numerous ripple reduction techniques can be used. It will be shown that these all have significant drawbacks, and thus new techniques are required.

R. Wu et al., *Precision Instrumentation Amplifiers and Read-Out Integrated Circuits*, Analog Circuits and Signal Processing, DOI: 10.1007/978-1-4614-3731-4_2,

2.1 Introduction

For sensor applications, the bandwidth of interest is generally a few Hz. In this bandwidth, offset, 1/*f* noise and drift are the dominant error sources. Thus, dynamic offset cancellation techniques are required to mitigate these errors. Before those dynamic offset cancellation techniques are discussed, it is necessary to first understand the nature and origins of these error sources.

2.2 Low Frequency Errors

2.2.1 Offset

In CMOS technology, the worst-case offset of a differential input pair can be as large as 10 mV [1]. This offset is caused by manufacturing variation or uncertainty. For example, MOS devices exhibit threshold voltage (V_{th}) mismatch because V_{th} is a function of the doping levels in MOS channels and the gates, and these parameters vary randomly from one device to another.

On the other hand, the dimensions of MOS devices suffer from random, microscopic, variations during fabrication and hence there is mismatch between the equivalent lengths and widths of nominally identical transistors. This mismatch can be reduced by using large devices. However, this increases chip area and therefore production cost.

2.2.2 1/f Noise

1/*f* noise is mainly caused by the defects in the interface between the gate oxide and the silicon substrate, so it depends on the "cleanness" of the oxide-silicon interface and may be considerably different from one CMOS technology to another [2, 3]. The typical 1/*f* noise corner frequency of CMOStechnology is in the order of several kHz to tens of kHz, making the 1/*f* noise a dominant error source at low frequencies. Related to the lifetime of the carriers, the 1/*f* noise can be modeled as a function of frequency [2], given by:

$$V_n^2 = \frac{K}{WLC_{ox}f} \tag{2.1}$$

where K is a process-dependent constant in the order of $10^{-25}\text{V}^2\text{F}$, W and L are the width and length of the MOS transistor, C_{ox} is the gate capacitance per unit area, and f is the operation frequency. Generally, 1/*f* noise in PMOS is much lower than NMOS in most technologies.

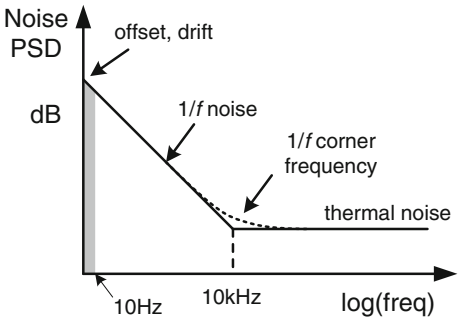

Fig. 2.1 Low frequency noise spectrum for CMOS amplifier

In (2.1), the noise spectral density of the 1/*f* noise is inversely proportional to the frequency. The inverse dependence of (2.1) on the area of the transistor *WL* suggests that to decrease 1/*f* noise, the device area must be increased. However, this again increases chip area.

2.2.3 Drift

Drift is caused by the cross-sensitivity of some error sources to temperature or time. Low drift is a critical requirement for precision temperature measurement (e.g. thermistor bridges and thermocouples), since the drift of the interface electronics can then not be distinguished from the sensor signal itself.

Drift mainly manifests itself as offset drift and gain drift. Thus it can be reduced by suppressing the offset and gain error to a low enough level, and furthermore by dynamically compensating for their temperature drift.

To conclude, Fig. 2.1 depict the low frequency errors in CMOS amplifier. As can be seen in the bandwidth of a few Hz for bridge transducer applications, the main errors are caused by 1/*f* noise, offset, and drift. To mitigate these errors, dynamic offset cancellation techniques can be employed, which will be described in the next section.

2.3 Dynamic Offset Cancellation Techniques

To reduce offset, three types of offset cancellation techniques can be applied: trimming, auto-zeroing, and chopping. Trimming involves measuring and then reducing the offset during production. While this approach can be used to obtain an order-of-magnitude reduction of the offset, it is unable to reduce the initial mV-level offset below a few tens of μV, because offset drift is not compensated for. Moreover, trimming does not eliminate low-frequency noise, such as 1/*f* noise. Dynamic offset cancellation techniques, such as auto-zeroing or chopping are therefore needed to counteract this problem.

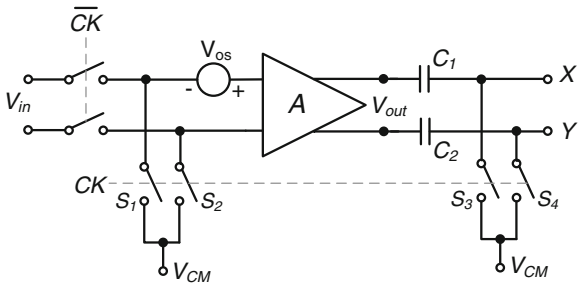

Fig. 2.2 Auto-zeroing with output offset storage

2.3.1 Auto-Zeroing

Auto-zeroing is a discrete-time sampling technique. It involves sampling the offset of the amplifier in one clock phase, and then subtracting it from the input signal in the other clock phase. There are three basic topologies for auto-zeroing [4]: output offset storage (also called open-loop offset cancellation), input offset storage (also called closed-loop offset cancellation) and closed-loop offset cancellation using an auxiliary amplifier.

2.3.1.1 Output Offset Storage

Figure 2.2 depicts an auto-zeroed amplifier with output offset storage. When CK is high, the amplifier is in the auto-zeroing phase in which its inputs are shorted together, driving its output to $V_{\text{out}} = A{\cdot}V_{\text{os}}$. During this period, nodes X and Y are shorted together as well. When all the node voltages are settled, $A{\cdot}V_{\text{os}}$ is stored across C_1 and C_2. When CK turns low, the amplifier enters the amplification phase. The differential input voltage together with Vos is amplified, and stored on C_1 and C_2. Since V_{os} is already stored on C_1 and C_2, V_{X} and V_{Y} does not see V_{os}, which is fully cancelled.

When a switch opens, it injects some charge into the surrounding circuitry. This charge consists of gate-source/drain channel charge and charge injected through the overlap capacitances (also known as clock feed-through). In reality, the charge injection in the switches S_3 and S_4 will not completely cancel. The mismatch charge injection results in a residual offset, given by

$$V_{os,res} = \left(\frac{q_{inj3}}{C_1} - \frac{q_{inj4}}{C_2}\right)/A, \tag{2.2}$$

where q_{inj3} and q_{inj4} are the charge injection caused by switches S_3 and S_4, A is the DC gain of the amplifier. Note that if A is large, $A{\cdot}V_{\text{OS}}$ may saturate the amplifier's output. For this reason, A is typically chosen to be between 10 and 100 [2]. An integrated amplifier with three cascaded auto-zeroed amplifiers with output voltage storage has been described in [4]. In [5], these stages were chopped, resulting in a low drift MOSFET operational amplifier.

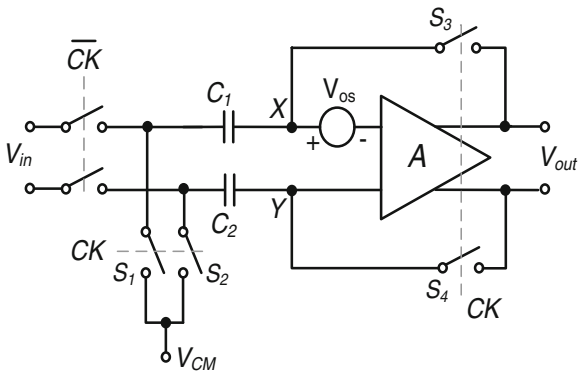

Fig. 2.3 Auto-zeroing with input offset storage

2.3.1.2 Input Offset Storage

The output offset storage technique limits the maximum gain of the amplifier. If a high gain is needed, storing the offset at the input storage capacitance would be a better solution. Figure 2.3 shows the basic principle of input offset storage technique [2]. In the auto-zeroing phase when CK is high, the output and input of the amplifier are shorted together by switches S_1 and S_2, placing the amplifier in a unity-gain configuration.

When the node voltages are settled, the output voltage V_{out} is given by

$$V_{out} = \frac{A}{1+A} \cdot V_{OS}. \tag{2.3}$$

The circuit reproduces the amplifier's offset at nodes X and Y, storing the result on C_1 and C_2. Note that for a zero differential input, the differential output is equal to V_{OS}. Thus, the input-referred offset voltage of the overall circuit equals V_{OS}/A if S_3 and S_4 match perfectly.

If S_3 and S_4 have any mismatch, this will cause mismatch charge injection and, in turn, lead to a residual offset, which is given by

$$V_{res} \approx \frac{V_{OS}}{A+1} + \left(\frac{q_{inj3}}{C_1} - \frac{q_{inj4}}{C_2}\right), \tag{2.4}$$

where q_{inj3} and q_{inj4} are the charge injection caused by switches S_3 and S_4, and A is the DC gain of the amplifier.

From (2.4), the offset V_{os} is suppressed by the gain of the amplifier. The charge injection and the leakage of the capacitors can be reduced by increasing the size of the capacitors, but cannot be suppressed by the gain because the capacitors are directly at the amplifier input.

The drawback of input offset storage and output offset storage is that they introduce capacitors in the signal path. The bottom-plate parasitic of the capacitors decreases the amplifier bandwidth, thus degrading its phase margin and stability.

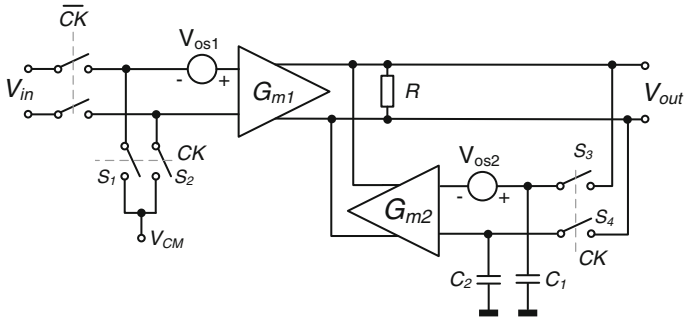

Fig. 2.4 Auxiliary amplifier placed in a feedback loop during offset cancellation

2.3.1.3 Closed-Loop Offset Cancellation with Auxiliary Amplifier

To mitigate the stability issue, closed-loop offset cancellation with an auxiliary amplifier can be used to isolate the offset storage capacitors from the signal path, as shown in Fig. 2.4.

In the auto-zeroing phase, the inputs of G_{m1} are shorted. Thus, the output voltage V_{out} can be calculated as

$$[G_{m1}V_{OS1} - G_{m2}(V_{out} - V_{OS2})]R = V_{out,AZ} \tag{2.5}$$

Thus,

$$V_{out,AZ} = \frac{G_{m1}RV_{OS1} + G_{m2}RV_{OS2}}{1 + G_{m2}R}. \tag{2.6}$$

This voltage is stored on C_1 and C_2 after S_3 and S_4 turn off. The offset voltage referred to the main input is given by

$$V_{OS,res} = \frac{V_{out,AZ}}{G_{m1}R} \approx \frac{V_{OS1}}{G_{m2}R} + \frac{V_{OS2}}{G_{m1}R}. \tag{2.7}$$

The charge injection due to the mismatch of S_3 and S_4 contributes to the offset of G_{m2}. In order to attenuate this charge injection, as seen from (2.7), G_{m2} is usually chosen to be at least 50 times smaller than G_{m1}.

Note that in an auto-zeroed amplifier, half of the clock period is used for auto-zeroing, so the amplified output is only available during part of the clock period. Such amplifiers cannot provide a continuous-time output, unless a ping-pong topology is employed [4, 6].

As seen from the discussion above, these three offset cancellation techniques cancel offset by periodically subtracting the offset obtained during the previous sampling moment. This assumes that the offset does not change too much during the amplification time. Since low-frequency noise and DC offset can not be

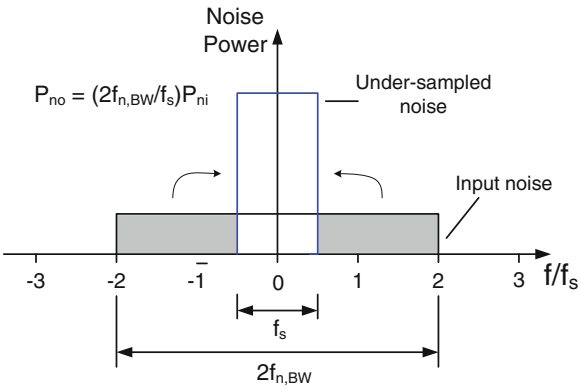

Fig. 2.5 Noise spectrum of a sampled system

distinguished from each other, these techniques also eliminate 1/*f* noise and drift. However, the sampling action of the auto-zeroing techniques affects the amplifier's noise performance at frequencies below the sampling frequency [4].

2.3.1.4 Noise in Auto-Zeroing

As discussed above, auto-zeroing is a sampling technique. To complete settle within a half clock cycle, the noise bandwidth $f_{n,\,BW}$ (determined by the time constant of the system) is usually chosen to be larger than the auto-zeroing frequency f_{AZ}, so that the under-sampled noise folds back to DC, increasing the noise PSD at the baseband.

The amount of folded noise to DC depends on the noise bandwidth $f_{n,\,BW}$ and the auto-zeroing frequency f_{AZ}. An exact quantitative calculation for the folded noise of auto-zeroing can be found in [4, 7]. Since, this is rather complex, a more intuitive explanation of noise folding in auto-zeroing is described here.

The noise folding factor n is defined as the ratio between the noise bandwidth and the auto-zeroing frequency, as given by

$$n = \frac{2f_{n,BW}}{f_{AZ}}. \tag{2.8}$$

Due to under-sampling, the noise power after sampling increases by this factor as compared to that before sampling (Fig. 2.5), thus incurring a noise penalty. This implies that by choosing a small $f_{n,\,BW}$, the folded noise can be restricted. Applying this concept, a slow-settling nulling loop is used in [8, 9] to reduce the noise bandwidth to a fraction of the auto-zeroing frequency. This approach will be discussed in Sect. 2.3.2.

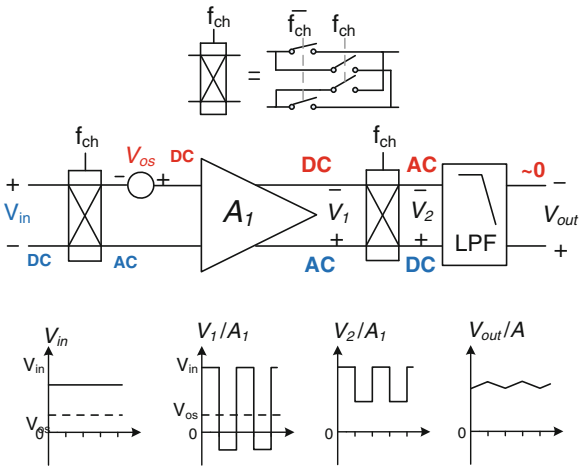

Fig. 2.6 Chopping principle in the time domain

2.3.2 Chopping

Unlike auto-zeroing, chopping is a continuous-time modulation technique that does not cause noise folding. Figure 2.6 shows a chopped amplifier together with its ideal waveforms. The input voltage V_{in} first passes through a chopper driven by a clock at frequency f_{ch}, thus it is converted to a square wave voltage at f_{ch}. Next, the modulated signal is amplified together with its own input offset. The second chopper then demodulates the amplified input signal back to DC, and at the same time modulates the offset to the odd harmonics of f_{ch}, where they are filtered out by a low-pass filter (LPF). This results in an amplified input signal without offset.

Low-frequency errors, such as $1/f$ noise and drift will be modulated and filtered out along with offset. This can be seen in Fig. 2.7, which depicts chopping in the frequency domain. To completely remove the $1/f$ noise, the chopping frequency should be higher than the $1/f$ noise corner frequency. At the beginning, the signal is modulated, and the noise and offset are superposed onto this modulated signal (Fig. 2.7b). After amplification and the second chopper, the modulated signal is demodulated back to DC, while the low-frequency noise and offset are modulated to the harmonics of the chopper frequency, appearing as a chopper ripple at the amplifier output (Fig. 2.7c). A LPF is then used to remove the modulated offset and $1/f$ noise, resulting in a clean low-frequency signal without offset or $1/f$ noise (Fig. 2.7d).

From the above discussion, the offset is amplified by the DC gain of A_1, while the signal is amplified by the effective gain of A_1 at the chopping frequency f_{ch}, To maximize the effective gain of the stage consisting of A_1 and two choppers, the optimum chopping frequency should be around 3 dB bandwidth of A_1 [4].

The amplitude of the chopper ripple can be calculated with the help of the simplified block diagram shown in Fig. 2.8. The chopped offset of the input stage is filtered by the main Miller compensation capacitor C_{M1} and appears as a

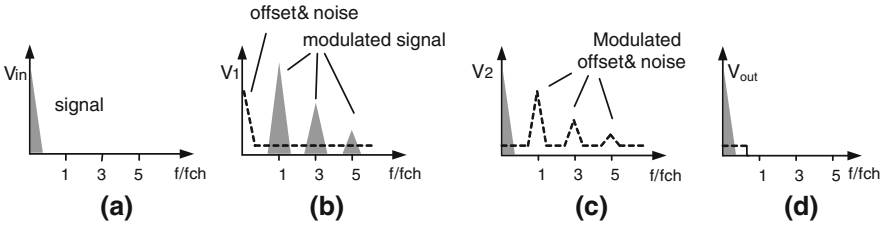

Fig. 2.7 Chopping principle in the frequency domain

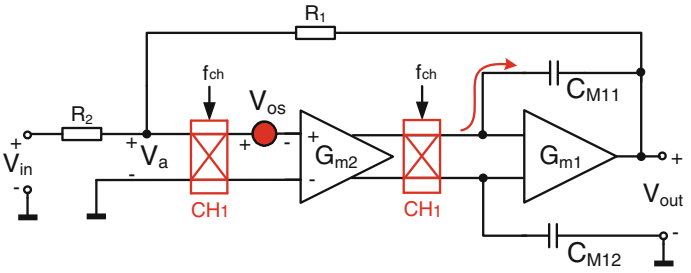

Fig. 2.8 Simplified block diagram of a chopper amplifier

triangular waveform at the output. The peak-to-peak amplitude of the ripple can then be approximated as:

$$V_{out,ripple} = \frac{V_{os} \cdot G_{m2}}{2C_{M1} \cdot f_{ch}}. \tag{2.9}$$

From (2.9), ripple amplitude can be reduced by reducing input-stage offset V_{os} with careful layout, by increasing the chopping frequency f_{ch1} or by increasing the size of the Miller compensation capacitor. For a worst-case 20 mV offset, with $G_{m2} = 250$ μA/V, $C_{M1} = 80$ pF, $V_{DD} = 5$ V, and $f_{ch1} = 40$ kHz, $V_{out,\ ripple} \approx 0.8$ V. This is quite large compared to the amplifier's maximum 5 V output range and so must be suppressed.

2.3.3 Conclusions

Both auto-zeroing and chopping techniques have been introduced. Table 2.1 compares and summarizes these two techniques. Chopping is superior to auto-zeroing because it is a continuous-time modulation technique that does not cause noise folding. However, chopping gives rise to a chopper ripple at the amplifier output. Auto-zeroing does not introduce ripple and its discrete-time nature is well compatible with switched-capacitor circuitry. Since power efficiency is an

Table 2.1 Comparison of auto-zeroing and chopping techniques

	Auto-zeroing	Chopping
Low frequency noise	±	+
Power-noise efficiency	−	+
Ripple	+	−
Residual offset	+	++

Note auto-zeroing removes 1/*f* noise, but causes the noise to fold back to DC, thus auto-zeroing in terms of low-frequency noise is denoted as "±"

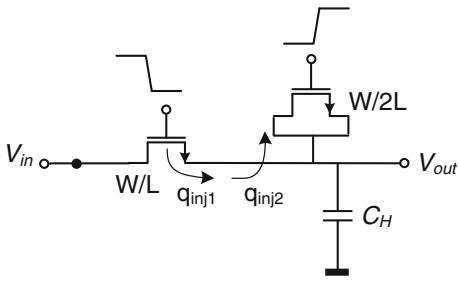

Fig. 2.9 Charge injection compensation using dummy switches

important concern in our work, chopping is applied here. In Sect. 2.5.5, various techniques will be discussed to eliminate the chopper ripple.

2.4 Charge Injection Compensation Techniques in Auto-Zeroed and Chopper Amplifiers

2.4.1 Compensation Techniques for Charge Injection

The residual offset of auto-zeroed amplifiers is mostly determined by charge injection and clock feed-through. To mitigate these two effects in a sampling circuit, several techniques can be applied.

Dummy Switches

Charge injection can be partially compensated for by adding dummy switches that are driven by a complementary clock signal and that inject an amount of charge which compensates for the charge injected by the main switch [10]. The effectiveness of the compensation depends on the matching of the injected charges. A clock signal with a high slew rate can be used to obtain an equal distribution of the channel charge in the main switch's drain and source terminals. A half-size dummy switch can then be used for compensation (Fig. 2.9). However, the assumption of equal splitting of the charge between the source and drain is generally invalid, making this approach less attractive.

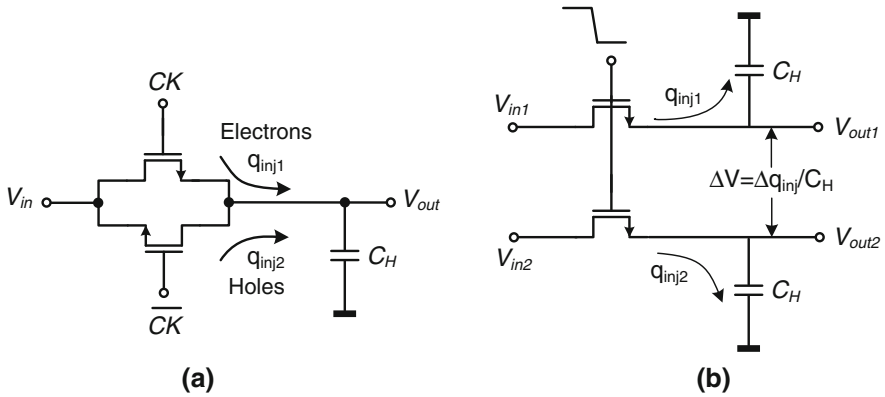

Fig. 2.10 **a** Using complementary switches to reduce charge injection **b** Using differential circuit to suppress charge injection

Using Complementary Switches

Another approach to reduce the charge injection is to use both PMOS and NMOS devices such that the opposite charge packets injected by the two cancel each other (Fig. 2.10a). However, this cancellation is only effective for a limited range of the input signal around half of the supply voltage.

Using a Fully Differential Circuit

The best way to compensate for charge injection is to use fully differential circuitry (Fig. 2.10b). If the charge injection in the two half circuits matches, the charge injection only results in a change in the common-mode voltage. A differential voltage change only results from charge-injection mismatch. With this compensation, a reduction in offset of at least 10 × can be expected.

2.4.2 Charge Injection and Clock Feed-Through in Chopper Amplifiers

For chopper amplifiers, residual offset is mainly caused by the following three issues:

- *Non-idealities in clock timing*
- *Demodulated clock feed-through current spikes*
- *Impedance mismatch between two input nodes*

Firstly, the *non-idealities in the clock timing*, such as clock skew, non-overlap and overlap in chopper clocks introduce residual offset. *Clock skew* is a phenomenon in which the two complementary chopper clocks switch at the different transition moments, as shown in Fig. 2.11a. Assuming the offset is 10 mV and the clock skew is 0.01 %, the resulting offset is 1 μV. To ensure a perfect offset

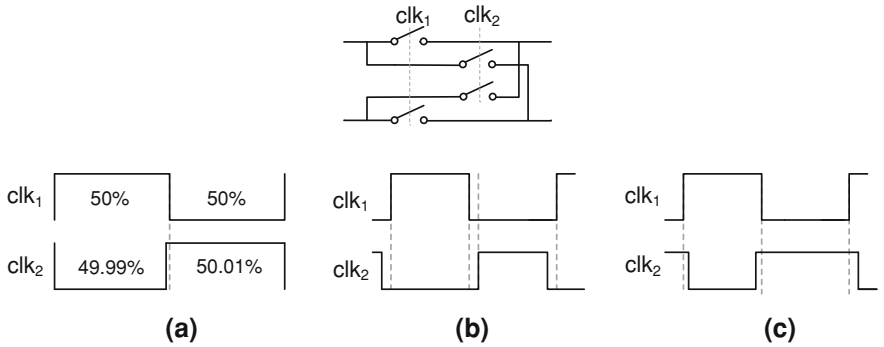

Fig. 2.11 Non-idealities in clock timing **a** Clock skew **b** Non-overlap clock **c** Overlap clock

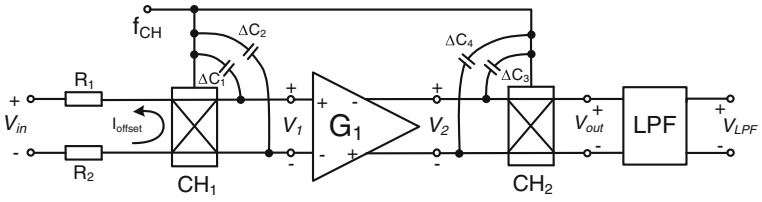

Fig. 2.12 Charge injection model in a chopper amplifier

cancellation, the two complementary chopping clocks must both exhibit 50 % duty cycle and have transitions at the same moments.

Having transitions at the same moment, means that both *non-overlap* and *overlap* of the complementary chopper clocks must be avoided. An NMOS chopper is driven by the non-overlap chopper clocks, as depicted in Fig. 2.11b. A small time gap exists when clk_1 and clk_2 are both low, hence the differential signal paths are being interrupted. This leaves the signal path not attenuated and may cause glitches at the output of the amplifier in between the choppers.

For the overlap chopper clocks (Fig. 2.11c), there is a small time interval when both clocks are high, thus causing a "short circuit" between the differential signal paths. This causes low input impedance and also shorten the amplification time between the choppers. Thus, the effective gain of the amplifier reduces, resulting in increased noise and offset.

Complementary chopper clocks with a 50 % duty cycle and the same transitions can be produced by a non 50 % duty cycle clock and a divider-by-two D-flipflop, as will be described in Sect. 4.6.5. Extra buffers can be added to reduce the rise and fall time.

Secondly, due to *clock feed-through*, the imbalance of parasitic capacitors in the choppers also causes a residual offset [11]. Figure 2.12 illustrates the charge injection due to imbalanced parasitic capacitances of the input and output choppers in a fully-differential chopper amplifier. Figure 2.13 depicts a zoom-in picture of the input and output choppers in which the current spikes caused by imbalanced parasitic capacitances are illustrated.

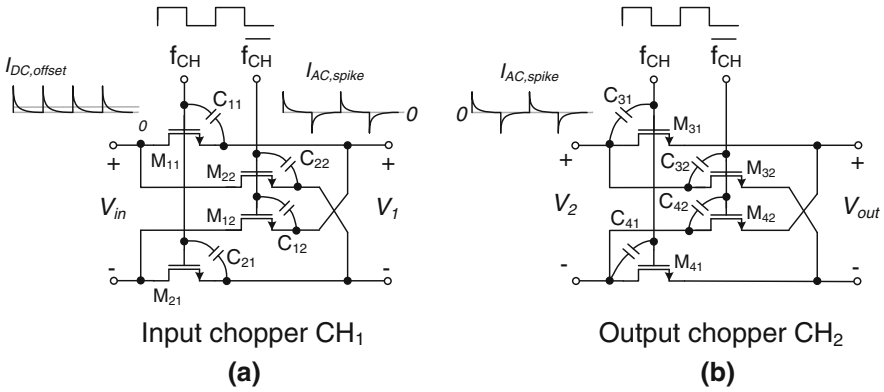

Fig. 2.13 Current spikes caused by imbalanced parasitic capacitances in the input and output choppers CH_1 and CH_2 that give rise to a residue offset

As shown in the input chopper CH_1 (Fig. 2.13a), at the transition moments of the chopper clocks, due to clock feed-through the mismatch between the capacitances C_{11} and C_{12} causes an AC current spike at the node of V_{1+}. For the same reason, the mismatch between C_{21} and C_{22} also leads to another AC current spike at V_{1-}. The difference between these two current spikes results in an AC current spike, as shown in Fig. 2.13a at V_1. This AC current spike is rectified by CH_1, which appears as a DC spike current at the input of CH_1, with an average value given by:

$$I_{offset,DC} = 2(\Delta C_1 - \Delta C_2) \cdot V_{clk} f_{CH} \tag{2.10}$$

where $\Delta C_1 = C_{11} - C_{12}$, and $\Delta C_2 = C_{21} - C_{22}$, V_{clk} is the amplitude of the clock signal, and f_{CH} is the chopper frequency. The DC current spike contributes to the input offset current I_{offset} of the amplifier. This current goes through the series impedance of the chopper and the input signal source, leading to a rectified input voltage spike. The average DC value of the spike results in a residual offset $V_{OS,\ res1}$, as given by:

$$V_{OS,res1} = 2(R_1 + R_2) \cdot (\Delta C_1 - \Delta C_2) \cdot V_{clk} f_{CH} \tag{2.11}$$

where $(R_1 + R_2)$ is the input impedance including on-resistance of the chopper switches and the impedance of the signal source. ΔC_1 and ΔC_2 are the mismatch of clock feed-through capacitances, which is mainly due to the overlap capacitances of the clock line and the source terminals of switches in the input chopper CH_1. If $\Delta C_1 = \Delta C_2$, then no residual offset occurs since it will only result in a common-mode spike.

ΔC_3 and ΔC_4 are the mismatch of clock feed-through capacitances due to the overlap capacitances of the clock lines and the amplifier G_1 output. They will also cause an AC current spike at V_2 (Fig. 2.13b). To provide this AC current spike, the input of G_1 needs to generate an AC voltage spike. This voltage spike is

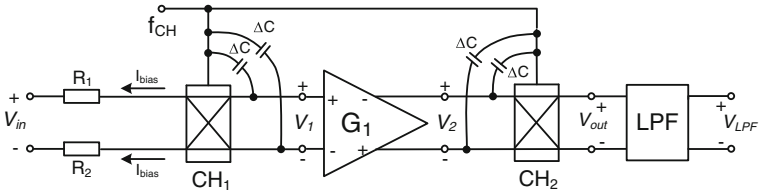

Fig. 2.14 Residual offset due to the bias current and impedance mismatch in a chopper amplifier

demodulated by the input chopper towards the input, resulting in a residual offset $V_{OS,\ res2}$ as given by:

$$V_{OS,res2} = \frac{2(\Delta C_3 - \Delta C_4) V_{clk} f_{CH}}{G_1} \tag{2.12}$$

where $\Delta C_3 = C_{31} - C_{32}$, $\Delta C_4 = C_{41} - C_{42}$, and G_1 is the transconductance of the chopped amplifier. It can be seen that an amplifier with a higher transconductance is less vulnerable to the mismatch of ΔC_3 and ΔC_4. For example, a 10 kHz chopper frequency with $1/G_1 = 5$ kΩ, no source impedance, and a 5 V driving clock voltage would result in a residual offset per unit of capacitance mismatch between ΔC_3 and ΔC_4 of 0.5 μ V/fF. The total residual offset due to clock feed-through is the sum of the offsets given in (2.11) and (2.12).

Thirdly, the *source impedance mismatch* ($\Delta R = R_1 - R_2$) causes another residual offset. The charge injection and clock feed-through due to chopping action cause two s (denoted as I_{bias} in Fig. 2.14) which both flow out of the amplifier's input in the same direction [12]. For bias current calculation, if $\Delta C_1 = \Delta C_2 = \Delta C$ as shown in Fig. 2.14, the average value of the bias current I_{bias} (Fig. 2.14) can be calculated as:

$$I_{bias,DC} = 2\Delta C \cdot V_{clk} \cdot f_{CH} \tag{2.13}$$

The mismatch between input impedances R_1 and R_2 is ΔR, so these two bias currents also generate residual offset, given by:

$$V_{OS,res3} = 2(R_1 - R_2) \cdot \Delta C \cdot V_{clk} \cdot f_{CH} \tag{2.14}$$

If ΔC is 1fF, the chopper frequency f_{CH} is 10 kHz with a 5 V chopper clock, then according to (2.13), the resulting bias current is 0.1 nA. From (2.14), if the mismatch between R_1 and R_2 is 100 kΩ, these two bias currents flow through these two resistors (Fig. 2.14), resulting in an extra residual offset of 10 μV.

It can be seen from (2.11), (2.12) and (2.14) that, the charge injection and clock feed-through of the choppers, cause input bias current, offset current and hence the residual offset. These three errors can be minimized by:

- *Decreasing the chopping frequency*
- *Decreasing the chopper clock amplitude*
- *Balancing or minimizing the overlap capacitors between the clock lines to the input and output terminals of G_1*

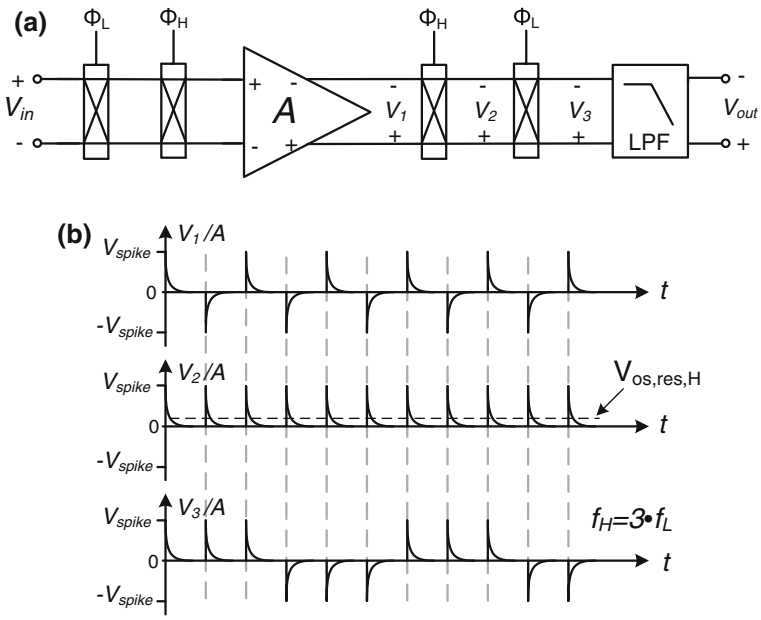

Fig. 2.15 **a** Nested chopper amplifier **b** Charge-injection spikes from the high-frequency choppers are chopped by the low-frequency chopper pair

- *Ensuring matched and balanced input impedance for differential paths reduces residual offset caused by the input bias current*

In Chap. 4, a chopper layout that minimizes the charge injection and clock feed-through will be presented.

2.4.3 Chopper Charge Injection Suppression Techniques

Besides minimizing the charge injection and clock feed-through with the aforementioned methods, there are several techniques that can be used to suppress the demodulated clock feed-through spikes.

Nested-Chopper Technique

Since the residual offset of a chopper amplifier is proportional to the chopper frequency f_{ch}, as expressed by Eqs. (2.11), (2.12) and (2.14), it can be decreased by reducing f_{ch}. However, f_{ch} cannot be lower than the $1/f$ noise corner, otherwise $1/f$ noise can not be completely removed. The nested chopper technique solves this problem by using an extra pair of choppers that run at a much lower frequency. The residual offset of the amplifier chopped by a high frequency chopper clock Φ_H is chopped out by a low-frequency chopper clock Φ_L [13] (Fig. 2.15).

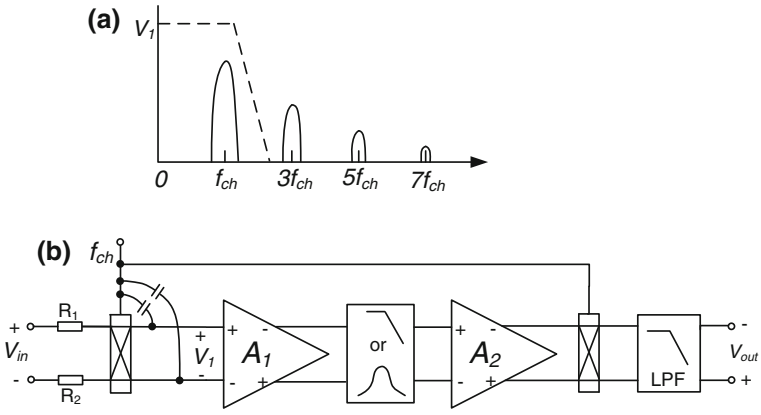

Fig. 2.16 **a** Modulated signal and spike harmonics of V_1 **b** Chopper amplifier with an LP or BP amplifier to remove clock feed-through spikes

The overall residual offset is only limited by the charge injection in the low-frequency chopper, and therefore it is reduced by a factor f_H/f_L, where f_H and f_L are high and low chopping frequencies, respectively.

The implementation of the nested chopper is very simple: only one extra pair of choppers and a low-frequency clock signal are needed. A disadvantage of this approach is that the useable signal bandwidth is reduced, since it is limited by f_L rather than f_H. However, this is not a problem for bridge read-out applications. Nested chopping can be used to chop the complete read-out chain which consists of a preamp and a ΔΣ ADC. The low-frequency chopper spikes at f_L can be filtered out in the decimation filter following the ΔΣ ADC [14]. The nested chopping will be applied to the read-out IC design, as will be discussed in Chap. 5.

Filtering of Spike Harmonics

The chopper clock is a square-wave signal that contains odd harmonics at f_{ch}, $3f_{ch}$, $5f_{ch}$, etc. Most of the energy of the chopper ripple is located at the first harmonics [4]. Therefore, a low-pass (LP) or band-pass (BP) filter can be incorporated between the chopper switches to filter out the chopper harmonics at the high frequencies, at the cost of a small reduction in the signal bandwidth [4] (Fig. 2.16a). A LP filter was implemented in [15] to filter the spikes, achieving a 5 μV offset (Fig. 2.16b). A BP filter implementation is presented in [16] to suppress the DC offset. Here, the chopping frequency is designed to track the center frequency of the BP filter. It achieves an offset of less than 600 nV. However, a disadvantage of this technique is the significant amount of extra circuitry required.

Chopper with Guard Band

Another approach to filter out clock feed-through spikes is to introduce a small guard time in the output chopper switch that prevents the spikes caused by the input chopper from being demodulated, as shown in Fig. 2.17b. This technique has

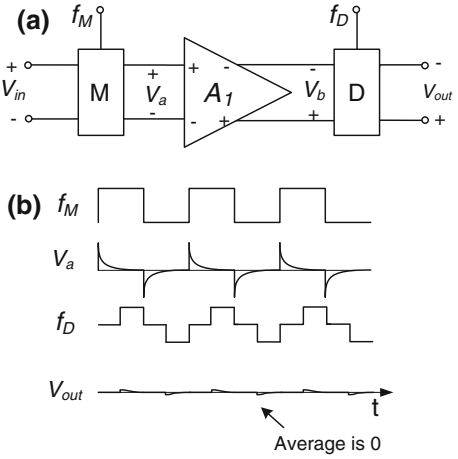

Fig. 2.17 **a** Modulated amplifier **b** Guard band clock diagram

been used in [17–19] for custom sensor interfaces. An average offset of 200 nV has been achieved in [18]. However, the residual offset with the guard band technique is limited by the matching between the shape of the spike and the guard time delay. Moreover, the output signal is no longer continuous-time due to the gap in the guard time since V_{out} just holds the value before the guard time starts, thus incurring a slight loss of gain and noise aliasing.

2.4.4 Conclusions

For the auto-zeroed amplifier, charge injection determines the residual offset. In the chopper amplifier, the residual offset is caused by the non-ideality in clock timing, the demodulated clock feed-through current spikes and the impedance mismatch between two input nodes. *To conclude*, symmetry, matching and balancing the parasitics are essential to achieve low residual offset in chopper amplifier.

2.5 Dynamic Offset Compensated Operational Amplifiers

This section discusses the basic principle of feedback and then reviews several precision operational amplifiers that employ the dynamic offset cancellation techniques discussed above, i.e. auto-zeroing and chopping. These amplifier topologies include ping-pong, offset stabilization and chopper offset stabilization.

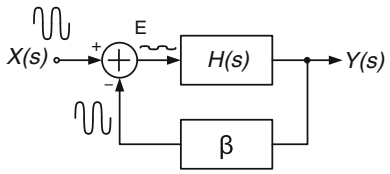

Fig. 2.18 Block diagram of a general feedback system

2.5.1 Feedback

Feedback is a powerful technique that has found wide application in high-precision signal processing. Figure 2.18 shows a negative feedback system, where $H(s)$ and β denote the high gain amplifier and the passive feedback network, respectively. Part of the output signal is redirected back to the input and compared to the incoming signal. The loop accurately controls the output to produce an amplified or processed replica of the input signal.

The error, which is indicated as E in Fig. 2.18, is given by:

$$E(s) = X(s) - \beta Y(s) = X(s)\frac{1}{1 + \beta H(s)} \tag{2.15}$$

From (2.15), the higher the loop gain $\beta H(s)$, the more effectively the error E is minimized. This means that a feedback loop with high loop gain can be applied to reduce an error.

This feedback concept will be used in the work presented in Chaps. 4 and 5 to reduce the offset and gain error of an amplifier. Generally, the feedback concept is used in operational amplifiers to obtain an accurate gain determined by $1/\beta$. The next few sections will review several precision operational amplifier topologies.

2.5.2 Ping-Pong Operational Amplifier

As discussed before, the auto-zeroing technique is not directly suitable for use in a continuous-time general purpose amplifier, since the amplified output signal is only available during one half of the clock period. To obtain a continuous-time output signal, the ping-pong technique can be used. This involves the use of two auto-zeroed amplifiers [6], as shown in Fig. 2.19. When one amplifier is being auto-zeroed, the other is being used to amplify the signal. The same output stage is shared by the two auto-zeroed amplifiers. Furthermore, the combination of auto-zeroing and chopping is employed to achieve a noise PSD of 20 nV/$\sqrt{}$Hz from DC to 1.5 kHz, which rises to 48 nV/$\sqrt{}$Hz at 20 kHz. It consumes a supply current of 800 μA.

Figure 2.20 shows the noise spectrum of chopping, auto-zeroing and the combination of these two. As seen from Fig. 2.20b, chopping modulates low-frequency $1/f$ noise to the chopping frequency, thus achieving a clean and flat noise

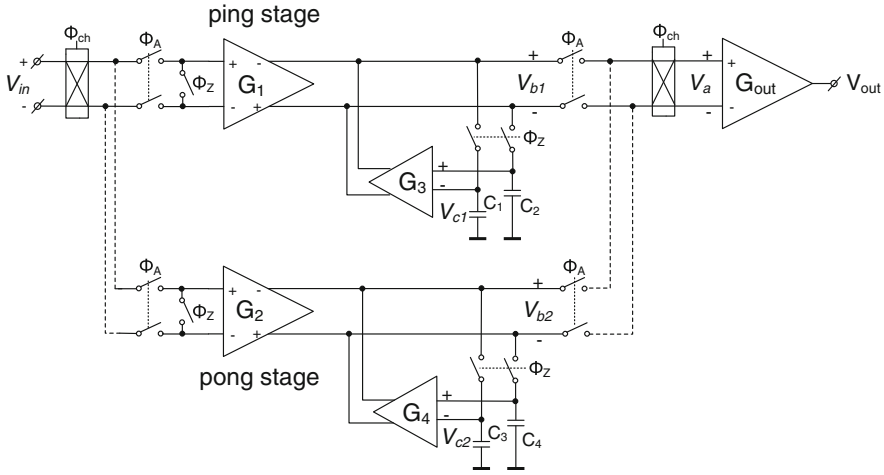

Fig. 2.19 Basic concept of the ping-pong operational amplifier

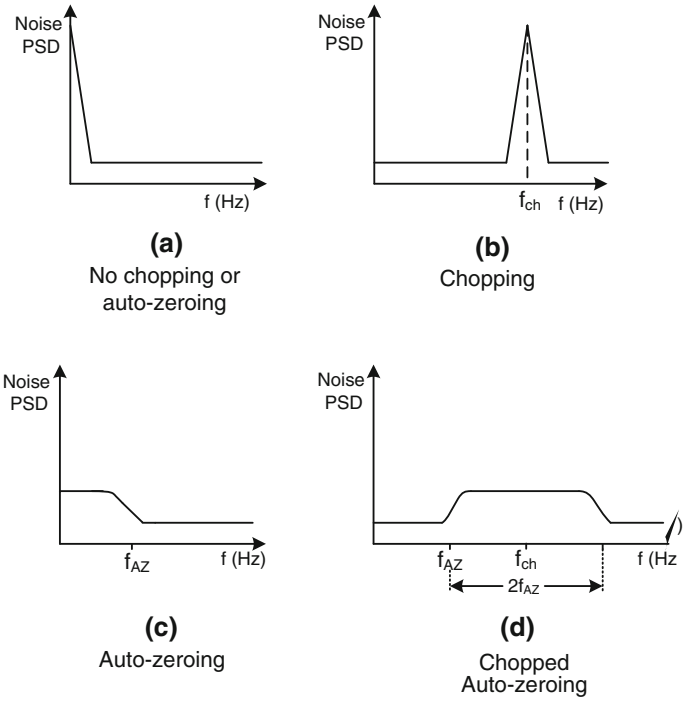

Fig. 2.20 Input-referred noise PSD of chopping, auto-zeroing and the combination of the two ($f_{ch} = 2f_{AZ}$)

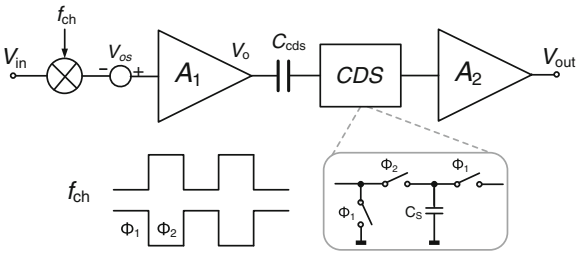

Fig. 2.21 Simplified chopper-CDS block diagram

spectrum at low frequencies, but with ripple at the chopping frequency. Auto-zeroing involves sampling, thus causing increased noise at DC due to aliasing (Fig. 2.20c). In their combination, since the input stage is chopped at twice the auto-zeroing frequency, this noise is then modulated away from DC to f_{ch} (or $2f_{AZ}$) [6] (Fig. 2.20d).

A disadvantage of the ping-pong technique is that spikes are introduced because the voltages V_{b1} and V_{b2} at the output of the first stage amplifiers have to switch between the offset compensating voltages V_{c1}, V_{c2} and the voltage required at the input of the output amplifier V_a. This results in spikes at the output. This effect can be reduced by replacing C_1-C_4 with active integrators with the same input CM voltage as the output stage G_{out} [1]. However, spikes still remain because switching occurs within the signal path.

2.5.3 Chopper-CDS Operational Amplifier

As a hybrid of chopping and auto-zeroing, a ripple-free operational amplifier is proposed in [20] that uses input chopping and correlated double sampling (CDS) for demodulation. As shown in Fig. 2.21, the AC-coupling capacitor C_{cds} is inserted between the first and the second stage, removing the offset from the first stage without causing ripple. The CDS then demodulates the signal back to DC.

Since CDS operates on the modulated input signal, the folded noise spectrum due to sampling is also around the f_{CDS}, which is equal to the chopping frequency. This implies that the gain of A_1 around the chopping frequency f_{ch} should be large since it suppresses the folded noise of CDS. The DC gain of A_1 should be low enough so that the amplified offset and $1/f$ noises do not saturate A_1. A_1 is implemented with a band-pass response that exhibits low gain around DC but high gain at f_{ch}. In the worst case, the amplified offset can still be too large. A band-reject passive feedback network is used that decreases the gain at low and high frequencies, but not at the chopping frequency. In this way, the DC gain of A_1 is reduced further. However, this scheme increases the circuit complexity. It achieves a 2 μV offset and a noise PSD of $37\text{nV}/\sqrt{\text{Hz}}$ with an NEF of 5.5.

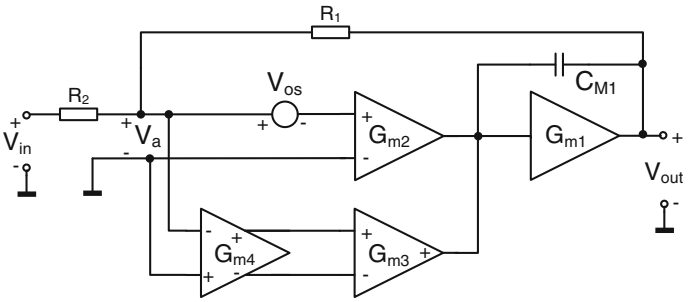

Fig. 2.22 The concept of the offset-stabilized operational amplifier

2.5.4 Offset-Stabilized Operational Amplifiers

Offset stabilization is another technique that can be used to design a precision wideband amplifier. The basic concept of offset-stabilization is shown in Fig. 2.22. A main operational amplifier G_{m2} with an offset V_{os}, is being offset-stabilized by a stabilizing amplifier G_{m4} with a hypothetical zero offset. G_{m3} acts as an auxiliary input of the main amplifier. The stabilizing amplifier G_{m4} applies a voltage to the inputs of G_{m3}, which drives a current to the output of G_{m2} to compensate for its input offset voltage [4]. The feedback resistors R_1 and R_2 determine the gain of the amplifier.

With the negative feedback configuration, the differential input voltage V_a of G_{m2} is approximately equal to the offset V_{os}. The residual offset due to the finite gain of the combined amplifier can then be expressed as:

$$V_{os,res} \approx \frac{A_{m2}}{A_{m4}A_{m3}} V_{os} \tag{2.16}$$

where A_{m4}, A_{m3} and A_{m2} are the DC voltage gains of the stabilizing amplifier G_{m4}, the main amplifier G_{m3}, and the auxiliary input of the main amplifier G_{m2}, respectively. Equation (2.16) indicates that the combined voltage gain of G_{m4} and G_{m3} has to be much larger than the voltage gain of the main amplifier G_{m2}. If G_{m3} is 50 times lower than G_{m2}, then to reduce a 10 mV worse-case offset to 1 μV, G_{m4} must have a minimum voltage gain of 114 dB. To maintain stability, frequency compensation must also be implemented.

This topology can also be seen as a multi-path amplifier in which the cascode of G_{m4}, G_{m3} and G_{m1} form the high-gain low-frequency path, and the main amplifier G_{m2} and G_{m1} form the low-gain high-frequency path. Low-frequency characteristics will, therefore, be determined by the low frequency path. In other words, the low-frequency noise, residual offset and gain accuracy are determined by G_{m4}, while the unity gain frequency is determined by the main amplifier G_{m2}. To achieve μV-level offset, the offset-stabilization loop needs to be chopped or auto-

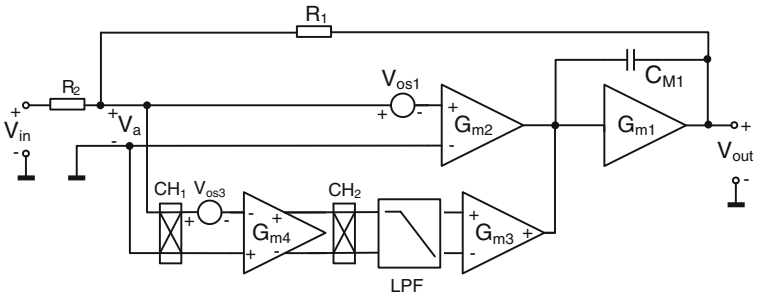

Fig. 2.23 Chopper offset-stabilized amplifier

zeroed. Chopping is more power-efficient than auto-zeroing, therefore chopper offset-stabilized amplifiers will be discussed in the next section.

2.5.5 Chopper Offset-Stabilized Operational Amplifiers

Figure 2.23 shows a chopper offset-stabilized amplifier. Since G_{m4} determines the low-frequency noise and offset of the overall amplifier, G_{m4} is chopped to eliminate its $1/f$ noise and offset. The chopper amplifier composed of chopper CH_1, stabilizing amplifier G_{m4}, and chopper CH_2 senses the offset of the main amplifier G_{m2}. A LPF suppresses the chopper ripple due to the chopped offset of G_{m4}. The residual offset due to finite gain is expressed by (2.16).

The effects of chopping on the noise of chopper offset-stabilized amplifier are depicted in Fig. 2.24. The offset and $1/f$ noise of G_{m4} are modulated to the chopping frequency f_{ch}, and then removed by the LPF. For effective suppression of $1/f$ noise, the bandwidth of the stabilizing loop as well as the chopper frequency f_{ch} should, therefore, be larger than the $1/f$ noise corner frequency of the main amplifier. To let the low-frequency noise be dominated by the low-frequency path, the –3 dB frequency of the LPF should be chosen higher than the $1/f$ corner frequency of the main amplifier G_{m2}, and the chopper frequency should be high enough and thus the chopper ripple can be filtered out properly.

The LPF that filters out the chopper ripple (Fig. 2.23) can be implemented in several ways, e.g. a continuous-time integrator, a sample-and-hold notch filter, or a continuous-time notch filter, which will be described as follows.

2.5.5.1 Continuous-Time Integrator

One way to implement the LPF is by using the integrator composed of G_{m5}, C_{51} and C_{52} to filter out the chopper ripple [21], as shown in Fig. 2.25. It depicts a

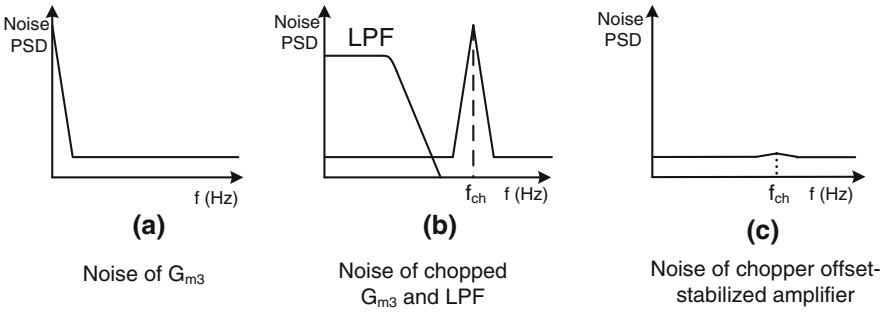

Fig. 2.24 Noise in chopper-stabilized amplifiers

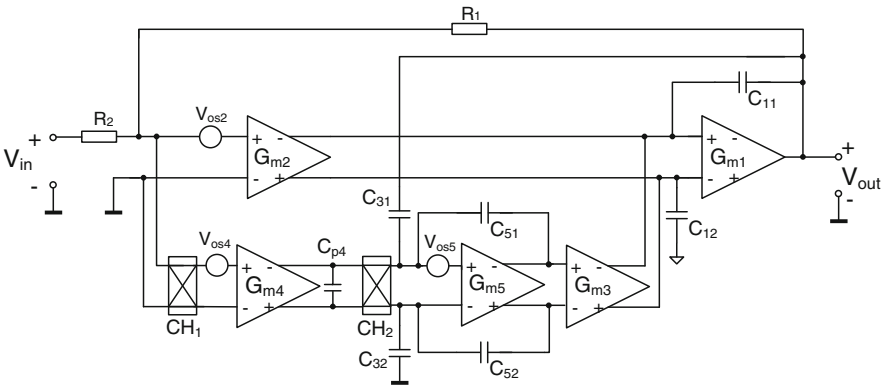

Fig. 2.25 Chopper offset-stabilization amplifier using an active integrator and multi-path hybrid-nested Miller compensation

multi-path architecture that employs this technique in combination with hybrid Miller compensation [22, 23]. The gain stages G_{m2} and G_{m1} form the high-frequency low-gain path, while the transconductances G_{m4}, G_{m5}, G_{m3} and G_{m1} form the high-gain low-frequency path. To realize a frequency response with a smooth roll-off, the unity gain frequency of both paths should be [23].

$$f_{0dB} = \frac{G_{m4}}{2\pi C_3} = \frac{G_{m2}}{2\pi C_1} \tag{2.17}$$

where C_3 and C_1 are the values of capacitors C_{31} (or C_{32}) and C_{11} (or C_{12}), respectively.

The modulated offset V_{os4} of G_{m4} is filtered by the integrator consisting of G_{m5}, C_{51} and C_{52}. However, the integrator needs very large capacitors to obtain a low cut-off frequency. Hence in reality, a residual chopper ripple in the form of a triangular wave appears at the integrator output. Furthermore, due to the action of the chopper CH_2, the offset of G_{m5} (V_{os5}) appears as a square-wave voltage over the capacitor C_{p4}, charging and discharging this capacitor. The resulting

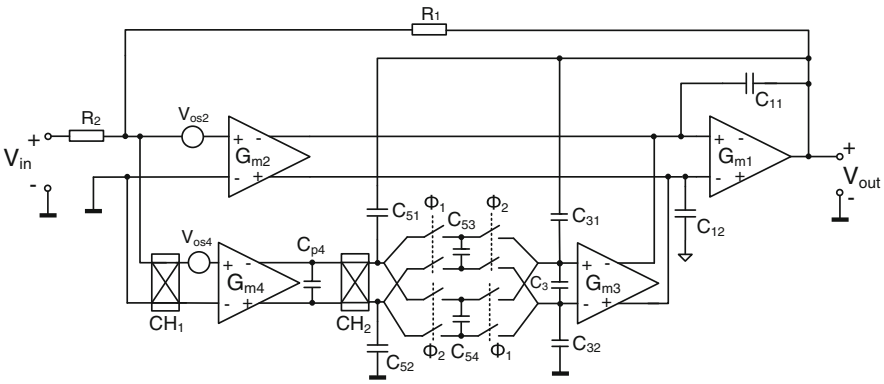

Fig. 2.26 Multi-path operational amplifier with an embedded sample-and-hold circuit

alternating current at the output of G_{m4} is demodulated by chopper CH_1, causing a residual offset.

To eliminate this residual offset, the parasitic capacitor C_{p4}, or the offset V_{os5} of the integrator, must be minimized. The parasitic capacitor C_{p4} can be minimized by choosing small dimensions for the transistors that are connected to the output terminals of G_{m4}. Furthermore, C_{p4} can be minimized to ensure a fully symmetric and balanced layout. To reduce offset V_{os5}, auto-zeroing can be used [21]. However, it increases the complexity and power consumption of the design. Since the focus of this thesis is to design a low- noise amplifier with good noise-power efficiency, the topology with G_{m5} auto-zeroed will not be elaborated further.

2.5.5.2 Sample-and-Hold Notch Filter

An alternative solution for implementing the LPF in Fig. 2.23 are to use a switched-capacitor (SC) sample-and-hold circuit to sample the chopper ripple at the output of the integrator, as shown in Fig. 2.26. It shows an operational amplifier with multi-path hybrid-nested Miller compensation. A LPF is implemented with a SC notch filter consisting of the switches driven by Φ_1 and Φ_2 and the capacitors C_{53} and C_{54} [24]. The switches sample the chopper ripple at the zero-crossing points. The notch positions of the Sinc filter are located at multiples of the chopper frequency, and thus are accurately determined by the chopping clock.

This notch filter acts as a passive integrator. To compensate for the extra pole introduced by the notch filter, the capacitors C_{51} and C_{52} are introduced for the same reason as the hybrid-nested Miller compensation [23]. Capacitors C_{31} and C_{32} are theoretically not needed, but they help to maintain local loop stability. The capacitor C_3 helps to limit the bandwidth of the low-frequency path so that the delay caused by the notch filter does not cause instability [24].

However, this technique still involves sampling, and so still incurs a certain noise-folding. More importantly, the sample-and-hold filter exhibits a Sinc

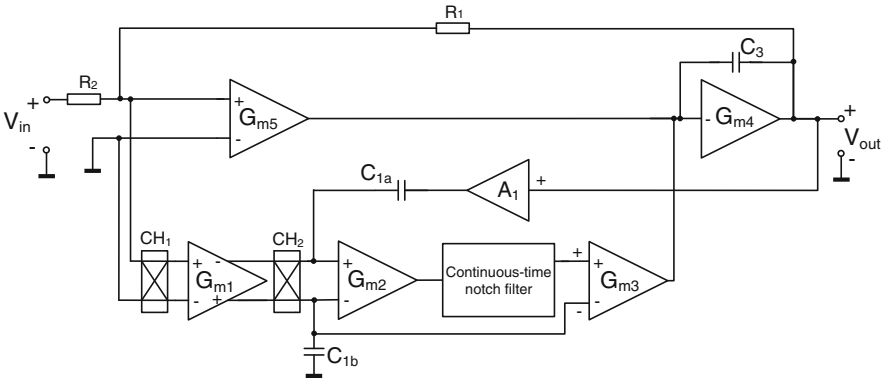

Fig. 2.27 Multi-path operational amplifier with an embedded continuous-time notch filter

filtering response, creating a significant phase shift at the chopping frequency. Overcoming these phase shift complicates the frequency compensation in the amplifier.

2.5.5.3 Continuous-Time Notch Filter

As a counterpart of SC implementation, the notch filter also can be implemented in a continuous-time (CT) fashion. Figure 2.27 shows a CT notch filter incorporated in the low-frequency path to filter out the chopper ripple [25] in a multi-path operational amplifier. Additionally, a buffer A_1 is used to allow feedback through a compensation capacitor C_{1a} for the low-frequency path, thus preventing the chopper ripple at the output of CH_2 from feeding forward through C_{1a} to the output of the amplifier.

The disadvantage of this approach is that the notch filter suppresses the ripple in an open-loop structure. This implies that the chopping frequency derived from the time constant of the on-chip relaxation oscillator needs to be well-matched to the notch position of the CT filter, which is also determined by the product of certain resistors and capacitors. This frequency tracking is not an issue for the SC notch filter [24], since the notch positions are precisely determined by the chopping clock. Furthermore, if a tunable chopping frequency is desired, a phase-locked loop (PLL) is then required to track the external chopping frequency to ensure that the RC time constant of the CT notch filter closely tracks the locking frequency. Otherwise, trimming is required to tune the notch location in the CT notch filter.

2.5.5.4 Auto-Correction Feedback Loop

Another way to suppress the chopper ripple is to use an auto-correction feedback (ACFB) loop to null the offset in a chopper multi-path operational amplifier [26, 27].

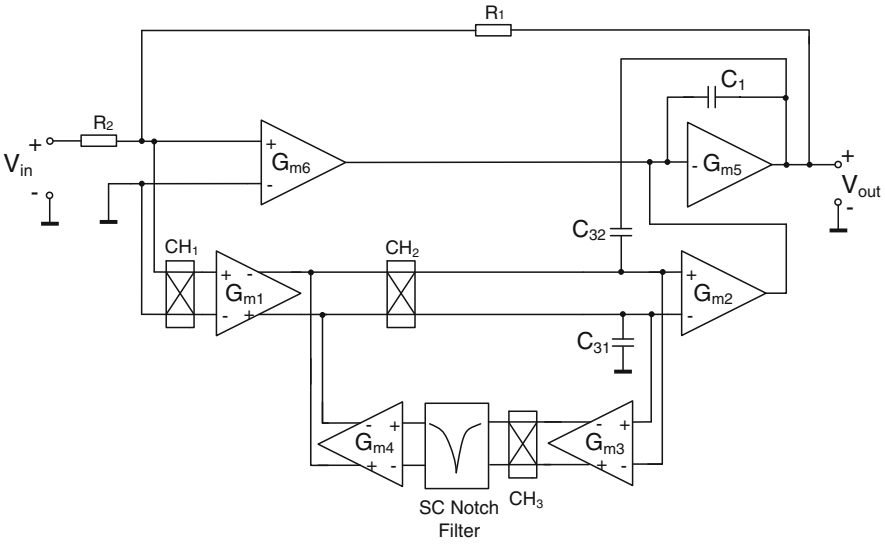

Fig. 2.28 Multi-path operational amplifier with an auto-correction feedback loop

Its block diagram is shown in Fig. 2.28. Unlike the designs presented in [24, 25] which employ notch filters in the signal path to suppress the chopper ripple, this approach uses a feedback loop outside the signal path. Therefore, it does not cause any phase shift in the signal path. However, the stability of the feedback loop itself needs to be taken care of. This is because the notch filter creates a significant phase shift at the chopping frequency, and the unity gain frequency of the ACFB loop must occur well below the chopping frequency to ensure the loop stability. Increasing the unity-gain frequency speeds up the settling of the loop. However, a higher chopping frequency is then required, thus increasing the charge injection and the offset.

Moreover, since the sensing points of the loop are the virtual ground of G_{m2}, they are relatively "quiet". The DC gain of the loop is limited because of the small ripple excitation. A ripple reduction of only 43 dB [26] is achieved. Furthermore, the SC notch filter (NF) causes sampling noise at DC. This noise is modulated by CH_2 and creates a peak output noise PSD around the chopping frequency.

2.6 Conclusions

Table 2.2 summarizes the performances of precision operational amplifiers that achieve μV-level offset. They apply different techniques to suppress chopper ripple. One technique is to use auto-zeroing to reduce the initial offset of the amplifier [6, 21]. However, the increased low-frequency noise due to noise folding leads to a noise penalty, i.e. extra power dissipation is needed to meet a given noise specification (NEF = 21.8 and 153). A band-pass filter can be implemented between the choppers to suppress the DC offset, so as to eliminate the output

Table 2.2 Comparison of precision operational amplifiers

	Tang [6]	Witte [21]	Burt [24]	Kusuda [27]	Belloni [20]
Year	2002	2006	2006	2011	2010
Noise PSD (nV/$\sqrt{}$Hz)	20	15	55	5.9	37
Chopping frequency (kHz)	15	32	125	200	500
Offset (μV)	3	1.5	3	0.78	1.94
Input bias current (pA)	40	–	70	72	–
GBW (kHz)	2500	1370	350	4000	260
Supply current (Iq)(μA)	800	700	17	1470	14.4
Die area(mm^2)	0.67	3.6	0.7	1.26	1.14
NEF [28]	21.8	153	8.7	8.7	5.5
GBW/Iq (kHz/μA)	3.1	2	20.6	2.7	18
Rail sensing capability	No	Yes	Yes	Yes	Yes
Ripple reduction technique	Auto-zeroing	Auto-zeroed integrator	SC notch filter	Auto feedback loop	Chopper-CDS

chopper ripple [16]. However, the chopping frequency needs to track the center frequency of the band-pass filter, which requires significant amount of extra circuitry.

A switched-capacitor [24] or a continuous-time notch filter [25] can be embedded in a multi-path offset stabilized operational amplifier to reduce the chopper ripple. However, the SC notch filter [24] involves sampling thus causing noise folding. The issue associated with the CT notch filter [25] is that the notch filter suppresses the ripple in an open-loop structure. To effectively suppress the chopper ripple, the notch frequency of the CT filter needs to closely track the chopping frequency, which could be limited by the RC spread in the CT notch filter. Another technique uses an auto-correction feedback loop [26] to suppress the chopper ripple. However, since the ripple sensing points are at the "quiet" virtual grounds of the output stage, the limited loop gain restricts the ripple suppression ratio.

In addition, the notch filters generate excess phase shift, meaning that the chopper clock frequency must be relatively high (> 125 kHz) to maintain stability in the signal path [24, 25] or in the feedback loop [26]. Such a high chopping frequency increases charge injection errors, and hence increases input offset, given the same noise level and process parameters. The chopper-CDS scheme [20] uses an AC-coupled capacitor to block the offset, thus generating no chopper ripple. However, this technique also necessitates a high chopping frequency of 500 kHz, resulting in a relatively low input impedance and a high input bias current.

Therefore, innovative solutions need to be explored to eliminate the chopper ripple without causing the above-mentioned issues: noise aliasing, frequency tracking, limited loop gain, and excess phase shift (high chopping frequencies). To counteract these problems, a new ripple reduction technique will be proposed in Chap. 4.

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Chapter 3
Current-Feedback Instrumentation Amplifiers and Gain Accuracy Improvement Techniques

As discussed in Chap. 1, compared to other instrumentation amplifier topologies, the current-feedback instrumentation amplifier (CFIA) is more suitable for bridge read-out because of its high CMRR [1, 2], rail-sensing capability [1], high input impedance and power efficiency [3, 4].

The main disadvantage of a CFIA is its limited gain accuracy, which is determined by the mismatch between the input and feedback transconductors [1, 5]. These also limit its input range and linearity. Although the limited input range is often not a problem for bridge readout applications, where the input signal is in the millivolt range, it limits the usefulness of the CFIA in other applications.

This section will review several previous precision CFIAs. It will be shown that the gain accuracy and linearity of a CFIA can be improved by using resistor-degeneration and dynamic element matching (DEM).

3.1 Current-Feedback Instrumentation Amplifier

Figure 3.1 shows a simplified block diagram of a current-feedback instrumentation amplifier (CFIA). The input transconductor G_{m2} and feedback transconductor G_{m3} convert the input and feedback voltages into the corresponding currents. Their difference is then nulled by the gain of G_{m1}. If the loop gain is high enough, the overall feedback ensures that the output currents of G_{m2} and G_{m3} cancel out each other and thus the closed-loop gain of the amplifier is given by:

$$Gain = \frac{G_{m2}}{G_{m3}} \frac{R_1 + R_{21} + R_{22}}{R_1} \tag{3.1}$$

In the CFIA, the signal is carried in the current domain. This is a very important point, because summation or subtraction in the current domain is much easier than that in the voltage domain. It opens various possibilities for compensation or calibration of some error sources, such as offset; these will be discussed in Chaps. 4, 5 and 6.

R. Wu et al., *Precision Instrumentation Amplifiers and Read-Out Integrated Circuits*, Analog Circuits and Signal Processing, DOI: 10.1007/978-1-4614-3731-4_3,

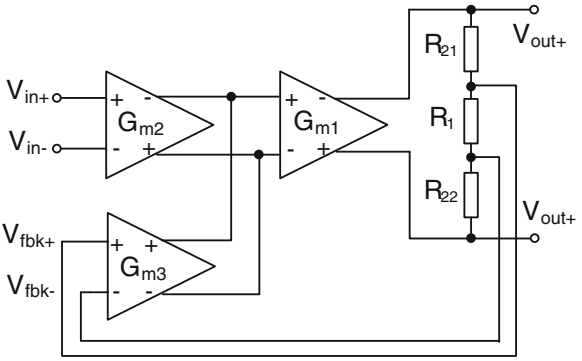

Fig. 3.1 Current-feedback instrumentation amplifier

From (3.1), the gain accuracy of the CFIA will be mainly determined by the mismatch of the input and feedback transconductances, provided that precision (0.01 %) gain-setting resistors are used. Furthermore, the CFIA's input range and linearity will also be limited by these transconductors. Available techniques to address these issues will be discussed later in this chapter.

Next, let us review the history of CFIAs. They can be classified into two categories: *indirect* current-feedback and *direct* current-feedback instrumentation amplifiers. Note that the CFIA is also referred to as "differential differential amplifier" (DDA) in [6] and "differential difference amplifier" (DDA) in [2].

3.1.1 Indirect Current-Feedback Instrumentation Amplifier

The first CFIA [7] was reported in 1971 and uses *indirect* current-feedback (Fig. 3.2). Two high-gain voltage amplifiers A_1 and A_2 force the current V_{in}/R_1 flowing though the degeneration resistors R_1 to also flow through R_2. The amplitude of the latter current is equal to V_{fbk}/R_2. Therefore, the gain is mainly determined by the resistor ratios:

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_1}\frac{R_3 + R_4}{R_4} \tag{3.2}$$

Since the input and feedback transconductances isolate the input and feedback CM voltages, a high CMRR (>120 dB) can be achieved. However, the drawback of this topology is that the feedback loop is rather complex, consisting of the input transconductance, voltage amplifiers A_1 and A_2, and the feedback transconductance. The multiple stages within the feedback loop leads to stability issues and slow settling.

To overcome the stability issue, the next two topologies use only one high-gain amplifier. Figure 3.3 shows an indirect CFIA topology [1] with one feedback amplifier A_1. The current sources I_1, I_2, I_3 and I_4 are nominally equal, as are I_5 and I_6. The loop amplifier A_1 forces the differential current flowing through R_1 to also flow through R_2 by applying the required voltage V_{fbk} to the inputs of Q_{21} and Q_{22}.

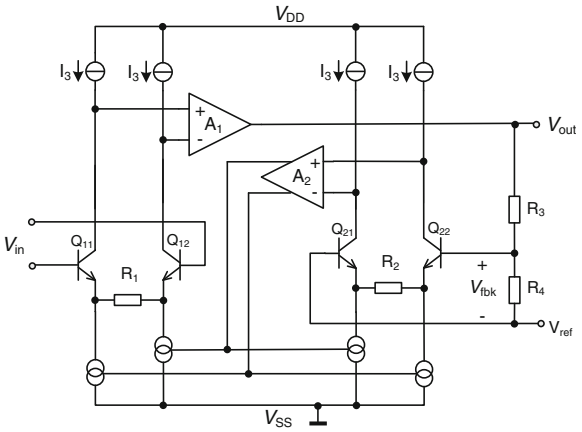

Fig. 3.2 CFIA using two feedback amplifiers

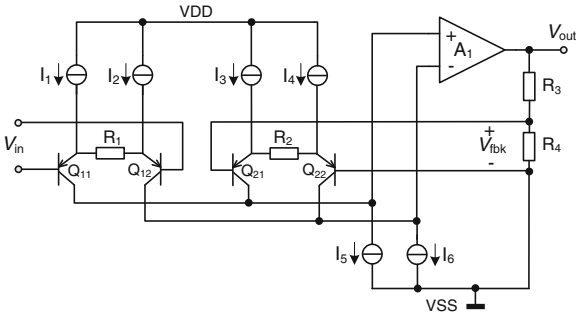

Fig. 3.3 Indirect current-feedback instrumentation amplifier

Due to the nonlinearity of the differential pairs, the currents flowing through Q_{11} and Q_{12} and of Q_{21} and Q_{22} are not linear functions of V_{in} and V_{fbk}, respectively. From (3.1), this non-linearity is cancelled to first order when the differential pairs are nominally identical, i.e. the transistors match and $R_1 = R_2$. The closed-loop gain is then given by

$$\frac{V_{out}}{V_{in}} = \frac{R_3 + R_4}{R_4} \tag{3.3}$$

An important advantage of the indirect CFIA topology is that by using PNP (or PMOS) differential pairs as the input and feedback transconductors, the common-mode (CM) input range includes ground [1].

3.1.2 Direct Current-Feedback Instrumentation Amplifier

Another category of CFIA uses *direct* current feedback, as shown in Fig. 3.4. Here, the input and feedback transconductances share the same bias current, thus

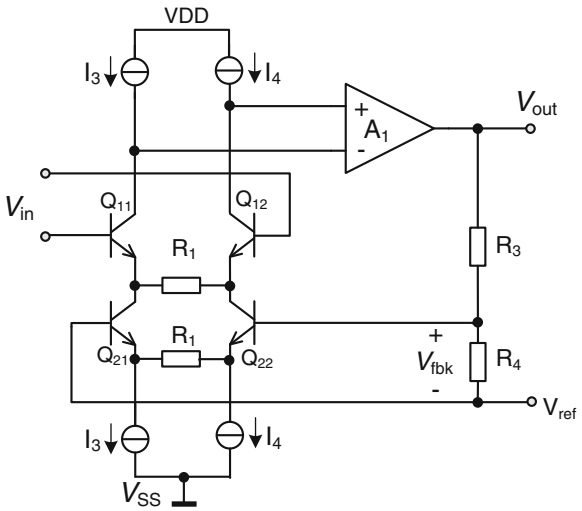

Fig. 3.4 Direct current-feedback instrumentation amplifier

the input and feedback signal currents directly compensate each other. This is in contrast with the *indirect* CFIA of Fig. 3.3, in which the two differential pairs do not share the same bias current. Because of this, the direct CFIA has been used in low-power biomedical applications where low power consumption is critical [9]. This topology was later implemented in CMOS [10]. However, the stacking of two transconductance stages increases the minimum supply voltage and reduces the input CM range, which cannot include ground [1]. Furthermore, since I_3 and I_4 are equal, the currents flowing through Q_{11} and Q_{12} are also equal. However, the current flowing through Q_{21} and Q_{22} is signal-dependent, which leads to signal dependent nonlinearity.

In summary, the direct CFIA is suitable for low-power design, while the indirect CFIA is better for low-voltage designs and for applications that require a large input CM range that may include one of the supply rails. As discussed in Chap. 1, bridge sensors require read-out electronics to have a CM input range that includes at least one rail. Therefore, the work presented in this thesis will mainly focus on the *indirect* CFIA. For simplicity, we will refer to this as a "CFIA" in the rest of this thesis.

3.2 Precision Current-Feedback Instrumentation Amplifiers

The CFIA can be seen as a merged version of the two-opamp topology in which the output stages are shared. Thus, the dynamic offset cancellation techniques applied in precision operational amplifiers can also be used in CFIAs. This section reviews several CFIAs that employ chopping, auto-zeroing and offset stabilization techniques to mitigate low-frequency errors.

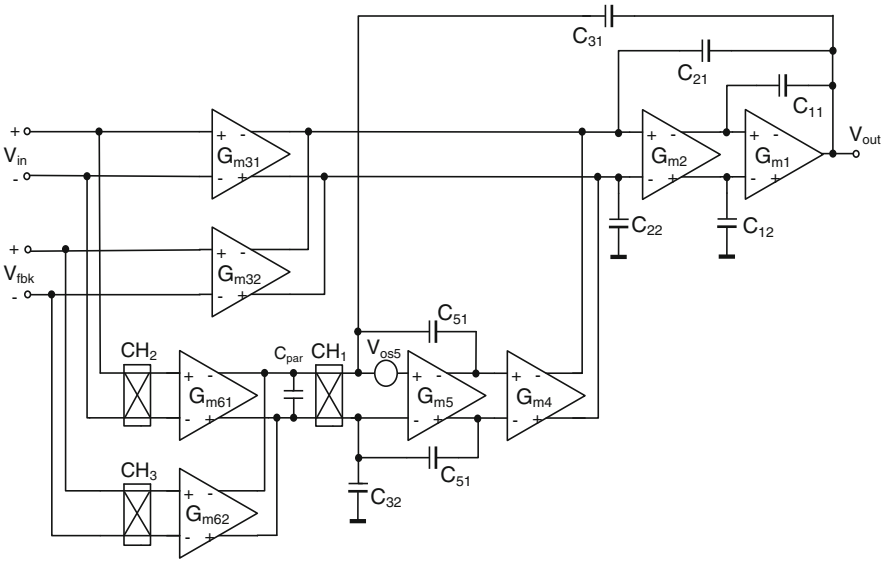

Fig. 3.5 Chopper-stabilized CFIA in a multi-path architecture [11]

3.2.1 Chopper-Stabilized Current-Feedback Instrumentation Amplifier

The chopper-stabilized operational amplifier (Fig. 2.25) can be transformed into a chopper-stabilized CFIA [11], as shown in Fig. 3.5. The resulting CFIA has a low-frequency path (LFP) and a high frequency path (HFP). The low-frequency characteristics, such as noise, offset and gain accuracy, are determined by the low-frequency path, while the high-frequency path dominates the noise after the turn over frequency.

To reduce the offset of the low-frequency path, the input and feedback trans-conductors G_{m61} and G_{m62} are chopped, thus giving rise to a chopper ripple. Although this ripple is partially filtered by the integrator built around G_{m5}, C_{51} and C_{52}, there is still a residual chopper ripple at the integrator output. To eliminate this, G_{m61} and G_{m62} are auto-zeroed to reduce their initial offset, as shown in Fig. 3.6. The auto-zeroing capacitor C_{A1}-C_{A4} isolates the input and feedback CM voltage from the CM of the G_{m61} and G_{m62}. However, the disadvantage is that the input choppers CH_2 and CH_3 together with the auto-zeroing capacitors C_{A1}-C_{A4} constitute a switched-capacitor circuit with an impedance of $1/F_1C_A$, where F_1 is the auto-zeroing frequency, and C_A is the value of C_{A1}-C_{A4}. Thus, the input impedance decreases compared to the case when G_{m61} and G_{m62} are not auto-zeroed.

The offset of G_{m5} also causes a residual input offset [11]. This offset, being chopped by CH_1 (Fig. 3.6), charges and discharges the parasitic capacitors at the

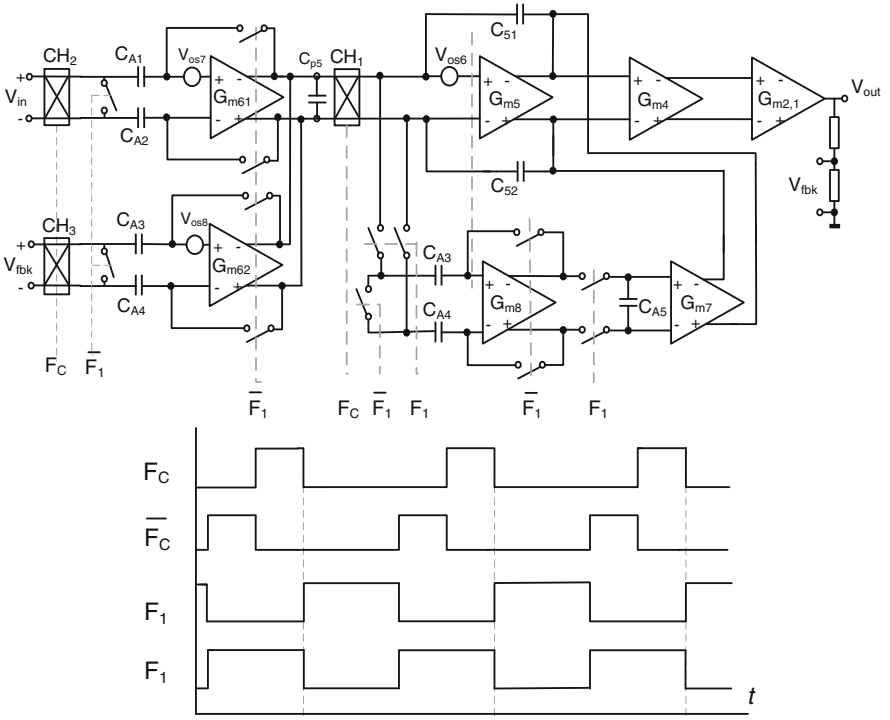

Fig. 3.6 The low-frequency path of a chopper offset-stabilized CFIA and associated timing diagram [11]

output of G_{m61} and G_{m62}, thus appearing as a square-wave voltage there. After being chopped again by CH_2 and CH_3, this square wave translates into an extra input-referred error. To mitigate this problem, G_{m5} is auto-zero offset-stabilized, as shown in Fig. 3.6. Finally, a 2.5 μV offset is achieved. G_{m61} (or G_{m62}) has a transconductance of 220 μA/V, which corresponds to a noise PSD of 20 nV/$\sqrt{\text{Hz}}$. Since the noise of G_{m61} and G_{m62} are uncorrelated, the noise PSD increases by a factor of $\sqrt{2}$. Furthermore, because they are auto-zeroed half of the time, the noise PSD increases by another $\sqrt{2}$ [11]. As a result, the measured noise PSD is 42 nV/$\sqrt{\text{Hz}}$ consuming a 325 μA supply current (NEF = 29.2).

3.2.2 *Ping-Pong Auto-Zeroed Current-Feedback Instrumentation Amplifier*

The auto-zeroed ping-pong operational amplifier (Fig. 2.19) can also be used to build a CFIA [5], as illustrated in Fig. 3.7. The input and feedback transconductors in the ping stage and pong stage are auto-zeroed to reduce the initial offset of the

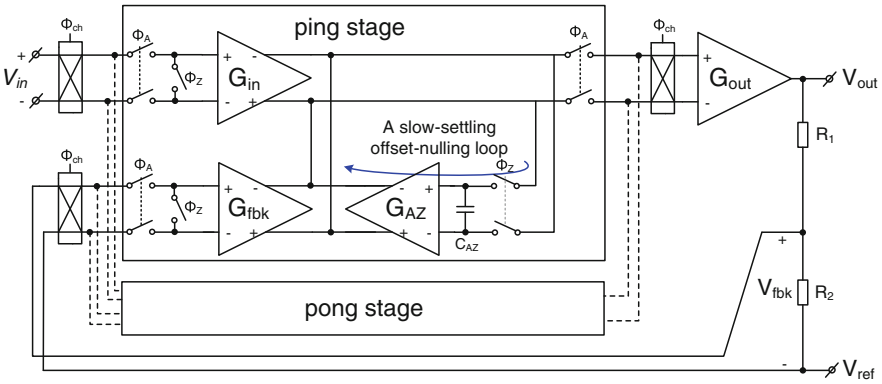

Fig. 3.7 CFIA employing ping-pong auto-zeroing and chopping [5]

amplifier. To mitigate the noise folding inherent to auto-zeroing, a slow-settling offset-nulling loop is applied to limit the noise bandwidth to less than half of the auto-zeroing frequency [5]. The noise is then modulated away from DC by chopping the input stages at half the auto-zeroing frequency, reducing the low-frequency noise to the white noise level. However, due to its ping-pong topology, this amplifier needs four low-noise G_m stages, so its power consumption is rather high. It consumes a supply current of 1.7 mA with a noise PSD of $27\text{nV}/\sqrt{\text{Hz}}$ (NEF = 43).

3.2.3 Conclusions

As shown in Fig. 3.6, the use of auto-zeroing in the input stages of the low frequency path of the multi-path CFIA increases the noise PSD by a factor of $\sqrt{2}$ compared to the case without auto-zeroing [11]. This implies that to achieve the same noise level, it needs to consume twice as much power. In [5], besides the factor $\sqrt{2}$ increase in the noise PSD, four low-noise transconductance stages are used in a ping-pong auto-zeroed topology, which is much less power-efficient than the chopped CFIA. Table 3.1 summarizes the performance of these two CFIAs.

Chapter 4 will present a CFIA that employs only chopping to eliminate the $1/f$ noise and offset [3]. To suppress the associated chopper ripple, a continuous-time technique is proposed that enables a significant improvement in power efficiency.

Table 3.1 Comparison of prior art CFIAs

	Witte [11]	Pertijs [5]
Year	2009	2010
Supply voltage	5 V	5 V
Supply current	325 μA	1.7 mA
Input noise PSD	42nV/$\sqrt{}$Hz	27nV/$\sqrt{}$Hz
CMRR	130 dB	142 dB
PSRR	114 dB	138 dB
Gain error	0.05 % (Untrimmed)	0.1 % (Untrimmed)
Offset	<2.5 μV	<2 μV
GBW	640 kHz	800 kHz
GBW/I_{supply} (kHz/μA)	2	0.5
NEF [3.9]	29.2	43

3.3 Gain Accuracy Improvement Techniques

The previous section mainly discussed how to eliminate the offset and 1/*f* noise in CFIAs. Besides that, however, gain error is another dominant error source at low frequencies. Figure 3.8 shows the output error versus input signal amplitude. For small input signals, offset dominates; while for large input signals, gain error dominates.

In a CFIA, the gain error is mainly due to the mismatch between the input and feedback transconductors (Fig. 3.9). This can be as much as 2 % over temperature and process. For instance, in a CFIA with a closed-loop gain of 100, a gain error of 2 %, an offset of 2 μV and a 5 V supply, the minimum input signal X that ensures the gain error is larger than the output referred offset, is given by

$$X \cdot 100 \cdot 2\,\% \geq 2\mu V \cdot 100. \tag{3.4}$$

Thus, $X \geq 100$ μV, meaning that when the input signal is larger than 100μV, the effect of gain error becomes larger than that of offset. With a 50 mV full scale input, the output-referred gain error is 100 mV, which is much larger than the output-referred offset of 200 μV. Apart from limited gain accuracy, the linear range of the CFIA is also limited to less than 100 mV due to the input and feedback transconductors (using simple differential pairs).

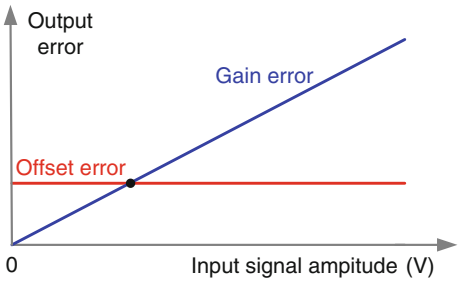

Fig. 3.8 Output gain error and offset vs. input signal amplitude

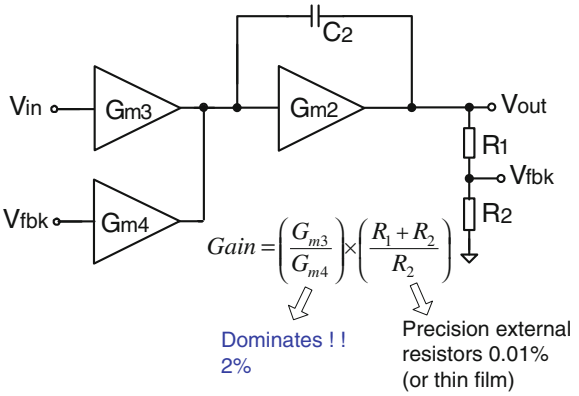

Fig. 3.9 Gain error sources in the CFIA

3.3.1 Current-Feedback Instrumentation Amplifier with Resistor-Degenerated Input Stages

To reduce transconductor mismatch and increase linear input range, one common approach is the use of resistor-degenerated differential pairs [5, 12]. The detailed schematic of a NMOS input resistor-degenerated stage is shown in Fig. 3.10. Its input CM range includes the positive supply rail. Figure 3.11 shows a PMOS input resistor-degenerated stage which has ground-sensing capability.

Taking Fig. 3.10 for example, local negative feedback loops maintain the NMOS input transistors M_1 and M_4 at a CM independent drain-source voltages [13]. Within the loops, M_3 and M_6 keep the drain currents of the input transistors (M_1 and M_4) constant. Folded cascode transistors M_2 and M_5 ensure that the input voltage includes the supply rail. The input transistors M_1 and M_4 level-shift the input common-mode voltage down by a gate-source voltage, and reproduce the differential input voltages across resistors R_1 and R_2. Thus, the signal current flowing through R_1 and R_2 is given by:

$$I_{dgn} = \frac{V_{in+} - V_{in-}}{R_1 + R_2} \tag{3.5}$$

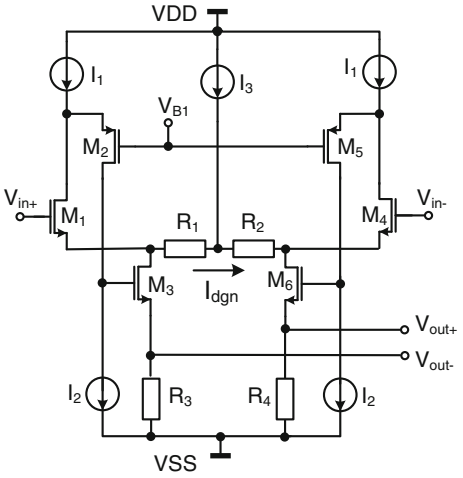

Fig. 3.10 Schematic of composite NMOS resistive-degenerated differential pair

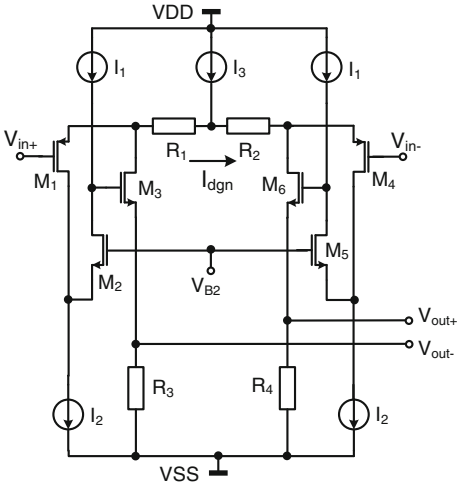

Fig. 3.11 Schematic of composite PMOS resistive-degenerated differential pair

Transistors M_3 and M_6 feed this current to the output load resistors R_3 and R_4. From (3.5), it can be seen that the transconductance of this stage is mainly determined by the degeneration resistors R_1 and R_2.

With careful layout, or by trimming, the degeneration resistors can be made to match better than the transistors. Gain errors of 0.1 % have been achieved by both auto-zeroed ping-pong CFIA (NEF = 43) [5] and chopper-stabilized CFIA (NEF = 153) [12]. As can be seen from the NEFs of these designs, the use of resistor degeneration leads to a significant loss in power efficiency. This is because of the extra current required to bias transistors M_3 and M_6 and the cascode transistors M_2 and M_5. All these transistors contribute to noise, and the transconductance of this stage decreases due to degeneration.

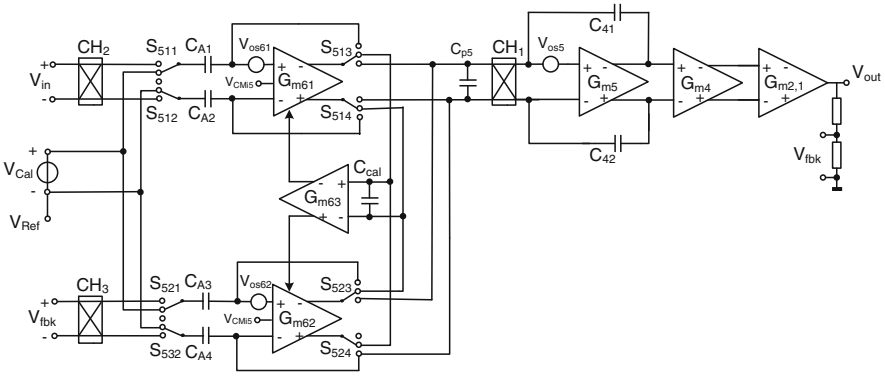

Fig. 3.12 Chopper-stabilized IA with auto-zero sense amplifiers and auto-gain calibration

3.3.2 *Chopper-Stabilized Current-Feedback Instrumentation Amplifier with Auto-Gain Calibration*

The different input and feedback CM voltages of a CFIA can be isolated by capacitors [11], as shown in Fig. 3.6. The auto-zeroing capacitors $C_{A1}-C_{A4}$ block the DC CM voltage. The CM voltage at the inputs of G_{m61} and G_{m62} is, therefore, set by the auto-zeroing action and so is the same as their output CM voltage, which, in turn, is regulated by a CM feedback loop [11]. The voltage non-linearity of C_{A1} to C_{A4} gives rise to a gain error that is a function of the CM voltage [11]. However, this error is less than 0.05 % over a CM range from 0 to 3.6 V.

To further improve gain accuracy, the gain of the low-frequency path of a chopper-stabilized CFIA (Fig. 3.6) also can be calibrated to equalize the transconductance of G_{m61} and G_{m62}, as proposed in [14]. This is shown in Fig. 3.12, for simplicity, the auto-zero stabilization loop that could be used to eliminate the offset V_{os5} is omitted here.

There are three operation modes for G_{m61} and G_{m62}: offset auto-zeroing, auto-gain calibration and normal operation. Figure 3.12 shows the amplifier in the auto-gain calibration mode. In this mode, both inputs of G_{m61} and G_{m62} are connected to a calibration voltage V_{Cal} and the output currents of these stages are compared. The difference of the output currents is then integrated by C_{Cal} to a DC voltage. This voltage feeds to G_{m63}, which converts it into two differential currents that fine-tune the tail currents of G_{m61} and G_{m62} to compensate their mismatch. Thus the suppression ratio for the mismatch is determined by the gain within the calibration loop.

Note that the stabilization loop accurately controls the gain at low frequencies. The gain at high frequencies is determined by the difference of the main input stages G_{m31} and G_{m32} in Fig. 3.5, which is not auto-calibrated. However, this is not

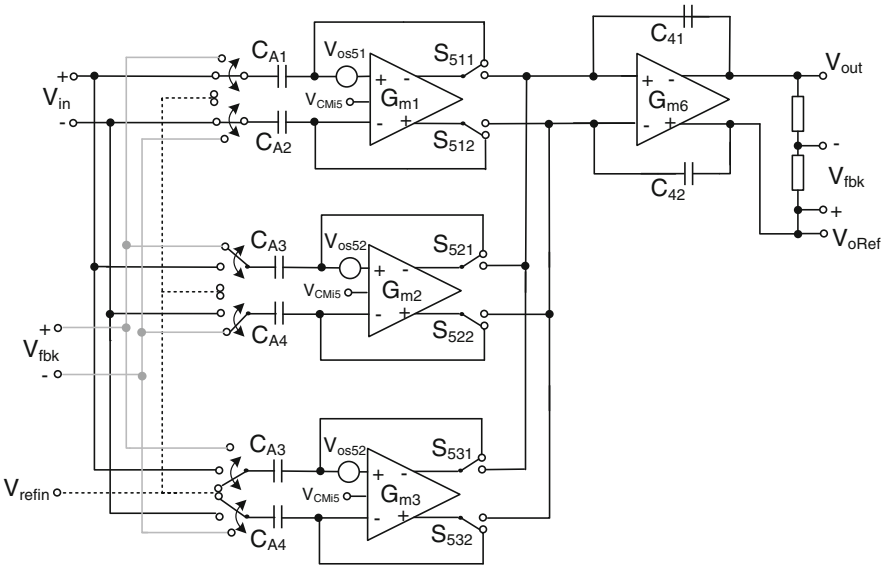

Fig. 3.13 Ping-pong-pang auto-zeroed CFIA [16]

a problem because at high frequencies the gain is not accurate anyway because of the drop in overall loop gain.

Since this approach needs an auto-gain correction phase, its continuous-time operation is interrupted. This implies that it can not compensate for temperature dependent gain drift.

3.3.3 Ping-Pong-Pang Current-Feedback Instrumentation Amplifier

Another method to improve the gain accuracy of the CFIA is to use dynamic element matching (DEM). An example of this is the ping-pong-pang (PPP) auto-zeroed CFIA [15, 16], whose simplified schematic is shown in Fig. 3.13.

The three transconductances G_{m1}, G_{m2} and G_{m3} are dynamically switched between the input, feedback, and auto-zeroed stages with the algorithm shown in Table 3.2 [16]. The average effect of DEM modulates the G_m mismatch to the DEM frequency, thus ensuring good accuracy at low frequencies.

This concept was first implemented in [17], around the same time as the work presented in Chap. 5. As shown in Fig. 3.14, the three transconductors are alternately switched between input, feedback and auto-zeroing states. While one transconductor is auto-zeroed, the other two provide the output signal (Fig. 3.14). Since each transconductor spends equal time in the input and feedback states, their mismatch is dynamically averaged out.

Table 3.2 Ping-pong-pang algorithm with DEM

	1	2	3	4	5	6	1
V_{in}	G_{m2}	G_{m4}	G_{m4}	G_{m3}	G_{m3}	G_{m2}	G_{m2}
V_{fbk}	G_{m3}	G_{m3}	G_{m2}	G_{m2}	G_{m4}	G_{m4}	G_{m3}
V_{Cal}	G_{m4}	G_{m2}	G_{m3}	G_{m4}	G_{m2}	G_{m3}	G_{m4}

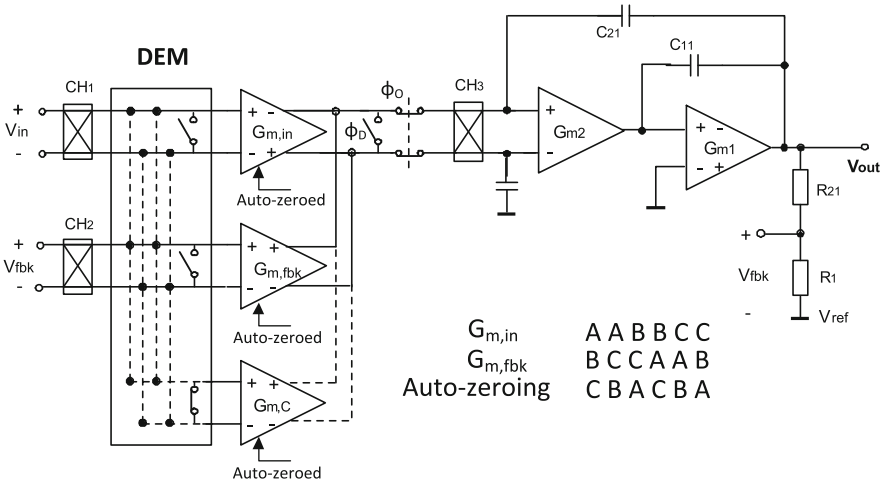

Fig. 3.14 Block diagram of the ping-pong-pang CFIA with the timing diagram [17]

To analysis the effect of DEM on gain error, a simplified block diagram of a CFIA that applys DEM to its input and feedback transconductors to average out their G_m mismatch is shown in Fig. 3.15. The G_m ratios corresponding to the two DEM phases are given by

$$G_m ratio_1 = \frac{G_{m3}}{G_{m4}} = \frac{1}{1+\Delta} \tag{3.6}$$

$$G_m ratio_2 = \frac{G_{m4}}{G_{m3}} = \frac{1+\Delta}{1} \tag{3.7}$$

where Δ is the initial mismatch between G_{m3} and G_{m4}. The G_m ratios will then toggle between two levels: $(1 + \Delta)/1$ and $1/(1 + \Delta)$, causing the CFIA output to toggle between $(1 + \Delta)V_{ideal,\ out}$ and $V_{ideal,out}/(1 + \Delta)$. The average gain error after applying DEM is given by [18]

$$G_m ratio_{avg} = \frac{\frac{1+\Delta}{1} + \frac{1}{1+\Delta}}{2} \approx 1 + \frac{\Delta^2}{2} \quad (for \Delta << 1) \tag{3.8}$$

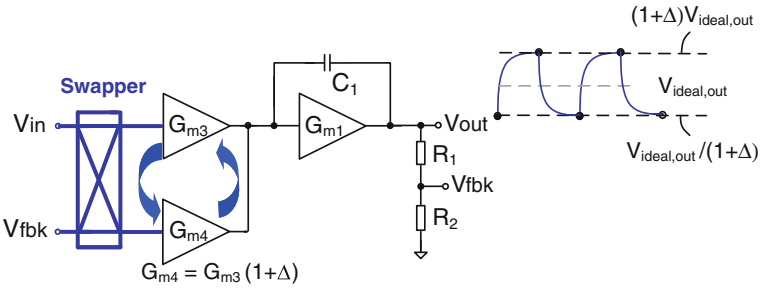

Fig. 3.15 CFIA with DEM ripple after applying DEM

Equation (3.8) shows that the use of DEM reduces the initial gain error from Δ to $\Delta^2/2$. So for a typical G_m mismatch of 2 %, the use of DEM will reduces this to, a negligible 0.02 %. In a practical CFIA, however, the common-mode (CM) dependence of G_{m3} and G_{m4} may still limit gain accuracy. If the input and output common-mode voltages are not the same, in a typical situation in IA applications, The actual transconductance of, say, the one that connects to the input CM will vary by an extra amount mismatch Δ_{cm} and this mismatch will always appears in the input path during the two DEM swap phases. The average gain error, after applying DEM, is then given by [18]:

$$|Gain\ Error| = |1 - \frac{\frac{1+\Delta+\Delta_{cm}}{1} + \frac{1+\Delta_{cm}}{1+\Delta}}{2}| \approx \frac{\Delta^2}{2} + \frac{\Delta \cdot \Delta_{cm}}{2} + \Delta_{cm} \quad (for \Delta << 1) \tag{3.9}$$

From (3.9), the CM-dependent mismatch Δ_{cm} will not be suppressed by the DEM. For simplicity, this issue will be neglected in the following analysis. However, a circuit-level technique to mitigate this problem will be described in Sects. 5.6 and 6.6.1.

The accurate gain achieved in the low frequency, however, is at the cost of a DEM ripple at the amplifier output due to the modulated G_m mismatch. It is assumed that the closed-loop gain of the CFIA is $1/\beta$, where β is the feedback factor determined by the gain-setting resistors, i.e. $\beta = R_2/(R_1 + R_2)$. The CFIA output amplitude during the two DEM phases is given by

$$V_{out1} = V_{in} \times \frac{1}{\beta} \times \frac{1+\Delta}{1} \tag{3.10}$$

$$V_{out2} = V_{in} \times \frac{1}{\beta} \times \frac{1}{1+\Delta}. \tag{3.11}$$

Therefore, the amplitude of the DEM ripple is given by [3.18]

$$V_{DEM,ripple} = V_{out1} - V_{out2} = 2\Delta \cdot V_{in} \cdot \frac{1}{\beta} = 2\Delta \cdot V_{ideal,out}. \tag{3.12}$$

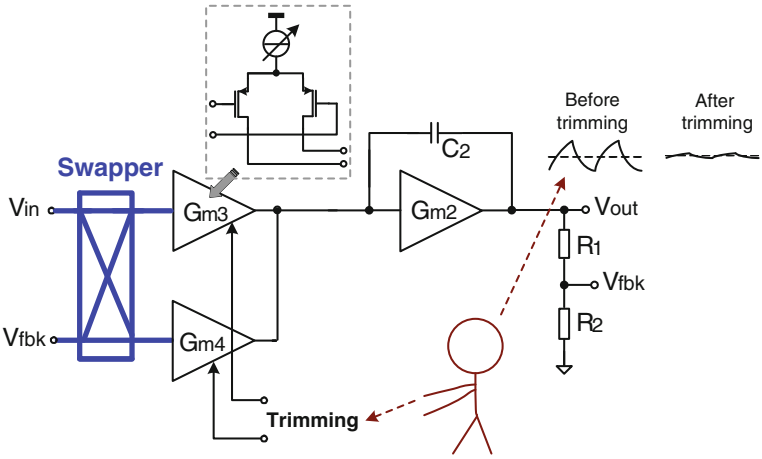

Fig. 3.16 Trimming in a CFIA employing DEM

where $V_{ideal,out}$ is the ideal output voltage of the CFIA. Equation (3.12) indicates that the DEM ripple is a product of the mismatch Δ and the output signal. With a mismatch of 0.5 % and a 4.5 V output signal, the amplitude of the DEM ripple can be as large as 45 mV, and therefore must be suppressed.

To reduce this signal-dependent ripple, the transconductors are trimmed by a 5-bit current DAC [17]. As depicted in Fig. 3.16, the trimming mechanism involves monitoring of the output DEM ripple, and then trimming a current-DAC that fine-tunes the tail current of G_{m3} and G_{m4} to compensate for their mismatch. When the output DEM ripple is reduced to zero, trimming is accomplished. The disadvantage of trimming is the increased production costs. More importantly, trimming is a one-time calibration, thus it will not compensate for temperature drift.

Compared to the previous ping-pong CFIA [5] (Fig. 3.7), this amplifier uses three transconductors rather than four. Furthermore, its transconductors are not degenerated. Thus, this amplifier achieves a 2 × improved power efficiency (NEF = 24). Overall, this CFIA achieves a gain error of 0.04 % and a noise PSD of 28nV/$\sqrt{}$Hz, while drawing a 480 μA supply current.

3.3.4 Conclusions

Gain accuracy is the major disadvantage of the CFIA, and is caused by the mismatch between its input and feedback transconductances. Furthermore, its nonlinearity and limited range is limited due to the input and feedback transconductors. To improve these, three approaches can be taken. The first method involves the use of resistor-degenerated input stages [5, 12] to shift

transconductance matching to resistive matching. As a result, a gain error of 0.1 % and improved linearity has been achieved. However, resistor-degeneration leads to a noise or power penalty. The second approach uses discrete-time auto-gain calibration in an auto-zeroed amplifier. However, it is not a continuous-time technique, unless it is applied in a ping-pong topology. The third method is to apply DEM to the three stages in a ping-pong-pang CFIA. As presented in [17], such CFIA can achieve a gain error of 0.04 %. To eliminate the signal-dependent DEM ripple, trimming can be applied [17]. However, it increases the production cost and cannot compensate for the temperature drift.

Chapter 5 will present a chopper CFIA that employs DEM to eliminate the gain error. To suppress the associated DEM ripple, a continuous-time technique is proposed, thus eliminating the need of trimming. These techniques result in a significant improvement in power efficiency.

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Chapter 4
A Chopper Instrumentation Amplifier with Offset Reduction Loop

This chapter discusses the design and implementation of a chopper current-feedback instrumentation amplifier (CFIA). This amplifier can be used in stand-alone sensor read-out systems that need to drive an external analog-to-digital converter (ADC).

Firstly, the requirements on the amplifier are described. It is targeted for thermistor read-out applications in wafer steppers (see Chap. 1). The design of the CFIA is then discussed. Both the input and intermediate stages of the CFIA are chopped to achieve a low 1/*f* noise corner. To reduce chopper ripple, a continuous-time (CT) offset reduction loop (ORL) is proposed. Due to its CT nature, it does not cause noise folding, thus offering improved power efficiency over auto-zeroed amplifiers. It will be shown that this ORL can be applied to both general-purpose instrumentation amplifiers and operational amplifiers.

Measurement results show that the CFIA achieves a 1 mHz 1/*f* noise corner at a noise PSD of 15 nV/$\sqrt{\text{Hz}}$ while consuming only 230 μA supply current (NEF = 8.8). To our knowledge, this represents the best LF noise performance ever reported for a stand-alone CMOS instrumentation amplifier.

4.1 Amplifier Requirements

In Chap. 1, a challenging interface application was described: the read-out of a precision thermistor bridge used in wafer steppers. The output of the thermistor bridge is only ±24 mV, thus it needs to be amplified before it is digitized or processed further. This requires the use of a low-noise instrumentation amplifier (IA). The challenges associated with the design of such an amplifier are summarized below.

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Table 4.1 Key requirements of the precision instrumentation amplifier for thermistor bridge readout

Specifications	Value
Supply voltage	5 V
Gain tolerance	0.5 %
Input referred noise PSD	15 nV/$\sqrt{}$Hz
1/*f* corner frequency	1 mHz
Offset	5 μV
Offset drift	20 nV/°C
CMRR	>120 dB
PSRR	>120 dB
Input common-mode	0–3 V
Output common-mode	2.5 V
Input impedance	>20 MΩ
Supply current	<300 μA

The first challenge is to achieve low thermal and 1/*f* noise. The thermistor bridge used in the wafer stepper application has a noise PSD of 1m nV/$\sqrt{}$Hz, and so the amplifier's noise PSD was chosen to be at roughly the same level, i.e. 16 nV/$\sqrt{}$Hz. As mentioned in Chap. 1, to achieve high power efficiency, the amplifier's noise should be white in the bandwidth of interest, which means that the amplifier should have a 1/*f* noise corner of a few mHz. To justify such low noise specifications, the amplifier must also have high CMRR (>120 dB) and PSRR (>120 dB).

Secondly, in addition to low thermal and 1/*f* noise, the read-out electronics must achieve low offset and good gain accuracy to maintain system accuracy over temperature. The offset and offset drift aim to achieve less than 5 μV and 20 nV/°C. Since the gain error of the thermistor bridge is about 0.5 %, the amplifier's gain accuracy does not need to be much better. Good gain drift can be achieved by using careful layout to match the input and feedback transconductors of the CFIA. This is our first approach.

The third challenge is the need for the amplifier to accommodate different input and output common-mode (CM) voltages. The input CM is at 0.61 V since the bridge is biased at 1.22 V. The output CM is at 2.5 V, since the amplifier's output is to be digitized by an Analog-to-Digital converter (ADC) with a 0–5 V input range.

The fourth challenge is to minimize the amplifier's power consumption to reduce self-heating. This should not be larger than that of the bridge (a few hundreds of μA) to restrict local self-heating errors.

Finally, the amplifier should have a high input impedance (>20 MΩ), so as not to attenuate the sensor signal, and it should be able to drive a 50 pF load capacitor, just like most general-purpose amplifiers. The target specifications of the amplifier are summarized in Table 4.1.

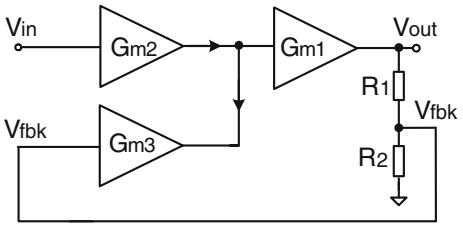

Fig. 4.1 Simplified block diagram of CFIA

4.2 Amplifier Architecture

As discussed in Chap. 1, a CFIA has significant advantages over the classic three-opamp IA because of its better power efficiency, high CMRR and rail sensing capability. Moreover, it can easily handle different input and output CM voltages. Compared with a switched-capacitor IA, a CFIA provides continuous-time signal. Compared to a capacitively-coupled IA, a CFIA has higher input impedance and does not produce glitches. These properties make a CFIA more suitable for use as a stand-alone IA for bridge readout.

Figure 4.1 shows the block diagram of a CFIA. The input transconductor G_{m2} and feedback transconductor G_{m3} convert the input and feedback voltages into the corresponding currents. Their difference is then nulled by the gain of G_{m1}. If the loop gain is high enough, the overall feedback ensures that the output currents of G_{m2} and G_{m3} cancel out each other and thus the closed-loop gain of the amplifier is given by:

$$Gain = \left(\frac{G_{m2}}{G_{m3}}\right) \times \left(\frac{R_1 + R_2}{R_2}\right) \tag{4.1}$$

Gain Accuracy

From (4.1), it can be seen that the amplifier's gain accuracy will depend on the open-loop gain of the CFIA and on the matching between the input and feedback transconductance stages G_{m2} and G_{m3}.

As mentioned in Chap. 1, the output range of the thermistor bridge is 48.6 mV. To optimally map this range to the 0–5 V range of the ADC, the amplifier should have a rail-to-rail output with a gain of 183. For an accuracy of 0.5 % at the intended closed-loop gain of 183, the open-loop gain of G_{m1} must be in excess of 90 dB, which is easily achievable with two stages of amplification. By restricting the input and output CM voltages to the 0–3 V range, the transconductors can be realized by PMOS differential pairs. With careful layout on the transconductors, it should be possible to realize a CFIA that achieves better than 0.5 % gain accuracy.

Chopping Strategy

Since chopping is a continuous-time modulation technique that does not cause noise folding, it is employed here to reduce the offset and $1/f$ noise of the amplifier. Simulations show that the unchopped $1/f$ noise corner of the CFIA in the

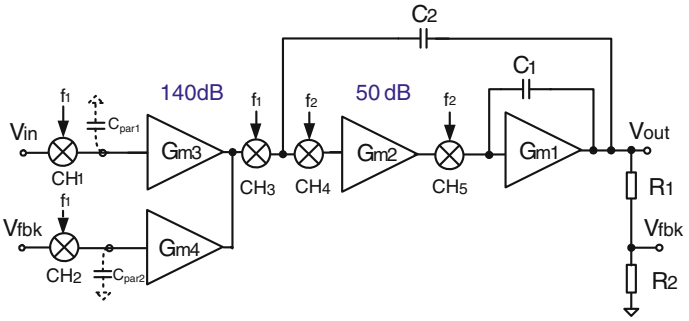

Fig. 4.2 Three-stage CFIA with the input and intermediate stages chopped

implemented 0.7 μm CMOS technology is 10 kHz. To completely remove 1/*f* noise, the chopping frequency should be well above the 10 kHz 1/*f* noise corner. However, it should not be too high due to charge injection and clock feed-through considerations. A chopping frequency of 30 kHz is chosen in this work. The goal of this design is to achieve a 1 mHz 1/*f* noise corner.

To drive a 50 pF load, the output stage of the CFIA is implemented in class-AB fashion. The large signals present in the class-AB stage means that it can not be easily chopped. Its 1/*f* noise must therefore be suppressed by the effective gain of the preceding stages at the chopping frequency. After setting the unity-gain bandwidth (UGB) of the amplifier to be 800 kHz, the effective gain at the chopping frequency can be translated to a DC gain requirement of the preceding stages.

Simulations show that the CFIA requires two chopped gain stages to provide sufficient gain to shift the class-AB stage's 1/*f* noise corner below 1 mHz. Thus, a three-stage topology was chosen, in which the input and intermediate stages are chopped to suppress their 1/*f* noise. To provide sufficient loop gain and to suppress the noise from the intermediate stage, the input stages are designed to have a DC gain of 140 dB. The intermediate stage is designed to have a DC gain of 50 dB.

To confirm the validity of this approach, simulations were done using the periodic steady-state (PSS) and periodic noise analysis (PNOISE) tools of Spectre RF [1]. Figure 4.2 shows the overall topology of the three-stage CFIA. The amplifier's simulated input-referred noise spectrum without chopping, with the input stage chopped and with the input and intermediate stages chopped, is shown in Fig. 4.3. Without chopping, the 1/*f* noise below 10 kHz is clearly visible. With only the input stage chopped, a 1/*f* noise corner of 0.3 Hz was observed, which is still too high for the targeted 1/*f* noise corner of 1 mHz. When both the input and intermediate stages are chopped, the resulting noise spectrum has a 1/*f* noise corner of 1 mHz.

Frequency Compensation

Nested Miller frequency-compensation [2] is used to maintain the stability of the three-stage amplifier. It is designed to be stable for a closed-loop gain of >20 with a 50 pF capacitive load, since unity-gain stability is not required in this application. The simulated open-loop frequency response of this amplifier is

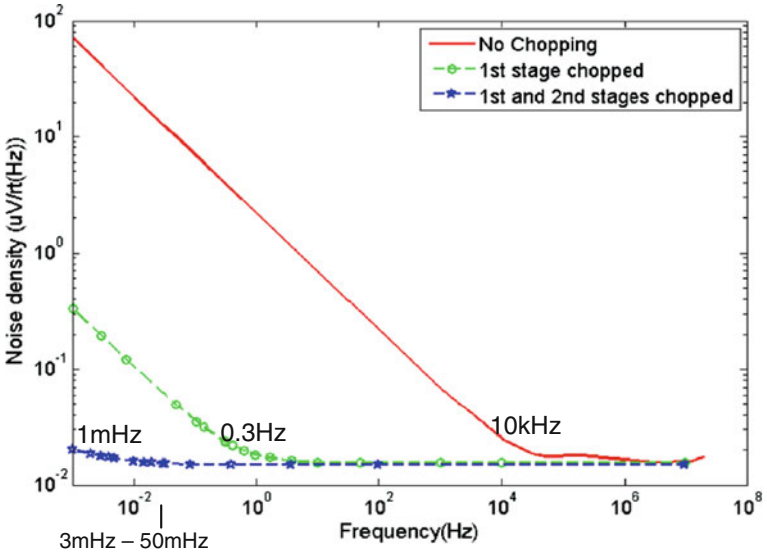

Fig. 4.3 Simulated input noise PSD

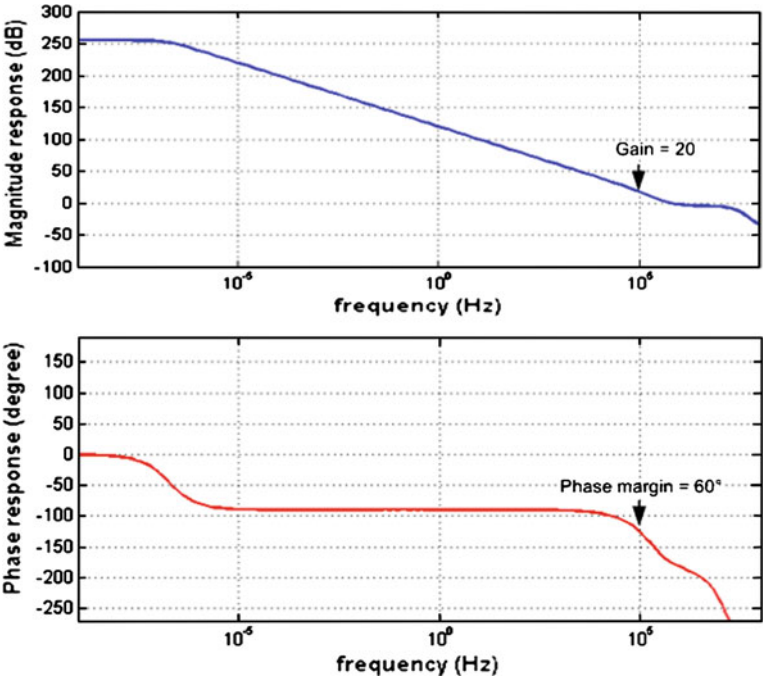

Fig. 4.4 Simulated open-loop frequency response

shown in Fig. 4.4. It has an open-loop gain above 250 dB, which means that gain errors due to finite DC loop gain are negligible.

Input Impedance

Configured at a gain of 100, the gain setting resistors R_1 and R_2 of the CFIA are about 300 Ω and 30 kΩ, respectively (Fig. 4.2). Due to the action of input choppers CH_1 and CH_2, the parasitic capacitors C_{par1} and C_{par2} at the input of G_{m3} and G_{m4} appear as switched-capacitor impedance at the input and feedback nodes of the CFIA. Assuming $C_{par1} = C_{par2} = 0.6$ pF and chopping frequency $f_1 = 30$ kHz, the input impedance is given by $1/(2f_1 \cdot C_{par1}) = 28$ MΩ, which is much larger than the equivalent resistance of the feedback network (300 Ω). Since the thermistor bridge has a resistance of 10 kΩ, the input impedance of the CFIA causes a gain error of 0.036 %, which is negligible compared to the gain error of the bridge itself (0.5 %).

4.3 Offset Reduction Loop

As discussed above, the input and intermediate stages of the CFIA are both chopped to suppress their 1/*f* noise corner below 1 mHz. However, the amplitude of the resulting chopper ripple can be quite large (∼800 mV), limiting the headroom. Thus, this ripple must be suppressed.

Several ripple reduction techniques were reviewed in Chap. 2. The discrete-time sampling techniques [3, 4] involve noise folding, thus incurring a certain noise penalty. Furthermore, the discrete-time [4] and continuous-time [5] notch filters all generate excess phase shift in the signal path. In the auto-correction feedback (ACFB) loop [6], the notch filter generates excess phase shift within the feedback loop. To maintain stability, the ripple reduction techniques [4–6] need a high chopping frequency to ease the frequency compensation, thus increasing the charge injection and the offset. Moreover, the ACFB loop [6] suffers from limited DC loop gain since the ripple sensing point is at the virtual ground of an amplifier. In this work, an AC-coupled offset reduction loop (ORL) [7] is proposed that avoids the foregoing issues.

4.3.1 Basic Concept

Figure 4.5 shows the conceptual diagram of the CFIA with the ORL. The ORL synchronously demodulates the chopper ripple from AC to DC, averages it to obtain a DC measure of the offset and then uses it to null the offset, hence the ripple.

The ORL consists of sense capacitor C_4, chopper CH_6, integrator G_{m6} with C_{int} and compensation transconductance G_{m5}. In the start-up condition, the sense

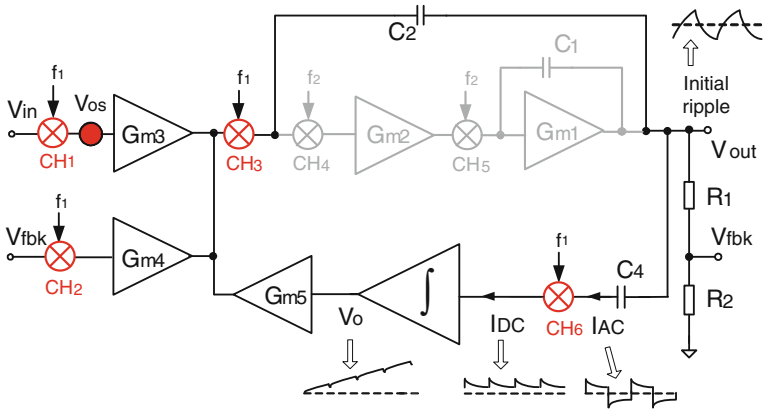

Fig. 4.5 Simplified block diagram of a three-stage CFIA with an AC-coupled ripple reduction loop (ORL) in start-up condition

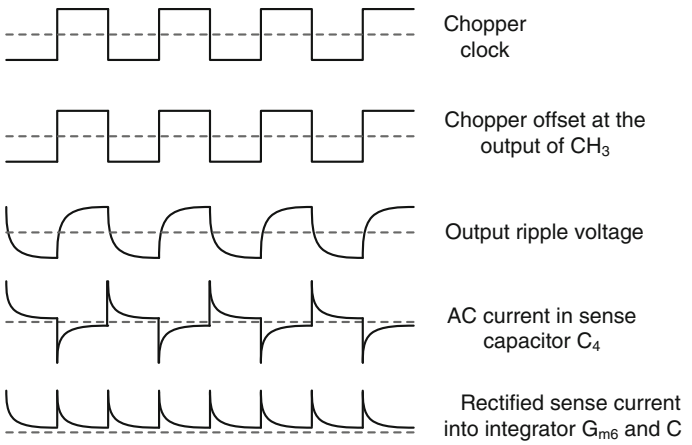

Fig. 4.6 Waveforms of chopper clock, chopped offset, output ripple voltage, AC current and rectified sense current in the ORL

capacitor C_4 converts the amplifier output ripple $V_{out,ripple}$ into an AC current I_{AC}. The current amplitude is proportional to the derivative of $V_{out,ripple}$, given by

$$I_{AC} = C\frac{dV_{out,ripple}}{dt} \tag{4.2}$$

This AC current is demodulated by chopper CH_6, and the resulting DC current I_{DC} is integrated by an integrator, generating a DC compensation voltage V_o that is proportional to the ripple amplitude. This is then fed back via transconductance G_{m5} to the outputs of G_{m3} and G_{m4}, injecting a current that compensates for the offset between G_{m3} and G_{m4}. Figure 4.6 shows the waveform of the chopper clock,

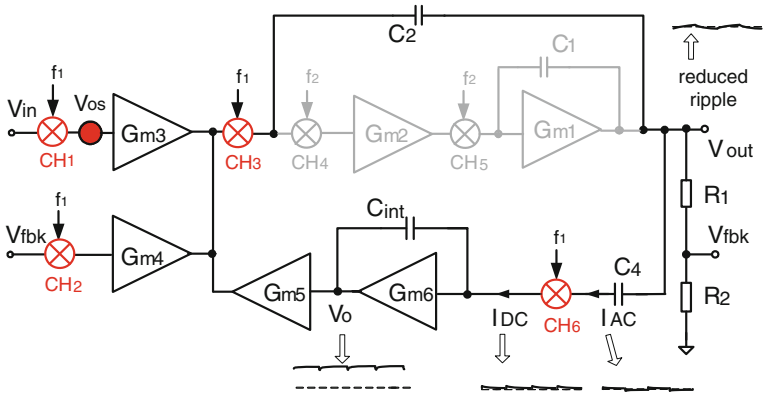

Fig. 4.7 Simplified block diagram of a three-stage CFIA with ORL in steady-state condition

the chopper offset at the output of CH_3, the output ripple, the sense current I_{AC} through C_4 and the rectified current I_{DC}.

At steady state, as shown in Fig. 4.7, the input offset V_{OS} is precisely cancelled by the ORL and the chopper ripple is strongly reduced. Since offset and the compensation current are both DC signals, the offset reduction ratio is determined by the DC loop gain in the ORL. The integrator in the ORL (Fig. 4.5) is built with G_{m6} and C_{int}, as shown in Fig. 4.7.

The synchronous demodulator formed by the chopper CH_6 and the integrator behaves like a narrow-band notch filter around the chopping frequency and its harmonics. As a result, the ORL has little effect at frequencies near DC, and therefore also little effect on the low-frequency response of the amplifier.

When input signal frequencies are close to the chopping frequency, however, the output signal is AC-coupled via C_4 into the synchronous demodulator, and then demodulated to DC and fed back to the outputs of G_{m3} and G_{m4}. This creates notches in the amplifier closed-loop gain at harmonics of the chopping frequency f_1, $3f_1$, and $5f_1$…. The notch at f_1 is visible in the closed-loop transfer function of the amplifier [7], while the notches at the higher harmonics of f_1 are suppressed by the low-pass transfer function of the amplifier. Figure 4.8 shows the transfer function of the amplifier with a notch at f_1 due to synchronous demodulation in the ORL. This notch will affect the amplifier's step response as some ringing will occur before the amplifier output settles. However, this is not a problem for bridge sensor applications, because such sensors typically output *millivolt*-signals at frequencies of a few Hz. For wide-band application, this notch can be buried in a multi-path amplifier topology to ensure a smooth single-pole response, as will be discussed in Sect. 4.5. The depth of the notch (Fig. 4.8) is determined by the amount of signal that is fed back through the offset reduction loop, while the width of the notch is determined by the unity-gain bandwidth of the ORL.

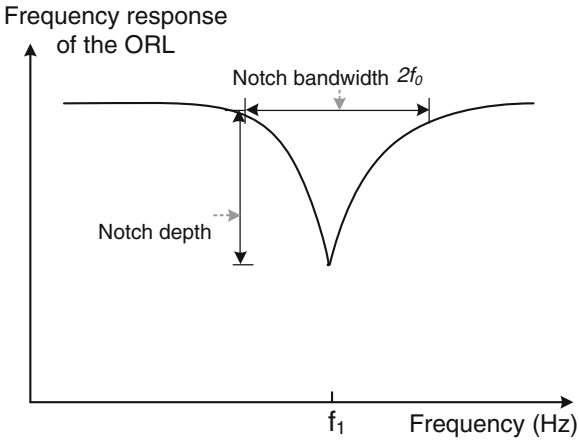

Fig. 4.8 Frequency response of ORL

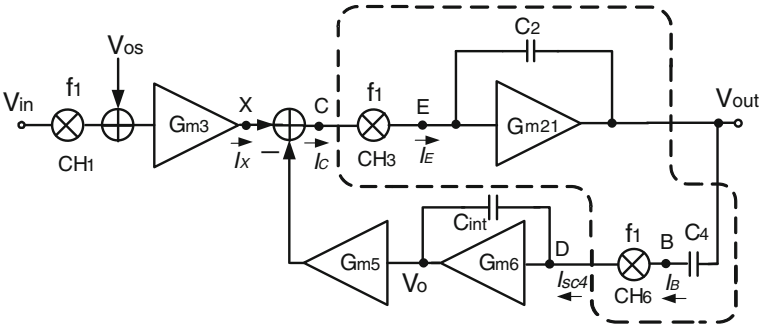

Fig. 4.9 Simplified block diagram of a CFIA with an AC-coupled ORL

4.3.2 Transfer Function Analysis

The loop transfer function of the ORL can be derived with the help of the block diagram shown in Fig. 4.9. In the forward path between nodes C and D (the components enclosed by the dashed lines in Fig. 4.9), an input current I_C is chopped by CH_3, integrated by C_2, differentiated by C_4, and then chopped by CH_6 again.

For simplicity, the nodes D and E are initially considered to be ideal virtual grounds. The relation between the current I_E flowing into integrator C_2 and the current I_B flowing into CH_6 is then given by:

$$K = \frac{I_B}{I_E} = \frac{sC_4}{sC_2} = \frac{C_4}{C_2} \tag{4.3}$$

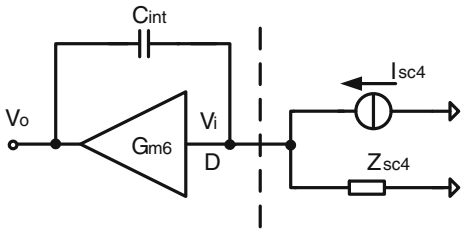

Fig. 4.10 Equivalent circuit of the integrator G_{m6} and C_{int}

Since this gain factor is not frequency-dependent, the operations of the two choppers CH_3 and CH_6 around the integrator C_2 and the differentiator C_4 cancel each other out. Hence, the relation between I_{SC4} and I_C is also K:

$$K = \frac{I_{SC4}}{I_C} = \frac{C_4}{C_2}. \tag{4.4}$$

It should be noted that if nodes D and E are not ideal virtual grounds, there will be a small error in the value of K expressed by (4.4), which will be neglected in this analysis.

Let $H(s) = V_0/I_{SC4}$ be the transfer function of the integrator built around G_{m6} and C_{int} (Fig. 4.9). If G_{m6} has a finite DC voltage gain of A_{06}, node D is no longer an ideal virtual ground, and then:

$$V_0 = -A_{06}V_i. \tag{4.5}$$

Since C_4 is chopped by CH_6, the switched-capacitor impedance Z_{SC4} looking into the chopper from the non-ideal virtual ground of the integrator (node D) is given by:

$$Z_{SC4} = 1/f_1C_4 \tag{4.6}$$

where f_1 is the chopping frequency of CH_6 and the output V_{out} is assumed to be a virtual ground. The action of C_4 and CH_6 can then be modeled by the Norton equivalent circuit shown in Fig. 4.10.

From Fig. 4.10, the input voltage V_i can be derived as:

$$V_i = I_{SC4}Z_{SC4} + (V_o - V_i)sC_{int}Z_{SC4} \tag{4.7}$$

By substituting (4.6) into (4.7), the transfer function $H(s)$ of the integrator can be calculated with:

$$H(s) = \frac{V_0}{I_{SC4}} = -\frac{Z_{SC4}A_{06}}{1 + sZ_{SC4}(1 + A_{06})C_{int}} \tag{4.8}$$

The loop gain $L(s)$ of the ORL can be expressed as

$$L(s) = K \cdot H(s) \cdot G_{m5}. \tag{4.9}$$

Substituting (4.4) and (4.8) into (4.9), the loop gain becomes,

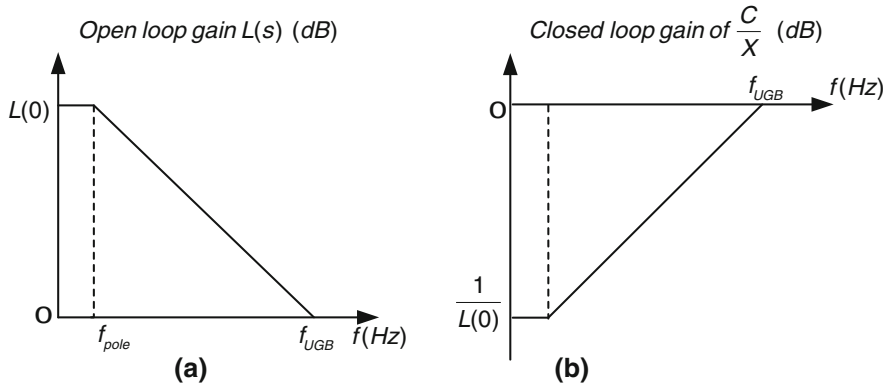

Fig. 4.11 **a** Open-loop gain L(s) of the ORL **b** Closed-loop gain of C/X

$$L(s) = \frac{C_4}{C_2} \cdot \frac{Z_{SC4} A_{06}}{1 + sZ_{SC4}(1 + A_{06})C_{\text{int}}} G_{m5}. \tag{4.10}$$

If $A_{06} \gg 1$ (4.10) can be simplified to

$$L(s) = \frac{C_4}{C_2} \cdot \frac{Z_{SC4} A_{06}}{1 + sZ_{SC4} A_{06} C_{\text{int}}} G_{\text{m5}}. \tag{4.11}$$

The loop gain $L(s)$ is plotted in Fig. 4.11a. It is a first-order low-pass function with a dominant pole that is related to the chopping frequency by:

$$f_{dominant,\, pole} = \frac{1}{2\pi A_{06} C_{\text{int}} Z_{SC4}} = \frac{f_1 C_4}{2\pi A_{06} C_{\text{int}}} \tag{4.12}$$

The DC loop gain $L(0)$ corresponding to the ripple-reduction ratio, i.e. the offset-reduction ratio, is given by:

$$L(0) = A_{06} G_{m5} \frac{C_4}{C_2} Z_{SC4} = \frac{A_{06} G_{\text{m5}}}{C_2 f_1} \tag{4.13}$$

The phase shift within the loop mainly originates from three blocks: integrator G_{m21} and C_2, a differentiator C_4 and an integrator C_{int}. In this design, C_4 = 5pF, C_{int} =80 pF, f_1 = 30 kHz, A_{06} is about 114 dB, so the dominant pole is at around 0.8 mHz. Since the phase shift of the first two blocks is cancelled out, the feedback loop is a stable first-order system having a phase margin close to 90°, i.e. it is inherently stable.

The closed-loop gain C/X between nodes C and X in Fig. 4.9 is plotted in Fig. 4.11b. The transfer function is given by

$$\begin{aligned}\frac{C}{X} &= \frac{1}{1+L(s)} \approx \frac{1+sZ_{SC4}A_{06}C_{\text{int}}}{sZ_{SC4}A_{06}C_{\text{int}}+\frac{C_4Z_{SC4}A_{06}G_{m5}}{C_2}} \\ &= \frac{C_2}{C_4Z_{SC4}A_{06}G_{m5}}\cdot\left(\frac{1+sZ_{SC4}A_{06}C_{\text{int}}}{1+s\cdot\frac{C_2C_{\text{int}}}{C_4G_{m5}}}\right)\end{aligned} \tag{4.14}$$

This result indicates that the ORL effectively high-pass filters the offset and $1/f$ noise of the input stage. In this design, the DC loop gain is about 114 dB, which, disregarding other contributors to output ripple, means that even the worst-case ripple amplitude of 0.8 V should be reduced to microvolt levels. As seen in this approach, the ripple sensing point is at the integrator output, where the ripple is large.

The unity-gain bandwidth f_0 of the loop can be derived from (4.11) by setting $L(s) = 1$

$$L(s) = \frac{C_4}{C_2}\cdot\frac{Z_{SC4}A_{06}}{1+2\pi f_0 Z_{SC4}A_{06}C_{\text{int}}}G_{m5} = 1. \tag{4.15}$$

Thus the unity-gain bandwidth of the ORL is given by:

$$f_0 = \frac{G_{\text{m5}}C_4}{2\pi C_2 C_{\text{int}}}. \tag{4.16}$$

Increasing the unity-gain bandwidth of the ORL reduces the settling time of the loop. The parameter C_2 is determined by the frequency compensation, G_{m5} is chosen much weaker than the input transconductance G_{m3} to reduce noise contribution from the ORL. The other two parameters C_4 and C_{int} can be flexibly chosen according to (4.16). In this design, C_2 = 80 pF, $G_{\text{m5}} = G_{\text{m3}}/18$ = 14 μA/V, C_4 = 5 pF and C_{int} = 80 pF, so the unity-gain bandwidth is 1.74 kHz. The notch bandwidth is roughly equal to $2f_0$, i.e. about 3.5 kHz. It will be shown in Sect. 4.5 that this notch can be buried in a multi-path architecture.

In summary, the inherent stability of the ORL is the key advantage of the ORL compared to other ripple reduction techniques [4–6]. This implies that the notch width from (4.16) and the notch location, i.e., the chopping frequency, can be independently chosen. Compared to a switched-capacitor notch filter [4] and auto correction feedback [6], a relatively low chopping frequency can then be chosen, leading to low offset without the stability problems caused by excessive notch-filter phase shift. Moreover, the ripple sensing point is at the output of the amplifier, where the ripple is quite large. Thus, the ripple suppression ratio of our approach can be much larger than that of the ACFB loop [6].

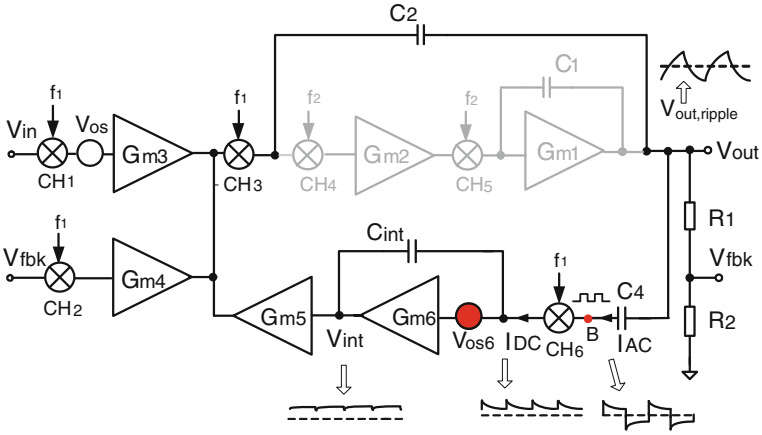

Fig. 4.12 Simplified block diagram of a three-stage CFIA with an AC-coupled ORL

4.4 Other Sources of Chopper Ripple

4.4.1 Cascode Buffer Isolation

The ORL suppresses chopper ripple originating from the input stage's offset, which is the major contributor to the output ripple. There is, however, a *second* source of ripple which originates from the offset of the integrator's amplifier G_{m6}, as shown in Fig. 4.12. This is because the offset of the transconductance stage G_{m6}, which is chopped by CH_6, appears as a square wave voltage at node B. This square wave appears across C_4, and cannot be distinguished from the output ripple. As a result, the ripple due to offset V_{os6} will not be completely cancelled out.

The ripple due to the offset of V_{OS6} (Fig. 4.12) can be mitigated in two ways: by autozero-stabilizing G_{m6} or by using a current buffer to isolate CH_6 from C_4. The auto-stabilization approach is shown in Fig. 4.13. The stabilization loop eliminates the offset of G_{m6} with a stabilization loop consisting of C_{A3}, C_{A4}, integrator G_{m8} and C_{A5} and transconductance G_{m7} [8]. As can be seen, the implementation becomes rather complicated, thus a cascode buffer is used here, as shown in Fig. 4.14. Compared to C_4, the cascode buffer 1 presents a much smaller parasitic capacitance C_{par} at the right side of chopper CH_6. C_{par} is around 0.6 pF, while C_4 is 5 pF, resulting in an 8-fold ripple reduction.

The ORL integrator was realized as a passive integrator built around a second cascode buffer (CB2), because this only requires half the capacitor area required by an active integrator. To minimize the effect of common-mode interference, the CFIA was implemented in a fully differential manner, as depicted in Fig. 4.15.

The introduction of the ORL does not significantly affect the noise performance of the amplifier. This is because CB2 and G_{m5} are located between the choppers CH_3 and CH_6 (Fig. 4.15) and so their $1/f$ noise contributions are chopped out.

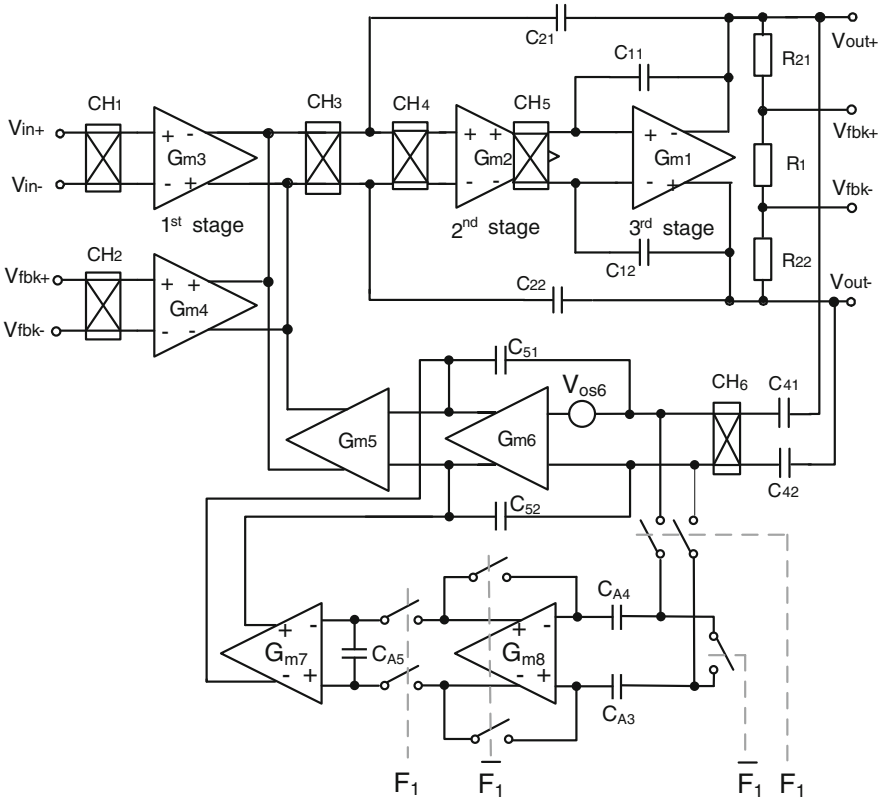

Fig. 4.13 CFIA with an ORL implemented with auto-zero stabilized integrator

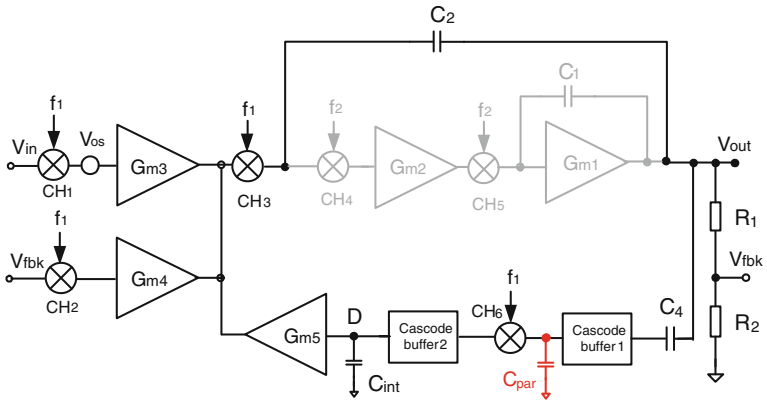

Fig. 4.14 CFIA with an ORL implemented with isolating cascode buffers

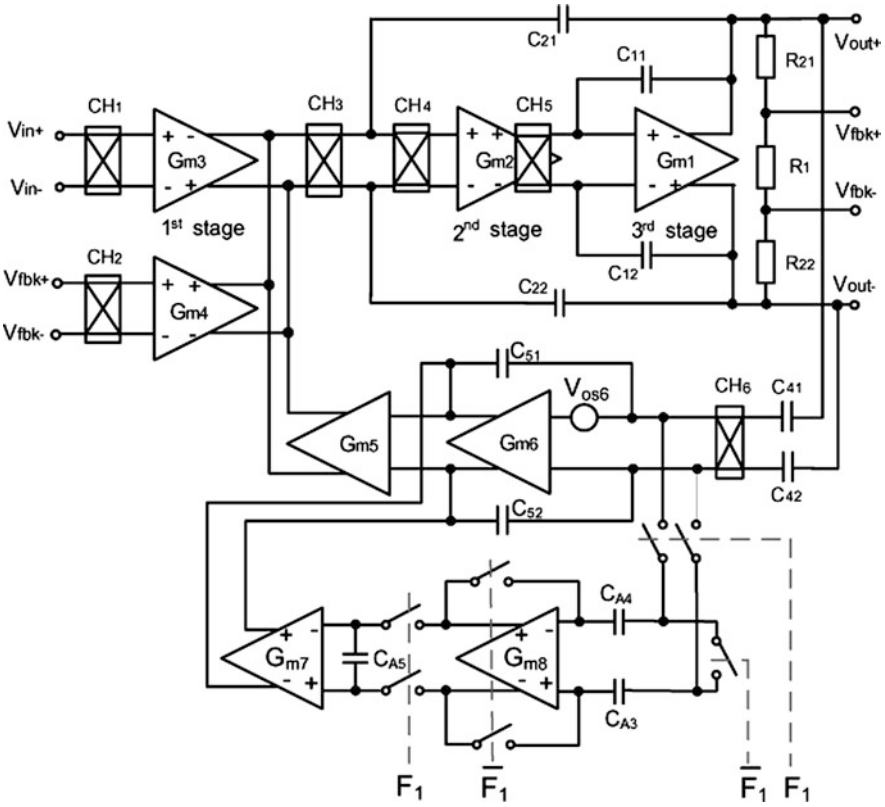

Fig. 4.15 Block diagram of the implemented fully-differential CFIA

Although, the cascode buffer 1 (CB1) is not chopped, its 1/*f* noise does not affect the CFIA's input-referred noise. This is because this is modulated to the chopping frequency by CH_6 (Fig. 4.16b), and then filtered out by C_{int} (Fig. 4.16c). After passing through CH_1, the filtered 1/*f* noise at the chopping frequency is demodulated to DC, as depicted in Fig. 4.16d. As long as the capacitor C_{int} is chosen large enough to filter out the modulated 1/*f* noise, the amplifier will still maintain its extremely low 1/*f* noise corner. Note that since the residual chopper ripple across C_{int} is up-modulated by CH_3, even-harmonics of f_1 are introduced at the amplifier output.

4.4.2 Chopper Ripple from the Intermediate Stage

The input and the intermediate stages of the CFIA are both chopped to eliminate their 1/*f* noise, thus providing sufficient gain to suppress the 1/*f* noise of the output

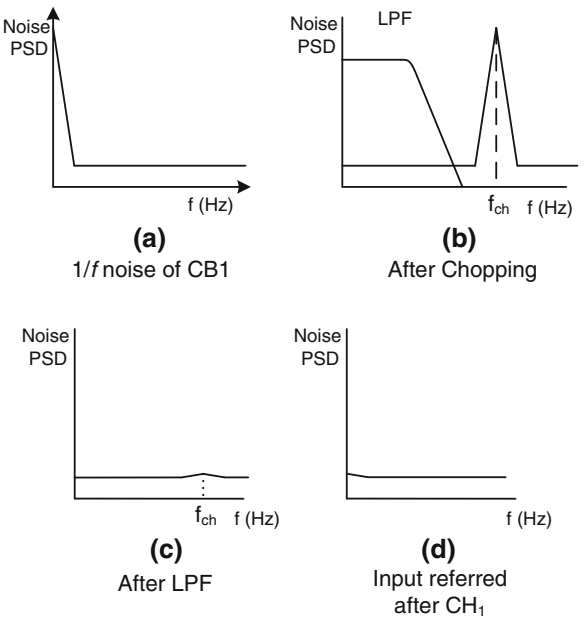

Fig. 4.16 1/f noise from CB1 passing through CH6, LPF and CH_1

stage down to 1 mHz. Thus, the chopped offset of the intermediate stage is another source of ripple.

Compared to the ripple due to the offset in the input stage, the ripple from the intermediate stage is much smaller, because G_{m2} is 13 times smaller than G_{m3}. Unfortunately, the ripple from the intermediate stage is only weakly affected by the presence of the ORL, because it originates within the frequency-compensation network, and so compared to the input stage ripple, is filtered by a different low-pass filter. In this design, the ripple associated with the intermediate stage is suppressed by chopping at a much higher frequency (510 kHz) than in the input stage. The resulting output ripple is then below 70 μV (at a gain of 200). Note that the increased frequency of the intermediate stage causes charge injection and clock spikes to the amplifier output through the Miller-compensation capacitors, resulting in a slightly increased offset.

4.5 Applying ORL to General Purpose Instrumentation Amplifiers and Operational Amplifiers

As discussed in Sect. 4.3, the ORL creates a notch at the chopping frequency. This is not a problem for the thermistor bridge application, because the bandwidth of interest is a few Hz, which is far below the chopping frequency of 30 kHz. As shown in [9], however, the notch can be eliminated by using a multi-path architecture. As shown in Fig. 4.17, a chopper amplifier with an ORL serves as the

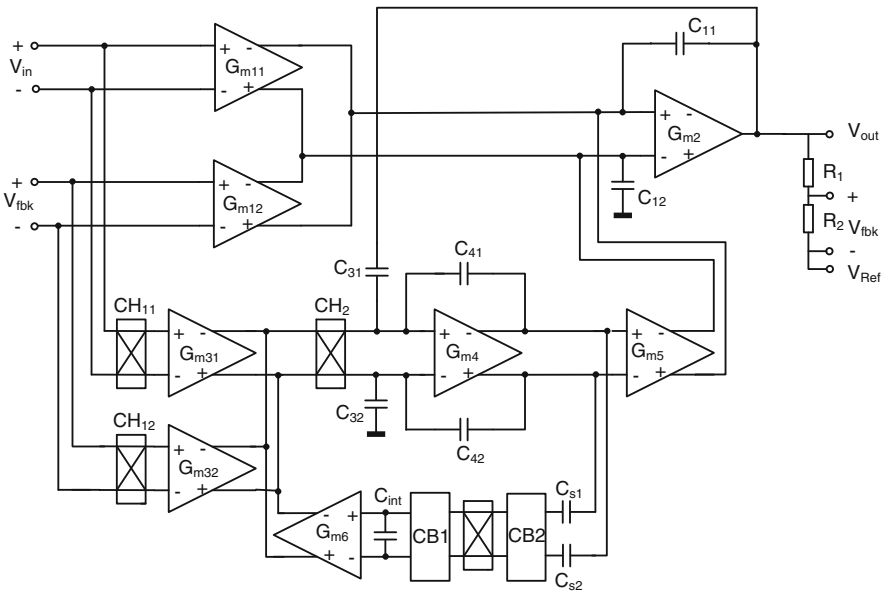

Fig. 4.17 Block diagram of the CFIA in a multi-path architecture

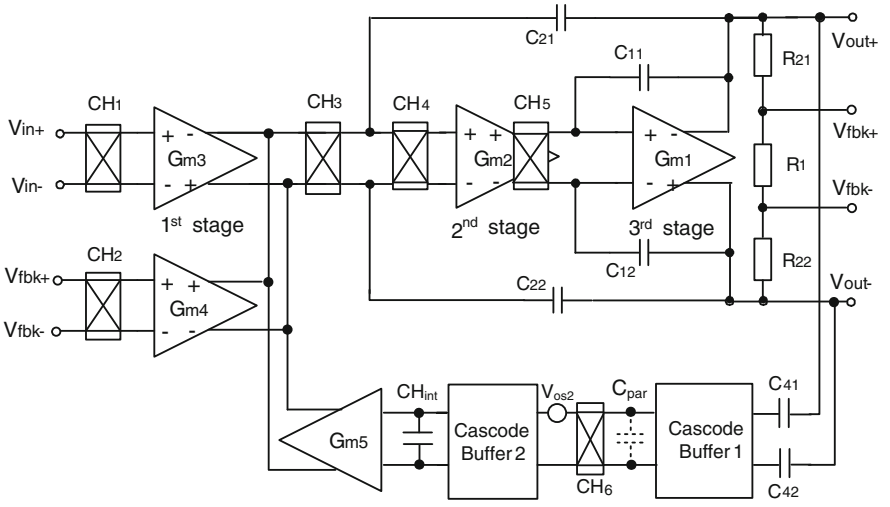

Fig. 4.18 Block diagram of the implemented fully-differential CFIA

low-frequency path, while the combination of G_{m11}, G_{m12} and G_{m2} serves as a high frequency path. The chopper amplifier's loss of gain at the notch frequency is compensated for by the gain of the high frequency path, resulting in a smooth single-pole response.

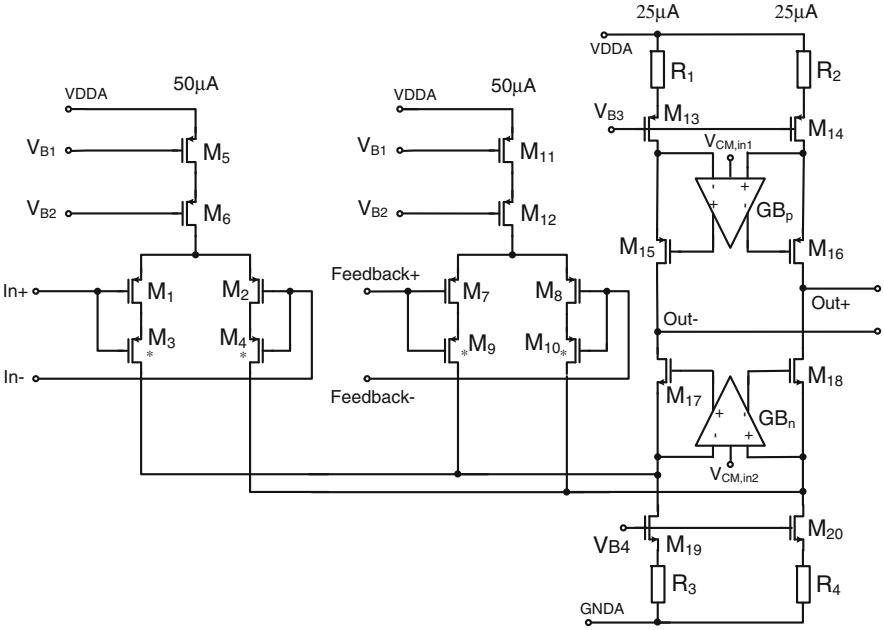

Fig. 4.19 Schematic of the input stage amplifier

Measurement results show that the multi-path CFIA achieves an offset of 2 μV, and a noise PSD of 21 nV/$\sqrt{}$Hz with an NEF of 9.6. By connecting the inputs of the input and feedback transconductors in parallel, it can be configured as a general purpose opamp which achieves an offset of 1.2 μV, and a noise PSD of 10.5 nV/$\sqrt{}$Hz with a NEF of 4.18 [9].

4.6 Circuit Implementations

For clarity, the fully-differential block diagram of the CFIA is shown again in Fig. 4.18 and the detailed implementation of each block will be described below.

4.6.1 The Input Stages

The input and feedback stages G_{m3} and G_{m4} are the most important parts of a CFIA, as they determine its gain accuracy and noise. To minimize the power consumption for a given noise specification, most of the power should be dissipated in the input stage. In this design, the input stage amplifier consumes a 161 μA supply current, which is 70 % of the total supply current dissipated in the

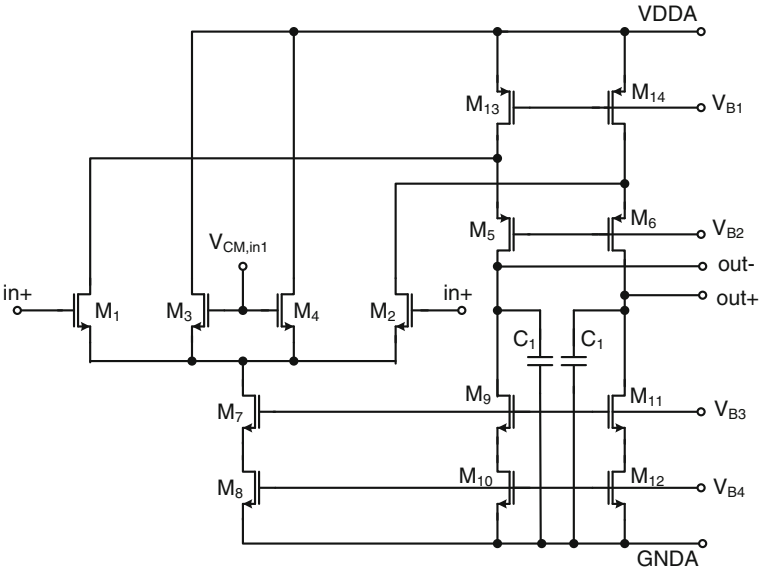

Fig. 4.20 Boost amplifier GB_p

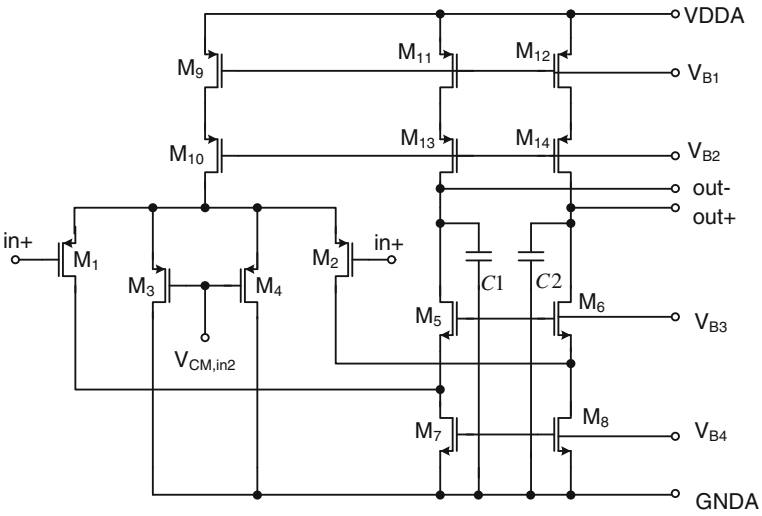

Fig. 4.21 Boost amplifier GB_n

CFIA. The input stage is implemented as a fully differential folded cascode gain-boosted topology, providing a high DC gain of 140 dB to suppress the noise and nonlinearity from subsequent stages.

Figure 4.19 shows the schematic of the input stage amplifier. Figures 4.20 and 4.21 depict the schematics of the boost amplifiers implemented in a fully

differential structure with input-regulated common-mode (CM) feedback [2]. The boost amplifier GB_p fixes the voltage across the current source M_{13} and M_{14} to the voltage of $V_{CM,in1}$ and the boost amplifier GB_n fixes the drain voltages of the input and feedback differential-input pair to the voltage of $V_{CM,in2}$, ensuring a very high output impedance.

Taking the boost amplifier GB_p for example (Fig. 4.20), the input differential pair (M_1 and M_2) is provided with two extra transistors (M_3 and M_4) in a common-source configuration, whose gates are connected to the input CM reference $V_{CM,in1}$. Due to the feedback between the input and output of the booster amplifier via the main cascode transistors, the output common-mode voltage is regulated in such a way that the input common-mode voltage is equal to $V_{CM,in1}$. Capacitors C_1 and C_2, as shown in Figs. 4.20 and 4.21, are added to the output terminals of the booster amplifier to augment stability.

This folded cascode gain-boosted input stage (Fig. 4.19) achieves a DC gain of 140 dB, which is determined by

$$A_{dc} = G_{m3} \cdot r_0 \tag{4.17}$$

where G_{m3} is the transconductance of the input G_m stage, r_0 is the output impedance seen from the output terminal of the input stage amplifier, which is determined by $G_{m15}r_{015}A_{GBp}r_{013}//[G_{m17}r_{017}A_{GBn}(r_{019}//G_{m3}r_{03}r_{01})]$. G_{m15}, G_{m17}, and G_{m3} are the transconductances of transistors M_{15}, M_{17} and M_3; r_{015}, r_{013}, r_{017}, r_{019}, r_{03} and r_{01} are the output impedances of transistors M_{15}, M_{13}, M_{17}, M_{19}, M_3 and M_1. A_{GBp} and A_{GBn} are the DC gain of the gain-boost amplifiers G_{Bn} and G_{Bp}.

The transconductances of G_{m3} and G_{m4} of the CFIA (Fig. 4.18) need to be well-matched for good gain accuracy. Consequently, the dimensions, bias currents and drain-source voltages of the input transistors should also be as well-matched as possible. The CM voltages of the two transconductances may differ, and so for good matching their G_m should be immune to CM voltage variations. Therefore, the drain-source voltages of the input transistors M_1, M_2, M_7 and M_8 were kept constant by low-threshold cascode transistors M_3, M_4, M_9 and M_{10}, as shown in Fig. 4.19. For the same reason, the current sources M_5 and M_{11} are also cascoded.

Compared to the resistor-degenerated differential pair incorporated with local feedback loops (Fig. 3.10 and Fig. 3.11), this simple PMOS differential pair shown in Fig. 4.19 is much more power-efficient, since the input and cascode transistors share the same bias current. However, its linear input range is then only ± 100 mV, which is good enough for bridge readout.

The input stage determines the noise of the CFIA, since the noise of the following stages is suppressed by the gain of the input stage. Assuming the degeneration resistors in the current sources have not been added, the main noise contribution is from the input transistors M_1, M_2, M_7, M_8, the current sources M_{19}, M_{20}, M_{13}, M_{14} and the input choppers. The input-referred noise is thus given by

$$e_n^2 = 4(e_1^2 + e_{13}^2(\frac{G_{m13}}{G_{m3}})^2 + e_{19}^2(\frac{G_{m19}}{G_{m3}})^2 + e_{in,chopper}^2 + e_{fbk,chopper}^2) \tag{4.18}$$

where e_1, e_{13}, e_{19}, $e_{in,chopper}$, $e_{fbk,chopper}$ are the noise voltages from transistors M_1, M_{13} and M_{19}, the chopper switches in CH_1 and the chopper switches in CH_2, respectively. As discussed in Sect. 4.1, the CFIA aims to achieve a noise PSD of 15 nV/$\sqrt{}$Hz, which is equivalent to a noise resistance of 14 kΩ. Next, each noise source in (4.18) will be analyzed successively.

The input and low-threshold cascode transistors M_1–M_4, M_7–M_{10} are all in weak inversion for better power efficiency (Fig. 4.19). Thus, the transconductance of the input differential pair is 250 μA/V with a 55 μA bias current. For each input transistors, the G_m/I ratio is 18. This corresponds to an equivalent noise resistance R_{in_Gm} of 4 kΩ and an input-referred noise PSD of 8 nV/$\sqrt{}$Hz. Considering both input and feedback stages, the total input-referred noise PSD is 8 nV/$\sqrt{}$Hz × $\sqrt{}$2 = 11.3 nV/$\sqrt{}$Hz.

To reduce the noise contribution from the current sources M_{19}, M_{20}, M_{13}, and M_{14}, resistive-degeneration is applied. The resulting equivalent noise resistance R_{CS_up} for the upper current source M_{13} (or M_{14}) is 8 kΩ, and the equivalent noise resistance R_{CS_down} for the bottom current source M_{19} (or M_{20}) is 2 kΩ.

The third noise contribution is from the choppers CH_1 and CH_2 (Fig. 4.18), which precede the input and feedback G_m stages. Since their 1/*f* noise is not chopped, they need to be fairly large. The switch size in the chopper is chosen to be 12 μ/0.7 μ as a compromise between 1/*f* noise and charge injection. The 1/*f* noise from the choppers CH_1 and CH_2 was simulated using PSS and PNOISE tools in Spectre RF [1].

For thermistor read-out application, the input and output CM voltages of the CFIA are 0.6 V and 2.5 V, respectively. Therefore, the on-resistances of these two choppers differ due to their different CM, and can be calculated as

$$R_{on\_in,chopper} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})} = 190\Omega \tag{4.19}$$

$$R_{on\_fbk,chopper} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})} = 480\Omega \tag{4.20}$$

where $R_{on\_in,chopper}$ and $R_{on\_fbk,chopper}$ are the on-resistance of the input and feedback choppers. It can be seen that the resistance of the feedback chopper is around 10 times smaller than that of one differential pair (4.2 kΩ). This means that the noise PSD from the choppers is more than 3 times lower than that of one differential pair, and thus is negligible.

Overall, the noise PSD of the input stage is given by:

$$\begin{aligned} \bar{V}_{input-stage} &= \sqrt{4kT(2 \times R_{in\_G_m} + 2 \times \frac{R_{in\_G_m}^2}{R_{CS\_down}} + 2 \times \frac{R_{in\_G_m}^2}{R_{CS\_up}})} \\ &= 15nV/\sqrt{Hz} \end{aligned} . \tag{4.21}$$

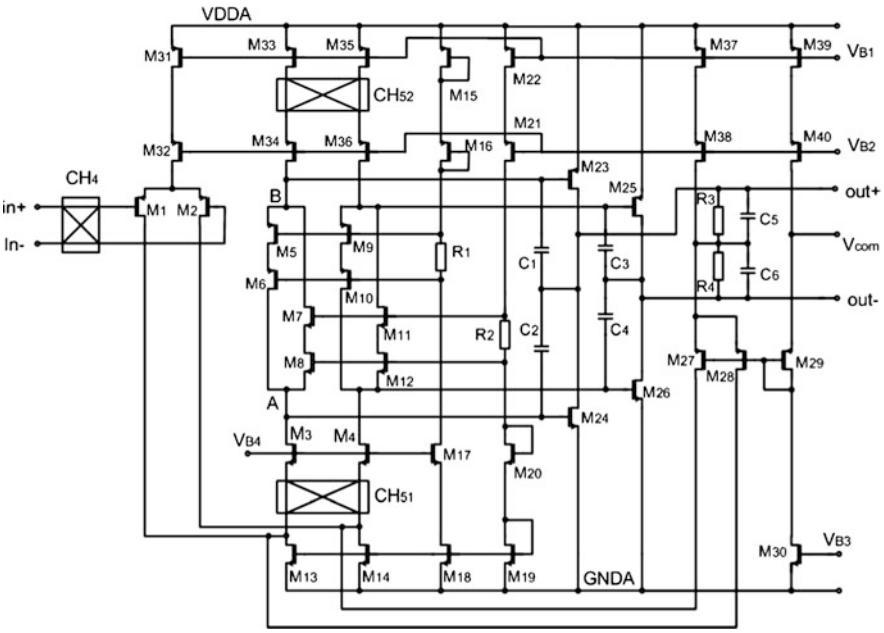

Fig. 4.22 Schematic of the intermediate and output stages

where $R_{\text{in\_Gm}}$, $R_{\text{CS\_up}}$ and $R_{\text{CS\_down}}$ denote the equivalent noise resistances of the input G_m stage, the upper degenerated current sources and the bottom degenerated current sources.

4.6.2 The Intermediate and Output Stages

The intermediate stage was implemented using a folded-cascode topology and the output stage was implemented in a class-AB fashion to achieve rail-to-rail output. Figure 4.22 depicts the schematic of these two stages.

To save power, the class-AB mesh structures were incorporated into the output branch of the intermediate stage [2]. The class-AB mesh was also cascoded to reduce the variation of the drain-source voltages of M_5, M_9, M_8, and M_{12} due to supply variation. The bias condition of the class-AB stage is determined by four translinear loops. For example, one of the translinear loops consists of M_{15}, M_{16}, M_5 and M_{23}, thus

$$V_{GS15} + V_{GS16} = V_{GS5} + V_{GS23} \tag{4.22}$$

With $V_{GS} = \sqrt{\frac{2I}{\mu_n C_{ox}\frac{W}{L}}} + V_{th}$,

$$\sqrt{\frac{I_{15}}{(\frac{W}{L})_{15}}}+\sqrt{\frac{I_{16}}{(\frac{W}{L})_{16}}}=\sqrt{\frac{I_{5}}{(\frac{W}{L})_{5}}}+\sqrt{\frac{I_{23}}{(\frac{W}{L})_{23}}}. \tag{4.23}$$

To maintain the same current-to-dimension ratio expressed by (4.23), the transistors within the translinear loops are all well-matched in the layout.

With $I_{16} = I_5$ and $(\frac{W}{L})_{16} = (\frac{W}{L})_5$ from (4.23), we can get

$$I_{23} = \frac{(\frac{W}{L})_{23}}{(\frac{W}{L})_{15}} \cdot I_{15}. \tag{4.24}$$

To achieve better settling, the demodulation choppers CH_{51} and CH_{52} should be located at the non-dominant poles of the intermediate stage. Therefore, chopper CH_{51} was located at the "quiet" sources of the cascode transistors M_3 and M_4. The same applies to chopper CH_{52}. Since the thermal noise of the intermediate stage is suppressed by the gain of the input stage, the differential pair consisting of M_1 and M_2 was biased at only 4 μA, resulting in a G_m of 20 μA/V. The unchopped cascode transistors M_3, M_4, M_{34}, and M_{36} are the main source of residual 1/*f* noise. However, this is suppressed by the gain of the preceding stages.

4.6.3 The Cascode Buffers

Figure 4.23 shows a schematic diagram of the cascode buffers. Transistors M_{23} and M_{24} serve as current buffer 2 (CB_2) to avoid chopping the large compensation voltage across C_{int} (around 200 mV). Transistors M_{25} and M_{26} act as current buffer 1 (CB_1) to isolate the chopper CH_6 from the sensing capacitors C_{41} and C_{42}. This isolation scheme (seen Fig. 4.18), provides lower capacitances C_{par1} and C_{par2} (compared to C_{41} and C_{42}) at the right side of CH_6, so as to reduce the ripple caused by CB_2's offset.

The ripple reduction ratio is determined by the DC loop gain of the ORL, as discussed in Sect. 4.3. A DC gain of 120 dB is required in the cascode buffer. Therefore, a gain-boosting topology was employed to increase its output impedance (Fig. 4.23a).

The offset of the booster G_{Bn} is chopped by CH_6, resulting in a square-wave voltage appearing across the drains of M_{25} and M_{26}. This voltage charges and discharges the parasitic capacitors $C_{par1,2}$, creating an AC offset current I_{AC1}. Furthermore, this square wave voltage modulates the bottom NMOS current sources to another AC offset current I_{AC2} [10]. The sum of these two AC currents charges and discharges the sensing capacitor C_{41} and C_{52}, appearing as another source of ripple at the amplifier output. The same goes for G_{Bp}, the offset of which has a similar effect.

To suppress this ripple, the position of the chopper was modified (Fig. 4.23b) so that these drain capacitances are located at the virtual grounds established by the gain-boosting amplifiers [10]. Now the mismatch of the bottom current sources

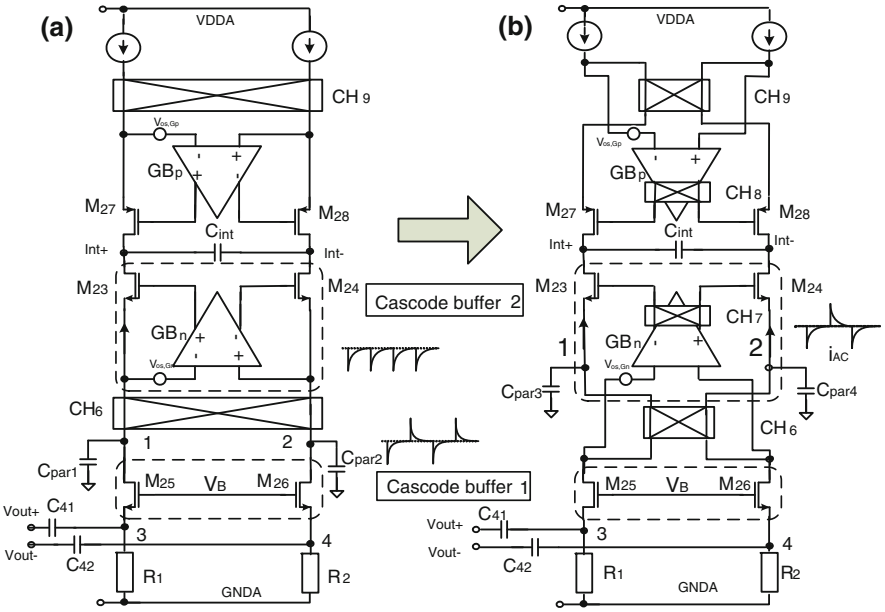

Fig. 4.23 Implementation of the gain-boosted cascode buffer

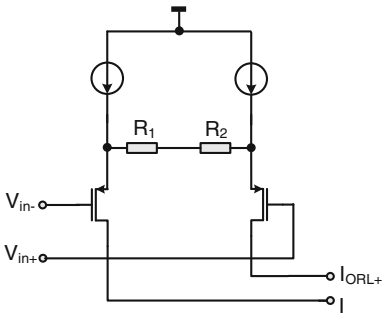

Fig. 4.24 Block diagram of the weak G_m stage G_{m5}

and the offset of GB_n appear as a square wave at nodes 1 and 2 (Fig. 4.23b). This square voltage charges and discharges $C_{par3,4}$, generating an AC current. To reduce this AC current, both CH_6 and M_{23}, M_{24} were implemented with minimum-size devices. Therefore, the residual ripple caused by the offset of GB_n and the mismatch of the bottom current sources is filtered out by the integration capacitor C_{int}. The AC current due to the offset of the upper current sources and GB_p is mitigated in the same manner.

Compensation Gm Stage G_{m5}

To minimize the noise contribution from the ORL and increase the input range of the compensation stage G_{m5} in Fig. 4.18, G_{m5} is implemented with a resistor-degenerated PMOS differential pair, as shown in Fig. 4.24. Its transconductance is 14 μA/V, which is 1/18 of the input stage G_{m3}.

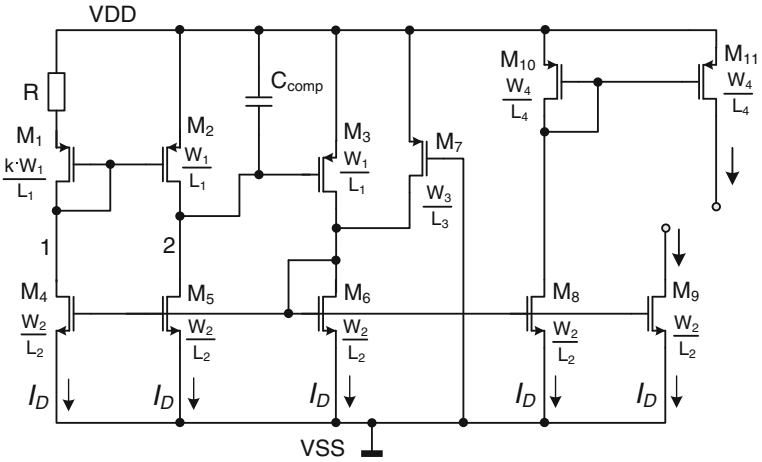

Fig. 4.25 Constant-G_m bias generator circuit

4.6.4 Constant-G_m Bias Circuit

A constant-G_m bias generator circuit is used to bias the transconductances in the CFIA so that they do not depend on the temperature or process variation, but to first order are only determined by a resistor. Figure 4.25 shows the schematic diagram of the constant-G_m bias circuit [11].

The currents flowing through M_4 and M_5 are set equal by using a feedback loop consisting of M_3, current mirrors M_4–M_6 and M_1–M_2. The feedback loop requires a compensation capacitor C_{comp} for stability. The feedback ensures that $V_{GS3} = V_{GS2}$ and thus $V_1 = V_2$, which minimizes channel length modulation effect in M_4 and M_5. The equal V_{DS} of M_4 and M_5 ensure a good power-supply rejection at low frequencies. At high frequencies, the power-supply rejection is reduced by the imbalance caused by C_{comp} [12]. M_7 is a very long transistor that produces a startup current to M_6 to raise its gate voltage, and then turn on the PMOS devices.

The transistors in the PMOS differential pairs in G_{m3} and G_{m4} operate in weak inversion for better power efficiency (Fig. 4.18), as well as transistors M_1–M_3 in the constant-G_m bias generator circuit. The bias current I_D of a transistor in weak inversion exhibits an exponential dependence on gate-source voltage V_{GS}, as given by:

$$I_D = I_S e^{\frac{V_{GS}}{\xi V_T}} \tag{4.25}$$

where $\xi > 1$ is a non-ideality factor that determines the weak inversion slope factor of a PMOS transistors, $V_T = kT/q$ and I_S is the specific current, as given by:

$$I_S = 2\xi \mu_p C_{ox} V_T^2 \frac{W}{L} \tag{4.26}$$

We can write $V_{GS1} + I_{D1} \cdot R = V_{GS2}$, thus

$$\xi \cdot V_T \cdot \ln \frac{I_D}{I_{S1}} + I_D \cdot R = \xi \cdot V_T \cdot \ln \frac{I_D}{I_{S2}} \tag{4.27}$$

As shown in Fig. 4.25, M_1 has the same L as M_2, but k times larger W, thus

$$I_{S1} = k \cdot I_{S2} \tag{4.28}$$

Substituting (4.28) into (4.27), I_D is then derived, which exhibits a PTAT property, as

$$I_D = \frac{\xi \cdot V_T \cdot \ln \frac{I_{S1}}{I_{S2}}}{R} = \frac{\xi \cdot V_T \cdot \ln k}{R} \tag{4.29}$$

The PMOS differential pair in the amplifier is biased with a multiple m of this current. If their current densities and their operation region are maintained the same as that of M_2, their transconductance will be, to first order, only determined by the resistors R and thus be insensitive to temperature:

$$G_m = \frac{mI_D}{\xi V_T} = \frac{\ln k}{R} \cdot m \tag{4.30}$$

After the implementation description of the analog blocks in the chopper amplifier, some other critical concerns about the chopper clock generator, chopper layout, and clock shielding will be discussed.

4.6.5 Chopper Clock Design and Layout

Chopper Clock Shielding

For chopper amplifiers, it is critical to minimize clock skew so as to reduce its effect on 1/*f* noise and offset (see Sect. 2.4.2). Therefore, the chopping clock signal must exhibit a 50 % duty cycle to ensure perfect offset cancellation. Furthermore, the transition of the chopper clocks must occur at the same moments to avoid any overlap or non-overlap between two complementary chopper clocks (Fig. 2.11).

As observed from the PSS and PNOISE simulations in Spectre RF [1], the rise and fall time of the clock pulse should be less than 3.3 ns for a 30 kHz chopping frequency (0.01 % of the clock period). Otherwise, the noise level near 0.01 Hz will increase. This implies that the longer the transition time, the more important the 1/*f* noise from the chopper switches becomes [13] since they are not chopped.

Figure 4.26 shows a chopper clock generator using a divider-by-2 D-flipflop to generate 50 % duty-cycle chopper clocks. To reduce the rise and fall time of the chopper clocks (clk_1 and clk_2), two inverter buffers INVA and INVB are parallel connected to the outputs of the D-flipflop. The resulting chopper clocks with steep transitions feed to the nearby choppers.

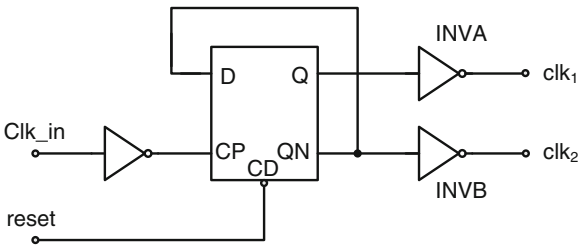

Fig. 4.26 Divider-by-2 chopper clock generator

Chopper Clock Layout

For chopper amplifiers aiming for μV offset, a careful chopper layout is essential. As discussed in Chap. 2, due to charge injection and clock feed-through, the imbalance of parasitic capacitors between ΔC_1 and ΔC_2 causes a residual offset (Fig. 4.27a). Furthermore, the charge injection due to ΔC (Fig. 4.27b) results in two bias currents, which together with the impedance mismatch between R_1 and R_2 cause another residual offset.

To mitigate these two effects, the absolute capacitive crosstalk from the clock lines towards one side of the chopper is minimized. Figure 4.28 illustrates the chopper layout [14]. In the layout, the poly clock lines only run perpendicular to the input signals line, but there is no overlap over the output signal lines. Thus, over-lap capacitances between the clock lines and the output signals are avoided. According to Fig. 4.27, the output terminals of this chopper layout should be chosen as the output of the input chopper (connected to the input of G_1) and the input terminal of the output chopper (connected to the output of G_1) to minimize the parasitic capacitances.

Due to transistor mismatch, another mismatch exists in the gate-source and gate-drain capacitance. Two dummy transistors M_{d1} and M_{d2} are used to ensure that transistors M_1–M_4 have the same surroundings. The gate line driving the dummy switch M_{d2} is necessary to make the crosstalk from f_{CH} to in_n equal to the crosstalk of f_{CH} to in_p by making the capacitances $C_{A1} + C_{A2}$ equal to $C_{A3} + C_{A4}$. To further reduce capacitive clock feed-through, a grounded metal 1 plate is used to shield the metal 2 clock lines from the signal lines. To conclude, the chopper layout depicted in Fig. 4.28 has matched switch transistors, minimal capacitive crosstalk towards the output, and balanced crosstalk from each clock line to the differential inputs and outputs.

Chopper Clock Shielding

The clock signal controlled the choppers need to be routed from the clock generation circuitry to the chopper switches. This may lead to clock feed-through and substrate feed-through.

To minimize the clock feed-through, an on-chip coaxial cable is made to restrict the clock coupling from the sensitive analog circuitry, as highlighted in Fig. 4.29. Figure 4.30a shows the cross section of the on-chip coax cables. In a three-metal process, the coaxial cable is made of three metal layers: metal 1–3. The layout of the two complementary chopper clocks is using metal 2.

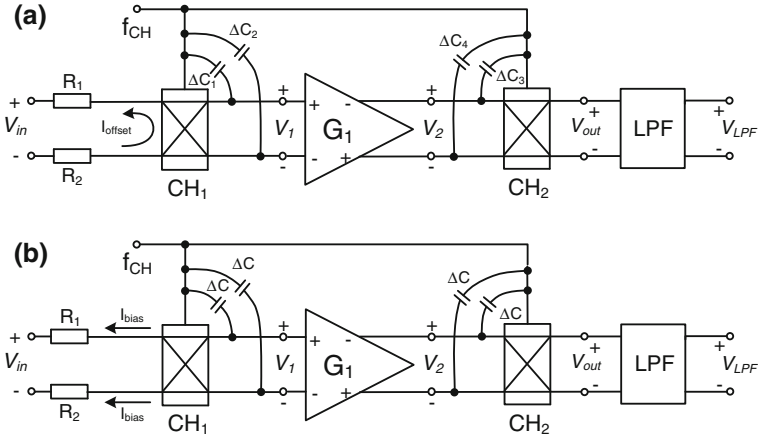

Fig. 4.27 **a** Offset current due to clock feed-through in a chopper amplifier. **b** bias current due to charge injection in a chopper amplifier

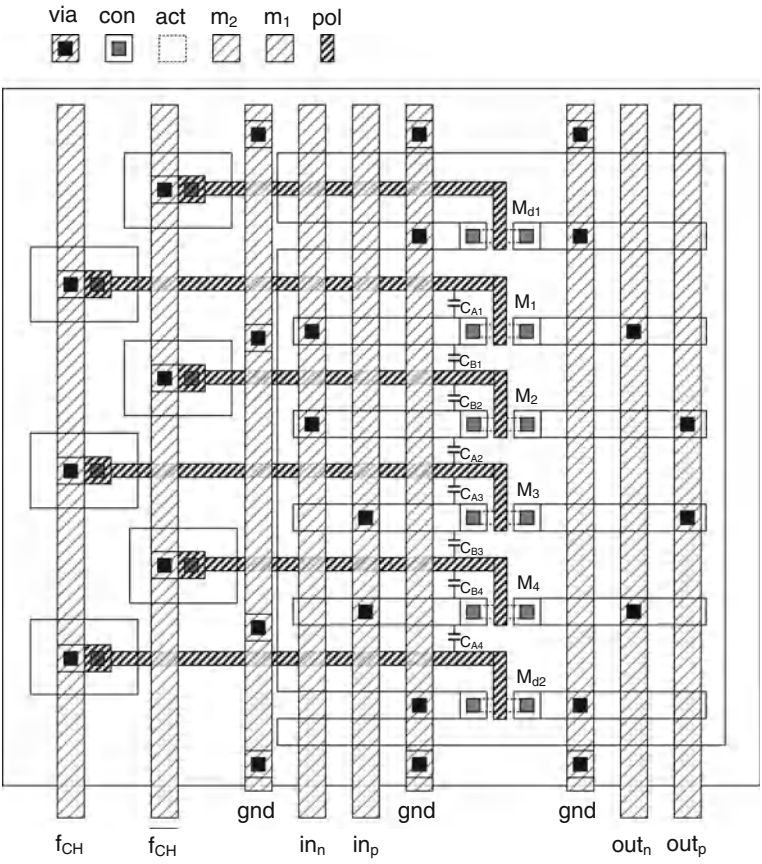

Fig. 4.28 Chopper layout where parasitic capacitor are shown

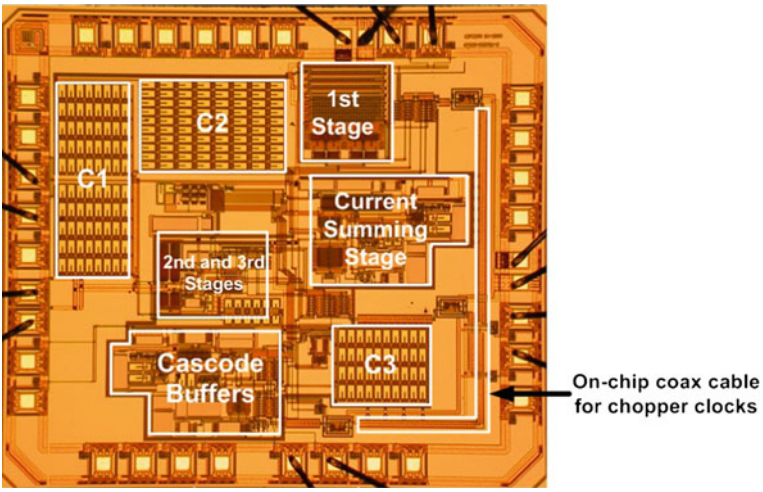

Fig. 4.29 Chip micrograph of the CFIA with on-chip coax cable for chopper clocks

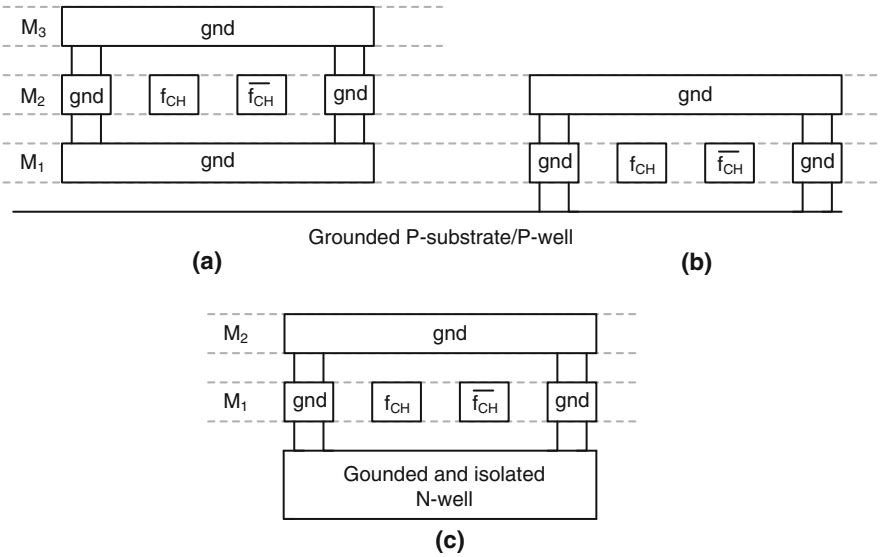

Fig. 4.30 Cross section of on-chip coaxial clock lines in (**a**) 3-metal process (**b**) a 2-metal process (use grounded P-substrate as the bottom plate) (**c**) a 2-metal process (use grounded and isolated N-well as the bottom plate)

In a two-metal process, the coaxial clock shielding can be made in two ways. Figure 4.30b uses the grounded P-substrate as the bottom plate for the clock shielding [14]. However, the disadvantage is that substrate coupling due to the capacitance from the clock lines to ground increases, thus relatively strong digital

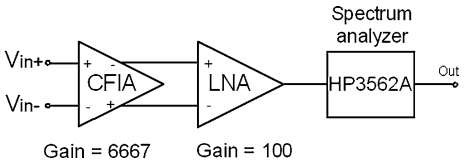

Fig. 4.31 Noise measurement set-up

buffers are needed to boost the clock signals. To avoid the substrate coupling issue, an isolated and grounded N-well can be used as the bottom plate in the coax cable, as shown in Fig. 4.30c.

4.7 Measurement Results

The CFIA with an ORL has been implemented in a 0.7 μm CMOS process. This process has low-threshold transistors, linear capacitors and high-resistivity poly resistors. The 4.8 mm^2 active chip area is shown in Fig. 4.29. The measured supply current is 230 μA from a 5 V supply voltage.

Noise

To ensure that the CFIA's 1/*f* noise is dominant, the noise measurements were made with the CFIA configured for a closed-loop gain of 6667 and followed by a low-noise amplifier (LNA) with a gain of 100, as shown in Fig. 4.31.

With these gain settings, the LNA acts as a differential to singled-ended buffer amplifier for the CFIA, so the contribution of the LNA and the HP3562A spectrum analyzer to the measured 1/*f* noise is negligible. Without chopping, the amplifier has a white noise floor of 15 nV/$\sqrt{}$Hz and a 1/*f* noise corner of 3 kHz. Chopping only the input stage resulted in a 1/*f* noise corner of 0.1 Hz. After chopping both the input and intermediate stages, the measured noise spectral density remained flat down to 1 mHz. Since the amplifier's offset is smeared out by the window function of the spectrum analyzer (HP3562A), the 1/*f* noise corner could not be accurately measured, but it is clearly below 1 mHz, as shown in Fig. 4.32. This confirms the simulation results shown in Sect. 4.2.

The measured noise spectrum from 10 Hz to 100 kHz is shown in Fig. 4.33. In this measurement, the CFIA is configured for a closed-loop gain of 200 and the LNA for a gain of 1. The measured output noise PSD is 3 μV/$\sqrt{}$Hz. Thus, it can be confirmed that the input-referred noise PSD equals: 3 μV/$\sqrt{}$Hz/200 = 15 nV/$\sqrt{}$Hz.

Closed-Loop Gain and Notch Measurement

As mentioned in Sect. 4.3, the ORL acts as a notch filter at the chopping frequency due to the synchronous demodulation in the ORL. Since the notch is quite narrow, it has little effect on the measured closed-loop response of the amplifier (Fig. 4.34). The zoom-in closed-loop response around the chopping frequency is shown in Fig. 4.35. The measured width of the notch, roughly 3.4 kHz wide at a gain of 20 and f_{ch1}=40 kHz, agrees well with the calculations presented in Sect. 4.3.

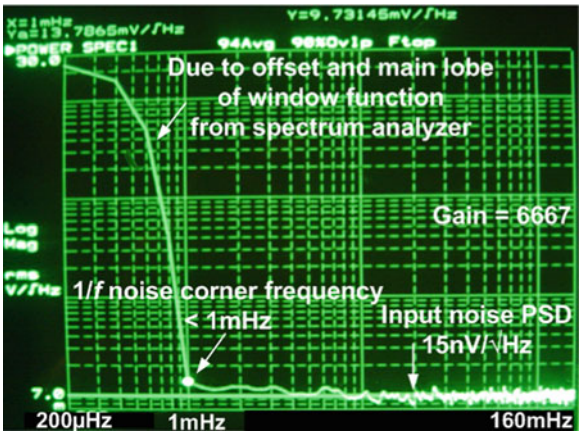

Fig. 4.32 Measured output noise spectrum from 200 μHz to 160 mHz (CFIA's gain = 6667, LNA = 100)

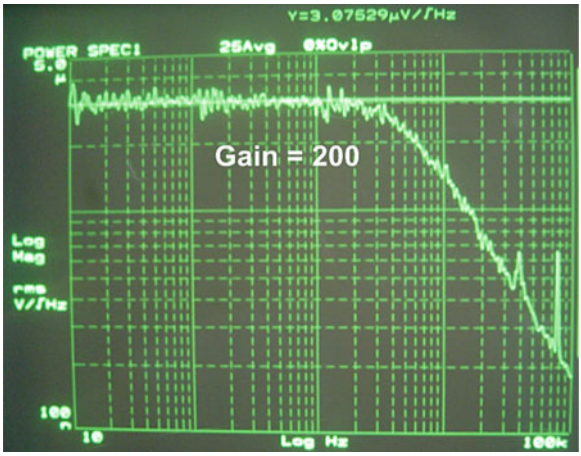

Fig. 4.33 Measured output noise spectrum from 10 Hz to 100 kHz (Gain of the CFIA = 200, LNA = 1)

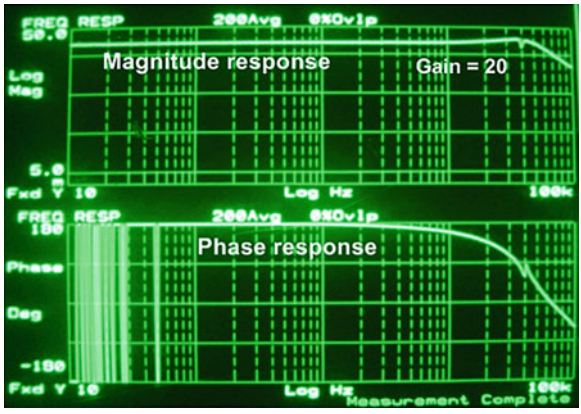

Fig. 4.34 Measured frequency response of the CFIA (gain of 20, f_{ch1} = 40 kHz, f_{ch2} = 510 kHz)

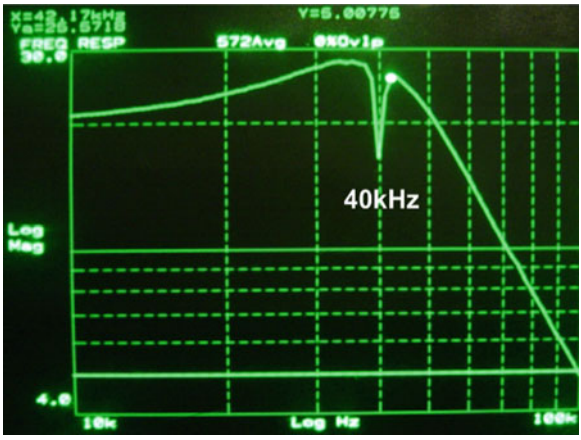

Fig. 4.35 Measured frequency response of the CFIA around the chopping frequency

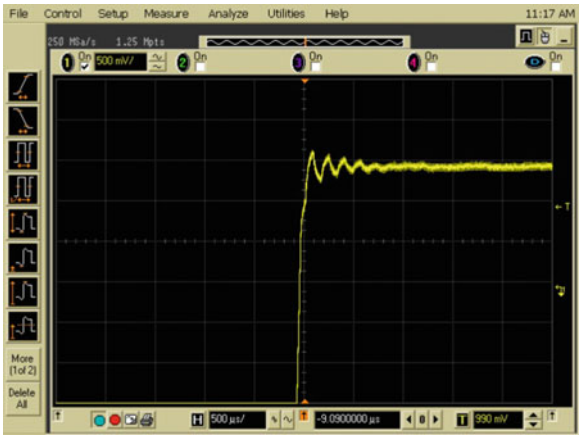

Fig. 4.36 Step response of the CFIA with the offset reduction loop

This notch will affect the settling of the amplifier with a step input, as it could cause some ringing before the amplifier output settles. The measured step response of the amplifier is shown in Fig. 4.36. The amplifier is configured at a gain of 100. Its output is a step from 0 to 3 V. It can be seen that the CFIA takes about 700 μs to settle.

Offset and Gain Error

Without chopping, the initial offset of the CFIA is less than 1.7 mV. Chopping only the input stage results in a measured offset of less than 1 μV. Chopping both the input and intermediate stages increases the offset to 5 μV, mainly because of the relatively high chopping frequency (510 kHz) used in the intermediate stage and the choppers in this stage could cause some charge injection and spikes through the Miller-compensation capacitors C_{11} and C_{12} to the amplifier output (Fig. 4.18), thus increasing the offset. The measured offset of 12 samples is shown

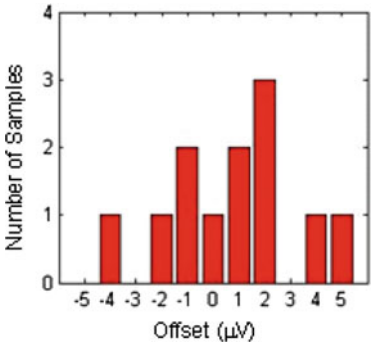

Fig. 4.37 Measured offset histogram of 12 samples

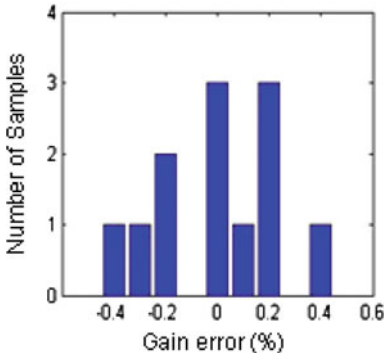

Fig. 4.38 Measured gain error histogram of 12 samples

in Fig. 4.37. Their measured gain error is shown in Fig. 4.38, and was less than ±0.5 % at a nominal gain of 200.

Output Ripple

The spectrum of the chopper ripple with and without the ORL is shown in Fig. 4.39 and Fig. 4.40. Since the frequency range of the HP3562A spectrum analyzer was limited to 100 kHz, the input choppers CH_1, CH_2, CH_3, and CH_6 were clocked at f_{ch1}=30 kHz in order to observe the 3rd harmonic of the chopping frequency. Measurements show that the amplitude of the output ripple at f_{ch1} was reduced by about 60 dB: from 48 mV to 41 μV. However, a larger second harmonic (78 μV) is also visible. This is due to the chopped mismatch of the degenerated current sources and the offset of the booster amplifiers (Fig. 4.23b), which CH_3 then up-modulates to the even harmonics of f_{ch1}. However, at the closed-loop gains for which the amplifier was designed (>20), the amplifier bandwidth is low enough to effectively filter out these harmonics. At a gain of 200, the amplifier's bandwidth is 4 kHz and the measured input-referred output ripple and noise are 0.55 μV(rms) and 0.95 μV(rms), respectively. Depending on the offset in the intermediate stage, the amplitude of the corresponding output ripple (at 510 kHz) varies from 0 to 70 μV.

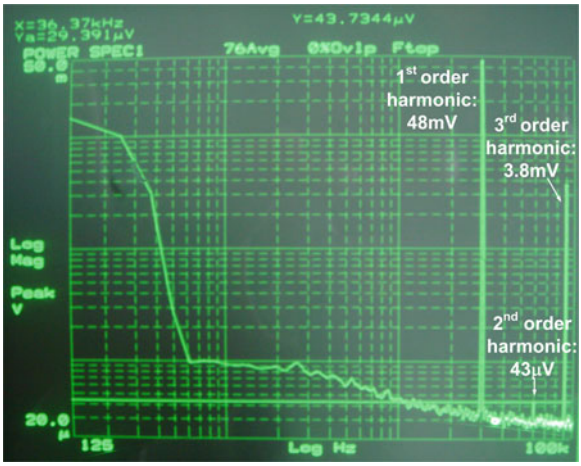

Fig. 4.39 Measured chopper ripple with the ORL "off" (125 Hz–100 kHz)

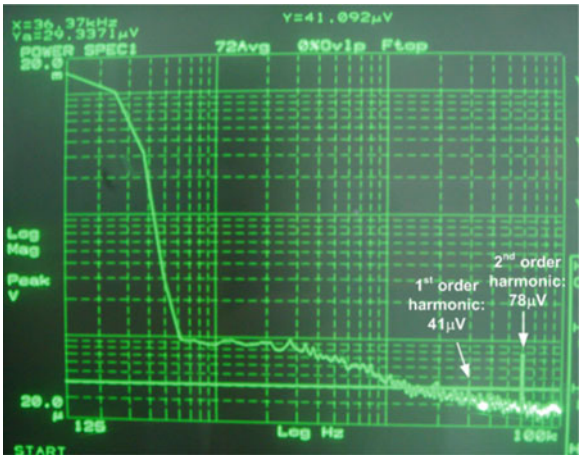

Fig. 4.40 Measured chopper ripple with the ORL "on" (125 Hz–100 kHz)

4.8 Benchmark and Conclusions

To interface a precision thermistor bridge, a three-stage stand alone current-feedback instrumentation amplifier (CFIA) has been realized. By chopping both the input and intermediate stages, their $1/f$ noise was effectively suppressed, while the $1/f$ noise corner of the output stage was suppressed by the gain of the preceding stages down to 1 mHz. A continuous-time offset reduction loop (ORL) was proposed to reduce chopper ripple. Due to its continuous-time nature, it does not cause noise aliasing, thus resulting in a very power-efficient solution compared to the use of auto-zeroing. The ORL dynamically compensates for the offset and thus eliminates temperature dependent offset and achieves low offset drift.

The ORL behaves like a narrow-band notch filter at the chopping frequency and its harmonics. As a result, the ORL has little effect on the amplifier's low-

Table 4.2 Performance comparison of low-power chopper amplifiers

	This work [7]	Yazicioglu [15]	Denison [16]	Fan [9]	Burt [4] in a two-opamp IA	Kusuda [17] in a two-opamp IA
Year of publication	2009	2008	2007	2010	2006	2011
1/*f* noise corner (Hz)	1 m	3	1	3	–	–
Noise PSD (V/$\sqrt{}$Hz)	15 n	55.8 n	94 n	21 n	76 n	9.2 n
Offset (μV)	5	–	–	2	6	0.78
GBW (kHz)	800 Stable Gain >20	350	20	900	350	3700
Chopping frequency (kHz)	30, 510	–	4	30	125	200
CMRR (dB)	>120	>120	100	137	130	>150 dB
PSRR (dB)	>120	90	–	120	113	>150 dB
Supply current (μA)	230	2.3	1.2	143	34	2940
Ripple suppression ratio	60 dB	–	–	60 dB	54 dB	–
Input-referred ripple	f_1 :0.41 μV $2f_1$:0.78 μV (gain = 100)	–	–	f_1 :0.45 μV $2f_1$: 0.39 μV (gain = 100)	–	–
NEF [18]	8.8	4.1	4.6	9.6	18.4	19.2
GBW/I_{supply}	3.5	152	17	6.3	10.3	1.25

frequency response, but creates notches in the amplifier's closed-loop transfer function around the chopping frequency f_1 (and its harmonics). For wide-band applications, this notch can be eliminated by using a multi-path architecture [9]. Since the ORL is a stable first-order system with a phase shift close to 90°, the notch width (determined by the unity-gain-frequency) and the notch location (determined by f_1) can be independently chosen [7]. Compared to the situation when a switched-capacitor notch filter [4] or an auto correction feedback is used [4.6], a relatively low chopping frequency can be chosen in this work. As a result, low offset can be achieved without the stability problems caused by excessive notch-filter phase shift. It has been proven that the concept of the ORL can be applied to general-purpose chopper CFIA or opamps [9].

To sum up, the advantages of the ORL compared to other ripple reduction techniques are:

- Continuous-time nature, thus incurring no noise folding → power efficient
- Inherently stable → lower chopping frequency and lower offset

Measurement results show that the ORL reduces the amplitude of the chopper ripple by 1100 times, to below the amplifier's own input-referred noise. Table 4.2

summarizes the measured performance of the CFIA and compared with the state-of-the-art chopper amplifiers. This CFIA achieves a worst-case 5 μV offset and a 1 mHz 1/*f* noise at noise PSD of 15 nV/$\sqrt{}$Hz while consuming only a 230 μA supply current. The NEF of the CFIA is 8.8, which is quite respectable [4, 15, 16–17]. To the author' knowledge, this represents the best LF noise performance ever reported for a stand-alone CMOS amplifier.

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Chapter 5
A Chopper Instrumentation Amplifier with Gain Error Reduction Loop

This chapter describes a stand-alone chopper current-feedback instrumentation amplifier (CFIA) that has improved performance compared to the one described in Chap. 4. It maintains the latter's low noise and low offset, and also obtains high gain accuracy and low gain drift without trimming. This is achieved by applying dynamic element matching (DEM) to the input and feedback transconductors so as to average out their mismatch. To eliminate the resulting DEM ripple, a gain error reduction loop (GERL) is employed to continuously null the G_m mismatch. The concept and analysis of DEM and the GERL is presented in Sects. 5.2 and 5.3. Then the similarities and differences between the offset reduction loop (ORL) and the GERL are discussed, together with their effects on the input and feedback G_m transfer functions.

Measurements show that *without trimming*, this CFIA achieves a gain error of 0.06 % and a maximum gain drift of 6 ppm/°C. It consumes only 290 μA supply current with an NEF of 11.2. Compared to previous CFIA with resistor-degenerated input stages, this work achieves a 4 × improvement in power efficiency.

5.1 Motivation

In instrumentation amplifiers, offset and gain error are the two dominant sources of error. For small input signals, offset and CMRR errors dominate; while for large signals, gain error dominates. The chopped CFIA presented in the previous chapter uses chopping to achieve microvolt-level offset and high CMRR (>120 dB) [1]. However, its gain error is about 0.5 %, even with careful layout (Sect. 4.7), and is thus the dominant source of residual error for input signals larger than a few hundred microvolts. For high-end strain gauge applications, the interface electronics should have a gain error less than 0.02 % [2]. Thus, the gain error of the CFIA needs to be reduced.

R. Wu et al., *Precision Instrumentation Amplifiers and Read-Out Integrated Circuits*, Analog Circuits and Signal Processing, DOI: 10.1007/978-1-4614-3731-4_5,

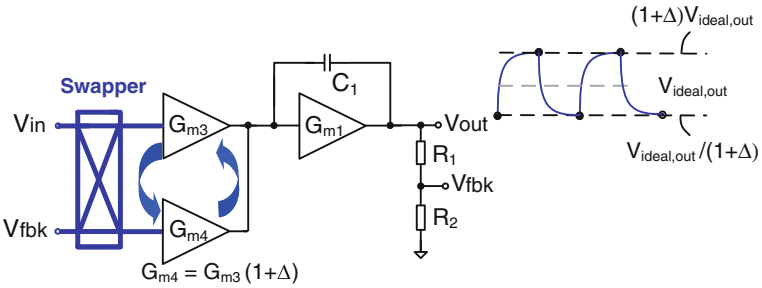

Fig. 5.1 CFIA with DEM ripple after applying DEM

Provided precision feedback resistors are used, the gain error of a CFIA is mainly determined by the mismatch between the input and feedback transconductances. To reduce this mismatch, one common approach is to use resistor-degenerated input stages [3, 4], as discussed in Sect. 3.3. However, the use of resistor degeneration leads to a significant loss in power efficiency. Furthermore, trimming the degeneration resistors [4] increases product costs. A better solution is to apply dynamic element matching (DEM) to average out their mismatch, thus permitting the use of simple differential pairs.

5.2 Dynamic Element Matching

As shown in Fig. 5.1, DEM can be implemented by swapping the positions of the input and feedback transconductors in the circuit. This only requires an input multiplexer, which we will call a "*swapper*". The use of DEM reduces the initial gain error from Δ to $\Delta^2/2$ [see Eq. (3.8)], Thus, a G_m mismatch of 2 % will be reduced to 0.02 %. In a practical CFIA, however, the common-mode (CM) dependence of G_{m3} and G_{m4} will limit the gain accuracy even if DEM is applied. In other words, the CM-dependent mismatch Δ_{cm} will not be suppressed by DEM [see Eq. (3.9)]. For simplicity, this issue will be neglected in the following analysis. However, a circuit-level technique to mitigate this problem will be described in Sect. 5.6.

The improved gain accuracy achieved by DEM comes at the expense of ripple at the amplifier output due to the modulated G_m mismatch. The amplitude of this DEM ripple is given by

$$V_{DEM,ripple} = V_{out1} - V_{out2} = 2\Delta \cdot V_{in} \cdot \frac{1}{\beta} = 2\Delta \cdot V_{ideal,out}. \tag{5.1}$$

where $V_{ideal,out}$ is the ideal output voltage of the CFIA. Eq. (5.1) indicates that the amplitude of the DEM ripple is a product of the mismatch Δ and the output signal. One common solution to eliminate DEM ripple is to trim the transconductances

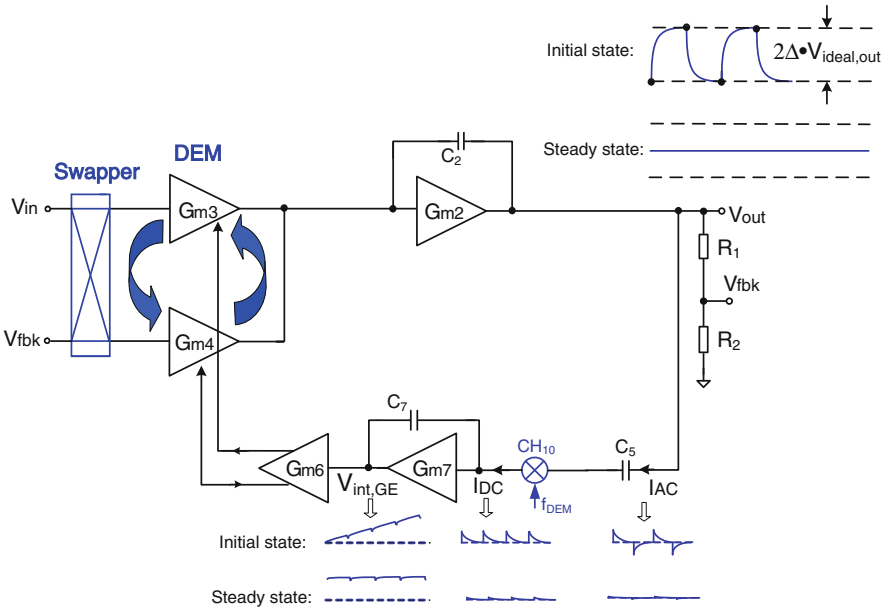

Fig. 5.2 Simplified block diagram of a CFIA with gain error reduction loop in the initial and steady state

[5]. However, trimming increases production costs and will not compensate for temperature drift. To avoid these issues, an automatic feedback loop—a GERL [6]—is employed to suppress DEM ripple.

5.3 Analog Gain Error Reduction Loop

5.3.1 Basic Concept

The GERL employs a synchronous detection technique similar to that used in the ORL. It extracts mismatch information from the amplitude of the DEM ripple, and then drives this ripple to zero by continuously nulling the G_m mismatch of the input and feedback transconductors, thus eliminating the need for trimming.

As shown in Fig. 5.2, the sense capacitor C_5 converts the amplifier's output ripple $V_{DEM,ripple}$ into an AC current I_{AC} whose amplitude is proportional to the derivative of $V_{DEM,ripple}$. This current is then demodulated by chopper CH_{10}, and the resulting DC current I_{DC} is integrated by G_{m7} and C_7 to generate a DC compensation voltage $V_{int,GE}$ proportional to the ripple amplitude. Via transconductance G_{m6}, this voltage is then used to cancel the mismatch between G_{m3} and G_{m4} by adjusting their tail currents. When the G_m mismatch is exactly compensated by the feedback loop, the output DEM ripple is ideally reduced to zero.

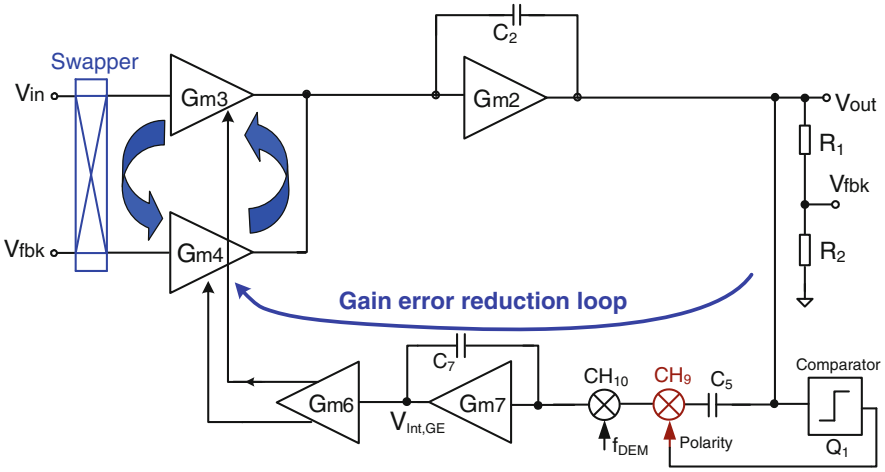

Fig. 5.3 CFIA with gain error reduction loop and polarity control switch

5.3.2 Qualitative Analysis

Unlike the offset reduction loop (see Sect. 4.3), which feeds back an additive offset-compensating signal, the GERL feeds back a *multiplicative* gain-compensating signal, which adjusts the ratio of G_{m3} and G_{m4}. The output DEM ripple is then the product of the residual mismatch and the output signal, and so the gain of the GERL will be signal dependent. This means that the loop gain not only depends on the amplitude of the output signal [shown in Eq. (5.1)], but also depends on the polarity of the output signal. Therefore, if no measures are taken, the GERL could turn into a positive feedback loop, causing $V_{int,GERL}$ to clip, and actually maximizing the CFIA's gain error. To maintain negative feedback, a polarity reversing switch is used to link the polarity of the GERL to that of the output signal (Fig. 5.3). In practice, this switch is a chopper, which is driven by a quantizer Q_1 that periodically monitors the polarity of the CFIA's output signal. However, the offset of the quantizer could cause it to generate incorrect polarity information, giving rise to large output ripple. To prevent this, an auto-zeroed quantizer is used with an estimated offset of less than 60 μV. At a closed-loop gain of 100, this translates into an error of 0.6 μV at the input of the CFIA, which, in most applications, is negligible.

5.3.3 Quantitative Analysis

To gain better insight into the operation of the GERL, its loop transfer function can be derived with the help of the simplified block diagram shown in Fig. 5.4. For simplicity, the polarity reversing switch CH_9, quantizer Q_1 (Fig. 5.3), choppers for offset reduction and ORL are neglected.

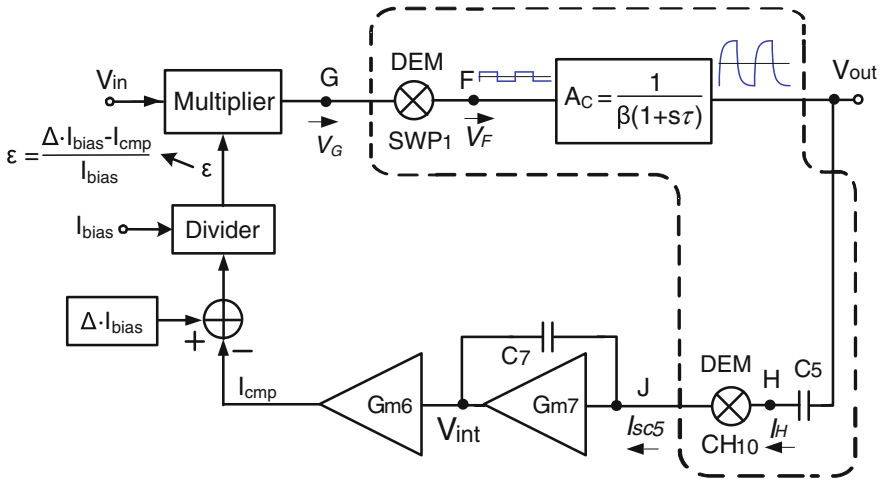

Fig. 5.4 Simplified block diagram of a CFIA with an GERL for loop-gain calculation

From (5.1), the output DEM ripple is a product of the input signal $V_{in,}$ the mismatch Δ between G_{m3} and G_{m4} and the closed-loop gain $1/\beta$. In line with this, V_{in} is *multiplied* in Fig. 5.4 by a normalized gain error ε, resulting in a voltage V_G, where ε represents the gain error after feedback loop compensation. For maximum power efficiency, G_{m3} and G_{m4} are biased in weak inversion and so their mismatch is proportional to their tail current mismatch. Thus, ε can be expressed as

$$\varepsilon = \frac{\Delta \cdot I_{bias} - I_{cmp}}{I_{bias}}, \tag{5.2}$$

where Δ is the initial mismatch between the input and feedback G_m stages, I_{bias} is the nominal bias current of input (or feedback) G_m stage and I_{cmp} is the compensation current from the GERL.

The voltage V_G is then fed to the DEM swapper SWP_1, where it is converted to a square-wave V_F. This voltage is then amplified by the CFIA's closed-loop gain A_C, and appears as an output ripple. This ripple is differentiated by C_5 into an AC current I_H, which is then demodulated by CH_{10} into a DC current I_{SC5}. For a sufficiently high DEM frequency, the CFIA's gain A_C can be modeled as an ideal integrator with a pole at DC:

$$A_C = \frac{1}{\beta(1+s\tau)} \approx \frac{1}{s\beta\tau}, \tag{5.3}$$

where the time constant τ determines the settling behavior of the output DEM ripple. The relation between the current I_H and V_F is then given by

$$K = \frac{I_H}{V_F} \approx \frac{sC_5}{s\beta\tau} = \frac{C_5}{\beta\tau}. \tag{5.4}$$

Since this gain factor is frequency-independent, the actions of the swapper SWP_1 and the chopper CH_{10} cancel each other, and so:

$$I_{SC5} = K \cdot V_G. \tag{5.5}$$

From its Norton equivalent circuit, the action of C_5 and CH_{10} can be modeled as a switched-capacitor impedance $Z_{SC5} = 1/f_{\mathrm{DEM}} \cdot C_5$ [1]. Assuming G_{m7} has a finite DC voltage gain of A_{07}, thus the transfer function *H(s)* of the integrator built around G_{m7} and C_7 (Fig. 5.4) can be calculated as

$$H(s) = \frac{V_{\mathrm{int}}}{I_{SC5}} = -\frac{Z_{SC5}A_{07}}{1 + sZ_{SC5}(1 + A_{07})C_7}. \tag{5.6}$$

The tail current mismatch $\Delta \cdot I_{bias}$ can be seen as the input of the loop since the feedback loop tries to cancel it to zero. Thus, the loop gain *L(s)* of the GERL is derived as

$$L(s) = -\frac{V_{in} \cdot K \cdot H(s) \cdot G_{\mathrm{m6}}}{I_{bias}} \tag{5.7}$$

By substituting (5.4) and (5.6) into (5.7) and assuming $A_{07} \gg 1$, the loop gain becomes

$$L(s) = V_{in} \cdot \frac{C_5}{\beta\tau} \cdot \frac{Z_{SC5}A_{07}}{1 + sZ_{SC5}A_{07}C_7} \cdot \frac{G_{m6}}{I_{bias}}. \tag{5.8}$$

Equation (5.8) indicates that the loop gain *L(s)* is a first-order low-pass function with a dominant pole that is related to the DEM frequency by

$$f_{dominant\ pole,GERL} = \frac{1}{2\pi A_{07}C_7Z_{SC5}} = \frac{f_{\mathrm{DEM}}C_5}{2\pi A_{07}C_7} \tag{5.9}$$

The phase shift within the loop mainly originates from three blocks: an integrator made from the single pole closed-loop transfer function A_{C}, the differentiator C_5 and the integrator C_6. In this design, $C_5 = 10$ pF, $C_7 = 40$ pF, $f_{\mathrm{DEM}} = 8$ kHz, A_{07} is 120 dB, so the dominant pole is at around 0.32 mHz. Since the phase shift of the first two blocks cancels out, the feedback loop behaves as a stable first-order system with a phase margin close to 90°.

The DC loop gain $L(0)$ corresponding to the DEM ripple reduction ratio is given by

$$L(0) = V_{in} \cdot \frac{C_5}{\beta\tau} \cdot Z_{SC5}A_{07} \cdot \frac{G_{m6}}{I_{bias}} \cdot = \frac{V_{in}A_{07}G_{\mathrm{m6}}}{\beta\tau f_{\mathrm{DEM}}I_{bias}} \tag{5.10}$$

As seen from (5.10), the DEM ripple reduction ratio depends on the magnitude of the input signal V_{in} and the DEM frequency f_{DEM}. In this design, f_{DEM} is 8 kHz, $G_{\mathrm{m6}} = 0.56$ μA/V and $I_{\mathrm{bias}} = 55$ μA. τ is determined by the unity-gain bandwidth of the CFIA and the feedback factor β, as given by

$$\tau = \frac{1}{2\pi f_{UGB,CFIA} \cdot \beta} = \frac{1}{2\pi}\frac{2\pi C_2}{G_{m3}}\frac{1}{\beta} = \frac{C_2}{G_{m3}\beta}. \tag{5.11}$$

where $G_{m3} = 270$ μA/V, $C_2 = 80$ pF and $\beta = 1/100$, thus $\tau = 30$ μs. With an input signal of 30 mV and the worst case 2 % mismatch, the DEM ripple amplitude without the GERL would be 120 mV at a closed-loop gain of 100. According to (5.10), however, the ripple reduction ratio is around 113 dB. This means that neglecting other contributors to the DEM ripple, even the worst-case DEM ripple should be reduced to microvolt levels.

Since the initial DEM ripple and the ripple reduction ratio $L(0)$ are both proportional to the ideal output signal $V_{ideal,out}$ (= V_{in}/β), the amplitude of the residual DEM ripple is signal-independent. This is an important advantage of GERL compared to trimming, because trimming can not eliminate the signal dependency in the DEM ripple, unless it is trimmed at all the input levels. With a signal-dependent residual ripple at the CFIA output (after trimming), the sampling moments of the succeeding ADC then become very critical and must locate at the zero-crossing points of the ripple. Otherwise, a signal-dependent sampling error occurs. While with a signal-independent residual ripple (with GERL), the sampling error only causes an offset, which can be easily calibrated out.

The unity-gain bandwidth f_0 of the loop can be derived from (5.8) by setting $L(s) = 1$

$$L(s) = V_{in} \cdot \frac{C_5}{\beta\tau} \cdot \frac{Z_{SC5}A_{07}}{1 + 2\pi f_0 Z_{SC5}A_{07}C_7} \cdot \frac{G_{m6}}{I_{bias}} = 1 \tag{5.12}$$

$$f_0 = \frac{V_{in}C_5G_{m6}}{2\pi\beta\tau C_7 I_{bias}} \tag{5.13}$$

In this design, with $V_{in} = 30$ mV, $C_5 = 10$ pF, $G_{m6} = 0.56$ μA/V, $\beta = 1/100$, $\tau = 30$ μs, $C_7 = 40$ pF and $I_{bias} = 55$ μA, the unity-gain-frequency f_0 is 41 Hz.

To verify the above analysis of the GERL and the analysis of the ORL described in Sect. 4.3, the settling times of the ORL and GERL were simulated. The CFIA is configured at a gain of 100 and a step input from 0 V to 40 mV is applied. Figure 5.5 shows the simulated waveforms of the step input, the step output of the CFIA, the integrator output of the GERL and the integrator output of the ORL.

It can be seen that the integrator outputs of the ORL and the GERL both settle in an exponential manner, confirming that these two loops are stable first-order systems. The time constant of the ORL is about 600 μs, while the time constant of the GERL is about 3 ms. The time constant of the GERL is thus in good agreement with the prediction of (5.13). During the transition time of the step input, the periodically sampled polarity-control quantizer is not fast enough to give the correct polarity information, thus the output of the GERL's integrator first goes in the opposite direction before settling to the correct mismatch compensation voltage.

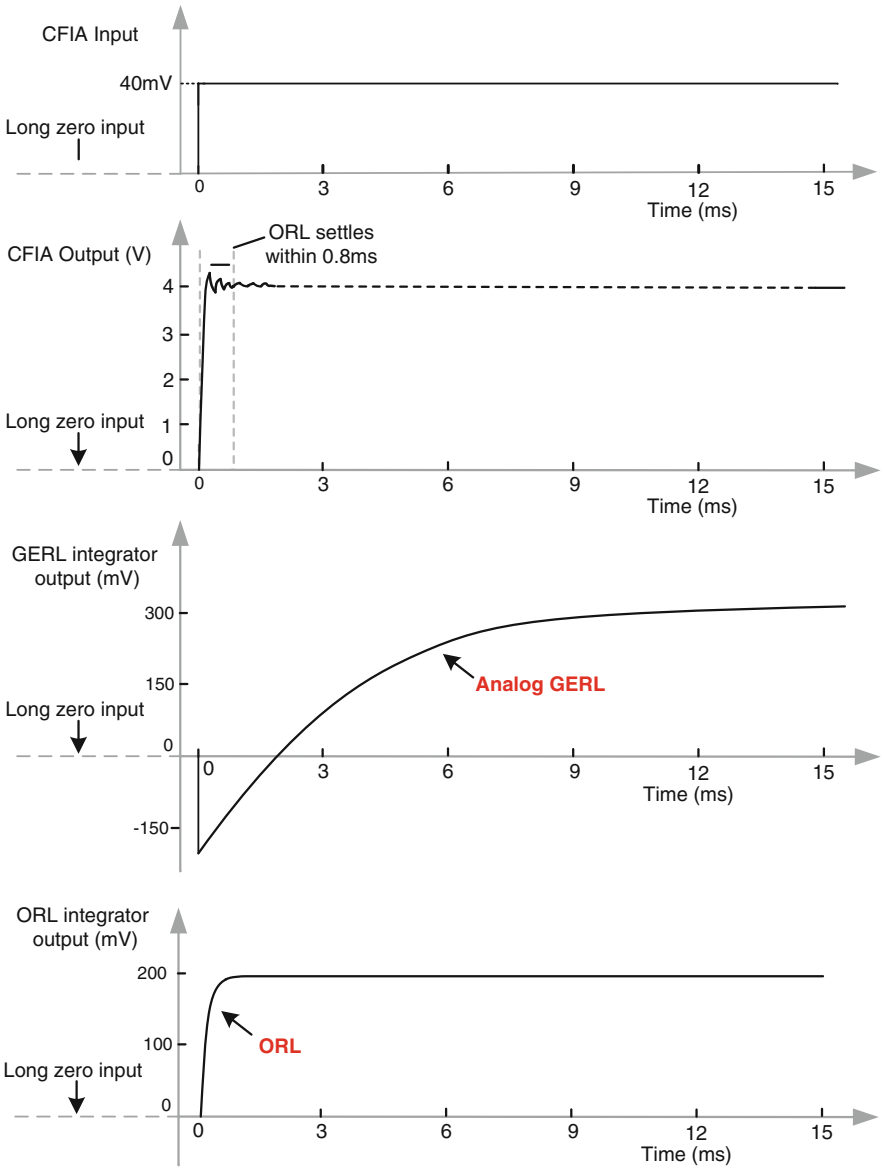

Fig. 5.5 Simulated settling time of the ORL and the GERL with a step input

5.4 Digitally-Assisted Gain Error Reduction Loop

From (5.8), the loop gain of the GERL is proportional to the input signal and so is zero for zero input. In this case, leakage causes the integrator output $V_{\text{int,GE}}$ to drift with a time constant of several seconds and eventually clip. The GERL will then

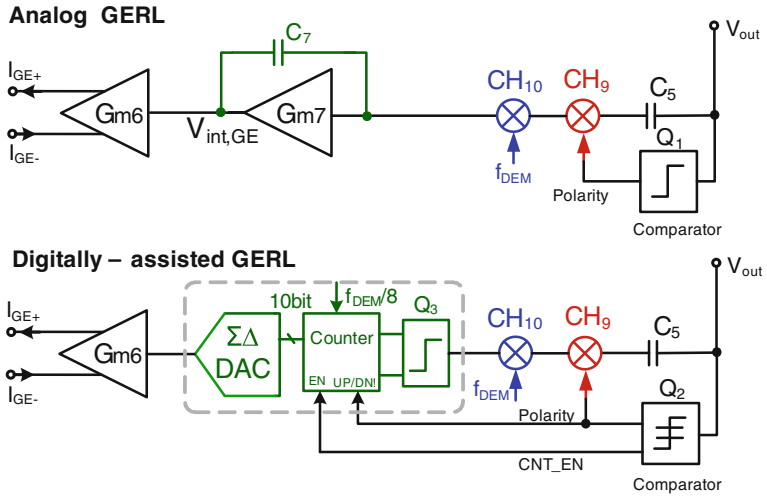

Fig. 5.6 Comparison between the analog GERL and digitally-assisted GERL

need to resettle whenever a finite input signal re-appears: within 14 ms for a 40 mV step input at a closed-loop gain of 100 and the loop parameters given above. To avoid the need for resettling, a digitally-assisted approach can be employed to store the mismatch information in the digital domain. The result is the digitally-assisted GERL shown in Fig. 5.6. For comparison, the analog implementation of the GERL is also shown. Here, the analog integrator is replaced by a comparator (Q_3), an up-down counter, a 1-bit first order $\Delta\Sigma$ DAC.

The comparator Q_3 determines the polarity of the demodulated DEM ripple. Its output then increments or decrements the up-down counter, whose output, in turn, drives the DAC. The DAC output drives a transconductance G_{m6} that, as in the analog GERL, generates the differential currents required to compensate for the G_m mismatch of the input and feedback transconductors. The function of the three-level quantizer Q_2 in Fig. 5.6 is to control the polarity of the loop via CH_9 for relative large input signal and also ensures that the integrator state is "frozen" for small input signals. In this way, the state of the loop will not drift in the presence of small input signals.

The threshold voltage to define the small inputs is chosen at a level when the output gain error equals the output-referred offset. For instance, assuming the closed-loop gain is 100, the gain error is 0.1 % and the offset is 2 μV, then the minimum input signal X, which ensures that the error induced by gain error is no less than the output offset error, is given by

$$X \cdot 100 \cdot 0.1\,\% \geq 2\mu V \cdot 100. \tag{5.14}$$

Thus, when the output signal becomes larger than 200 mV, the gain error dominates. Figure 5.7 shows the decision thresholds of the three-level quantizer. When the absolute amplitude of the CFIA output is smaller than 200 mV,

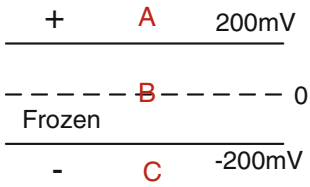

Fig. 5.7 Decision threshold of the three-level quantizer

the digital counter freezes the mismatch information, while when the absolute output amplitude is larger than 200 mV, the loop's polarity is controlled by the quantizer's polarity decisions.

At steady state, the output of the DAC will toggle between two LSBs, giving rise to a limit cycle within the loop. 10-bit resolution is enough to ensure that the resulting input-referred tone is well below the CFIA's noise level and also provides enough dynamic range to suppress the DEM ripple. Since the 10-bit counter is updated at a rate of $f_S = f_{DEM}/8 = 1$ kHz, the digitally-assisted GERL has a worst-case start-up time of $2^{10}/f_s = 1$ s. This can be significantly reduced by adjusting the counter's state in a successive-approximation fashion.

The usable signal bandwidth of the amplifier does not depend on the settling time of the GERL, but is determined by the DEM frequency ($f_{DEM} = 8$ kHz). For input frequencies higher than $f_{DEM}/2$, the quantizer Q_2 (Fig. 5.6) will not give correct polarity information since it is clocked at f_{DEM}. Thus, good gain accuracy is achieved in the frequency band lower than 4 kHz. However, this is not a problem because at high frequencies, the gain will probably not be accurate anyway due to the first-order roll-off of the CFIA's open-loop gain.

5.5 Comparison Between ORL and GERL

The combination of chopping and an ORL is similar to that of the combination of DEM and a GERL (Fig. 5.8). They both use modulation techniques to modulate the error (offset or G_m mismatch) to a high frequency, synchronously demodulate the output ripple, and then use a feedback loop to drive the error to zero. The main difference between them is that the ORL feeds back an *additive* offset-compensating current to cancel the offset, while the GERL feeds back a *multiplicative* gain-compensating current to fine-tune the tail currents of G_{m3} and G_{m4} in order to cancel their mismatch. Therefore, the GERL and the ORL can work independently of each other, provided that these two loops are clocked at different frequencies, and that the chopper ripple and gain error ripple are suppressed to a low enough level. Only prior to the complete settling of these two loops, the unsuppressed offset chopper ripple and DEM ripple may cause some interaction between these two loops.

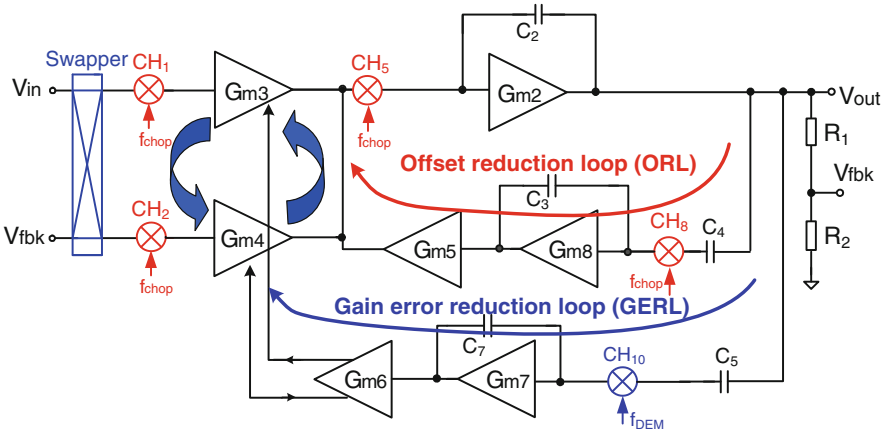

Fig. 5.8 Simplified block diagram of a CFIA employing chopping + ORL and DEM + GERL

5.6 The Effects of Chopping, DEM and GERL on CFIA Performance

Since the nonlinearities of the input and feedback G_m stages compensate each other, the typical nonlinearity of the CFIA is at the 30 ppm level (at a gain of 100). Figure 5.9a shows the typical transfer functions of G_{m3} and G_{m4} as a function of their input range. It is assumed that their transconductances decreases slightly with input amplitude. The presence of offset causes a horizontal shift between the two G_m characteristics. Chopping eliminates this offset and thus aligns the resulting average characteristics of G_{m3} and G_{m4} (Fig. 5.9b).

However, G_{m3} and G_{m4} still exhibit a transconductance mismatch of Δ. Applying DEM to G_{m3} and G_{m4} reduces their average gain error from Δ to $\Delta^2/2$, as shown in Fig. 5.9c. Compared to the situation without DEM, the use of DEM moves their average transcondutances $G_{m3,avg}$ and $G_{m4,avg}$ closer to each other. As a result, the nonlinearities of these two G_m stages better compensate each other, thus improving CFIA's linearity. The GERL improves matters further, since it drives the mismatch Δ to zero. As a result, $G_{m3,avg}$ and $G_{m4,avg}$ become even more closely *aligned* (Fig. 5.9d), which, in turn, results in a further improvement in the linearity of the CFIA. The same goes for the gain error and gain drift of the CFIA.

Transistor-level simulations are used to confirm the above analysis. The CFIA is simulated at a gain of 100 with 10 mV offset and with the offset reduction loop "on". A 2 % mismatch is added between the input and feedback transconductors. Figure 5.10 shows the simulated INL in four cases: (a) DEM phase 1; (b) DEM phase 2; (c) DEM only and (d) DEM + GERL. Without DEM, the CFIA's INL is around 90 ppm for both of the swapper phases. The use of DEM improves the amplifier's linearity from 90 ppm to 30 ppm. As described above, this is because DEM reduces the transconductor mismatch from Δ to $\Delta^2/2$, moving the transfer

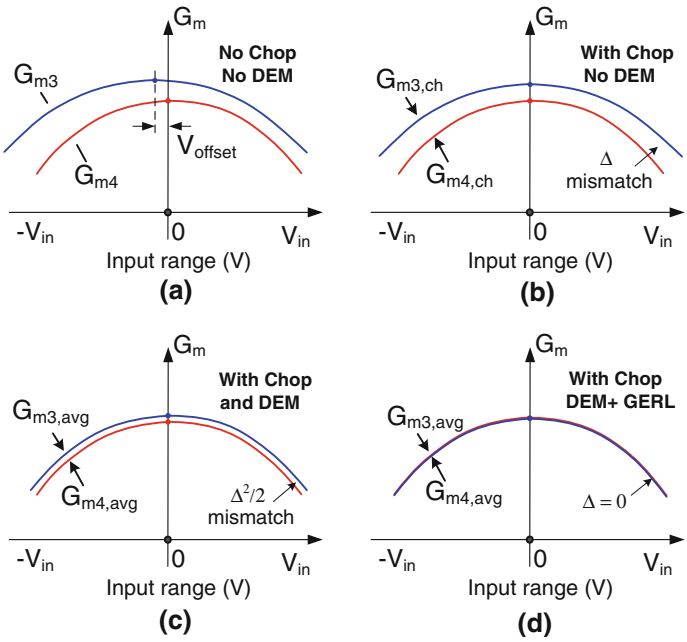

Fig. 5.9 Effects of chopping, DEM and GERL on the transfer functions of G_{m3} and G_{m4} in four cases: **a** No Chop and no DEM; **b** With chopping and no DEM; **c** With chop and DEM; **d** With chop, DEM and GERL

functions of $G_{m3,avg}$ and $G_{m4,avg}$ closer to each other. Turning on the GERL further improves the INL to 6 ppm, since the mismatch is now reduced to zero. It can also be seen that the combination of DEM and the GERL extends the CFIA's linear input range.

5.7 Circuit Implementations

5.7.1 Current-Feedback Instrumentation Amplifier with Analog Gain Error Reduction Loop

Figure 5.11 shows the block diagram of the implemented CFIA. Similar to the CFIA in Chap. 4, it consists of three fully-differential gain stages with an open-loop DC gain in excess of 250 dB. The input and feedback transconductors G_{m3}, G_{m4} as well as the intermediate stage G_{m2} are chopped, and their gain sufficiently suppresses the $1/f$ noise of the unchopped class-AB output stage G_{m1} down to 1 mHz [1]. As in [1], the chopping frequencies for the input and the intermediate stages are 32 kHz and 512 kHz, respectively. The chopper ripple caused by the

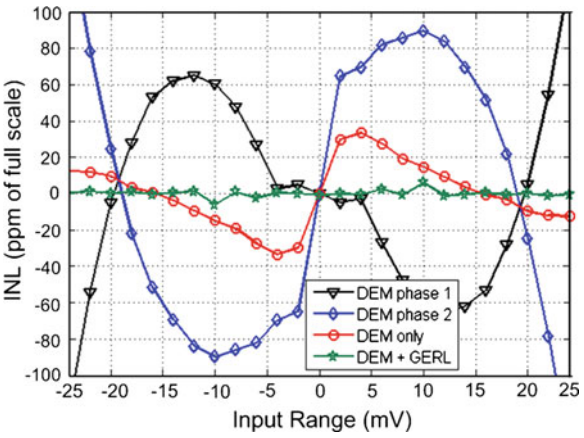

Fig. 5.10 Simulated INL with transistor-level circuit in four cases: **a** DEM phase 1; **b** DEM phase 2; **c** DEM only; **d** DEM + GERL

offset of G_{m3} and G_{m4} is suppressed by the ORL, while the higher frequency ripple of the intermediate stage is suppressed by the Miller-compensation network [1]. To minimize their noise contribution, the DEM swapper and the input choppers are merged and realized by four NMOS choppers CH_1, CH_2, CH_3, and CH_4. The timing of these choppers is also shown in Fig. 5.11. In DEM swap phase 1, choppers CH_1 and CH_4 are active (Fig. 5.12), while in DEM swap phase 2, choppers CH_2 and CH_3 are active (Fig. 5.13).

As in the ORL (Sect. 4.4.1), a current buffer before the demodulation chopper CH_{10} is used to minimize the DEM ripple due to the offset of G_{m7} (Fig. 5.8). To avoid chopping the large compensation voltage across C_7, the current buffer 4 (CB 4) is added to separate the chopper CH_{10} from C_7. The implementation of the intermediate stage G_{m2}, the output stage G_{m1}, the cascode buffer 3 (CB3) and the cascode buffer 4 (CB4) of the GERL is similar to that in the ORL [1].

Configured at a gain of 100, the gain setting resistors R_1, R_{21} and R_{22} of the CFIA are 300 Ω, 14.8 kΩ and 14.8 kΩ, respectively. As discussed in Sect. 4.2, the switched-capacitor (SC) impedance corresponds to a 26 MΩ input impedance, which is much larger than the equivalent resistance of the feedback network (300 Ω) and is high enough for most sensor read-out applications. In addition, the swapping action and the parasitic capacitances $C_{par1\text{-}4}$ also lead to switched-capacitor impedance between the input and feedback nodes of the amplifier. This impedance value is determined by $1/(2f_{DEM} \cdot 2C_{par1,2}) = 52$ MΩ, which is high enough and thus will not load the output stage of the amplifier.

5.7.1.1 Design Considerations and Implementation of DEM

To ensure that the GERL and the ORL only respond to the DEM ripple and the chopper ripple, respectively, the two loops are operated at different frequencies. Choosing a DEM frequency f_{DEM} higher than the input stage's chopping frequency

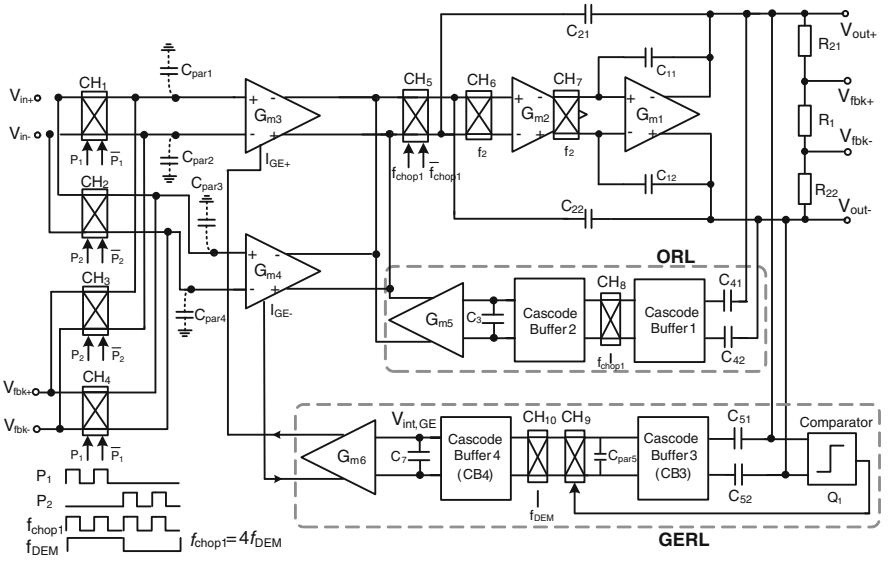

Fig. 5.11 Block diagram of a CFIA with ORL and analog GERL

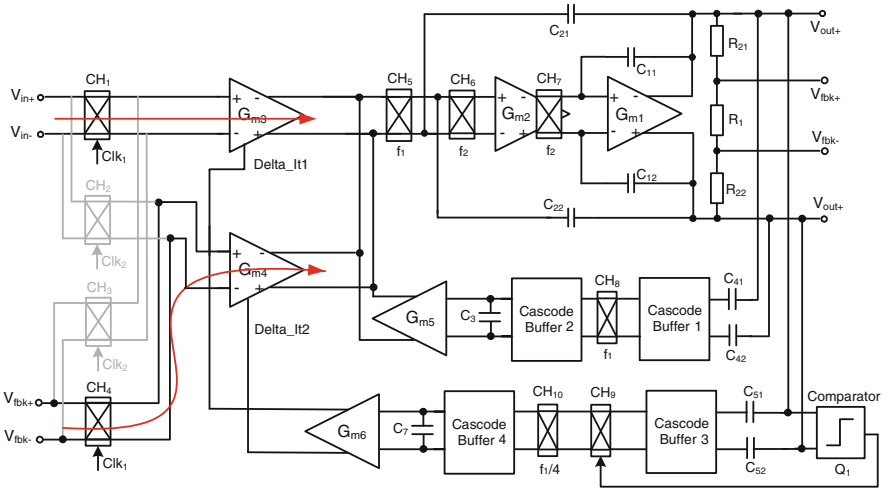

Fig. 5.12 CFIA with ORL and GERL in DEM phase 1

f_{chop1} causes extra switching activity during a chopping period, as shown in Fig. 5.14. The resulting spikes would increase the CFIA's residual offset [7]. To avoid this, f_{DEM} was chosen to be a sub-multiple of f_{chop1}.

The GERL generates a 2nd harmonic of f_{DEM} at the CFIA output. This is because the offset of CB3 (Fig. 5.13), after being chopped by CH_{10}, gives rise to

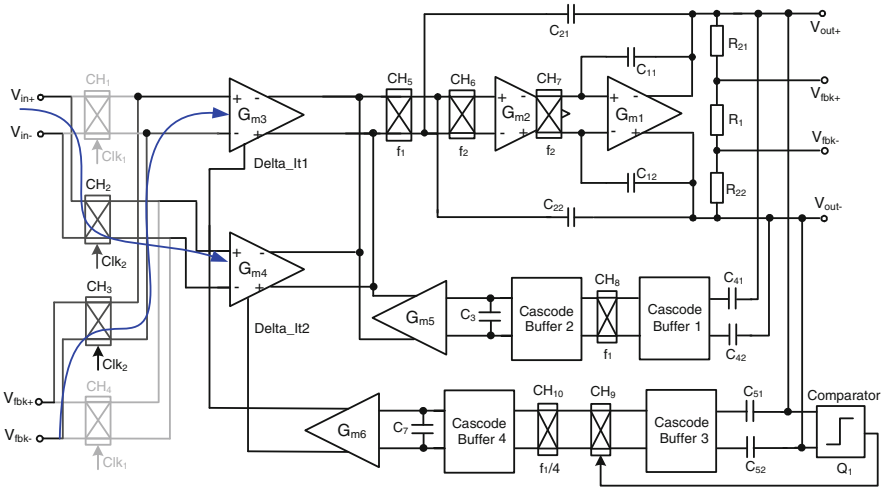

Fig. 5.13 CFIA with ORL and GERL in DEM phase 2

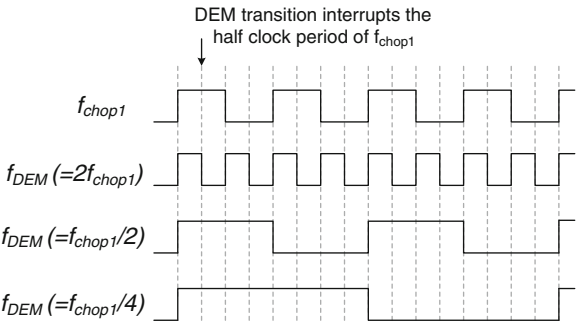

Fig. 5.14 The clock timing of f_{chop1} and f_{DEM} (f_{chop1}/f_{DEM} = 1/2, 2, 4)

chopper ripple across C_7. This ripple voltage is converted by G_{m6} into differential currents, which modulate the tail currents and consequently the transconductances of G_{m3} and G_{m4} at f_{DEM}. This results in a modulated gain mismatch at $f_{DEM,}$ which the swapper modulates to even harmonics of f_{DEM}. To ensure that the ORL does not sense these harmonics, we chose $f_{DEM} = f_{chop1}/4$, making the interference between these two loops negligible.

The noise contribution from the GERL is negligible because it is attenuated by the ratio of $G_{m3}/G_{m6} = 480$ and suppressed by the finite CMRR of the input stages. G_{m6} is implemented as a resistor-degenerated differential pair. Its bias current is chosen just large enough to cover the maximum expected mismatch (2 %) between G_{m3} and G_{m4}, thus minimizing the DEM ripple with zero input. Since G_{m3}'s tail current is 55 μA, the bias current of G_{m6} is around 1.1 μA.

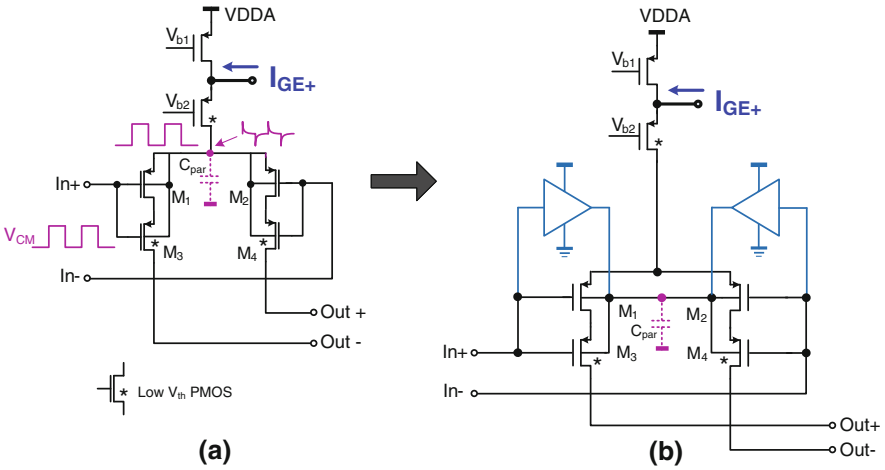

Fig. 5.15 **a** Input (or feedback) G_m stage with low-threshold cascodes; **b** Input (or feedback) G_m stage with class-AB boot-strap of the back- gate with unity gain buffers

5.7.1.2 Implementation of the Input and Feedback G_m Stages

The use of DEM ensures good gain accuracy, implying that the input and feedback transconductors can be implemented with simple differential pairs. Figure 5.15a depicts the input (or feedback) G_m stages made by this simple differential pair. Since they typically operate at different common-mode voltages, their CMRR was enhanced by cascoding the input transistors with low-threshold devices [1].

During the DEM transitions, the CM voltages of the transconductors will change abruptly. As a result, the parasitic capacitances between the substrate and the n-wells of the input devices, shown as C_{par} in Fig. 5.15 a, will be charged and discharged, causing large CM current spikes in the input stages. To bypass these spikes, two class-AB boot-strap unity-gain buffers are employed (Fig. 5.15b). Their detailed schematic is shown in Fig. 5.16. The n-wells of the input transistors M_1, M_2, and their cascodes M_3, M_4 are actively bootstrapped by class-AB buffers consisting of M_5–M_{10}. M_7–M_9 act as level shifters to accommodate the bias voltage of the class-AB stages. The source followers M_5 and M_6 provide a low-impedance path to ground, while M_{10} provides a low-impedance path to the supply. As a result, the bootstrap circuit effectively bypasses the DEM spikes to the supply rails.

5.7.1.3 Polarity Control Quantizer Q_1 in Analog GERL

As discussed in Sect. 5.3.2, the polarity of the GERL is linked to the polarity of the output signal by a low-offset quantizer and the estimated offset of the quantizer needs to be less than 60 μV. This offset level is achieved by adding an auto-zeroed preamp [8] preceding the quantizer, as shown in Fig. 5.17.

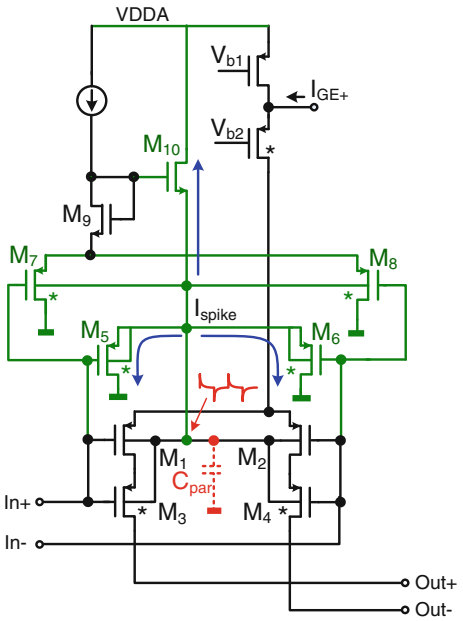

Fig. 5.16 Schematic diagram of the input (or feedback) G_m stages with class-AB bootstrapping of the back-gates

The auto-zeroed preamp works as follows. In the auto-zero phase, the input terminals are shorted by clock Φ_{AZ}, and the output of the cascode connects the offset nulling loop, which consists of an integrator and an auxiliary stage g_{m2}. The loop integrates the differential current generated by the cascode until the current through g_{m2} nulls the offset current. At the end of auto-zeroing cycle, the charge injection mismatch errors cause residual offset, as determined by

$$V_{res,offset} \approx \frac{V_{os1}}{g_{m2} \cdot R} + \frac{V_{os2}}{g_{m1} \cdot R} + \Delta V_{inj} \cdot \frac{g_{m2}}{g_{m1}} \tag{5.15}$$

where V_{os1} is the offset of g_{m1}, V_{os2} is the offset of g_{m2}, and ΔV_{inj} is the charge injection caused by switches which are located at the output of g_{m1} and controlled by Φ_{AZ}. By choosing a ratio of $g_{m1}/g_{m2} = 60$, the offset induced by charge injection errors is attenuated when input-referred. The amplification phase is controlled by clocks Φ_{AMP}, in the manner shown in Fig. 5.17. According to simulations, this auto-zeroed quantizer achieves a less than 60 μV offset. At a closed-loop gain of 100, this translates into an error of 0.6 μV at the input of the CFIA, which is small enough for most applications.

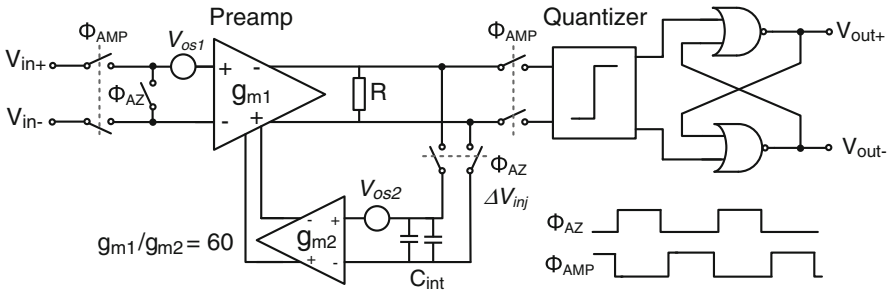

Fig. 5.17 Circuit diagram of an auto-zeroed preamp and quantizer

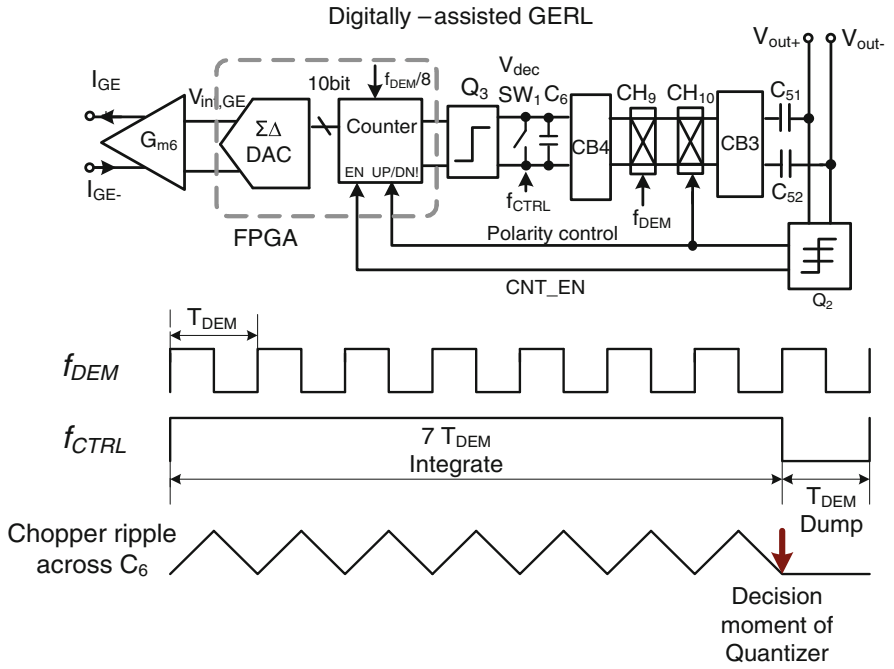

Fig. 5.18 Block diagram of the digitally-assisted GERL with the associated timing diagram

5.7.2 Current-Feedback Instrumentation Amplifier with Digitally-Assisted Gain Error Reduction Loop

As discussed in Sect. 5.4, the analog GERL needs to re-settle when an input step re-appears after a long zero-input. To avoid this, the analog integrator can be replaced by a digital integrator to store the mismatch information in the digital domain. The result is the digitally-assisted GERL shown in Fig. 5.6 and whose detailed implementation is depicted in Fig. 5.18.

To mitigate the effect of the comparator Q_3's offset and hysteresis, a chopped integrate-and-dump pre-amplifier was realized by integrating the demodulated DEM ripple on C_6 for seven DEM periods (Fig. 5.18). The decision of the comparator is then made. During the next DEM period, SW_1 resets the voltage on C_6. Thus, the gain of the preamp is $16 \times 7 = 112$ (41 dB), where $C_{51}/C_6 = 16$. This gain is sufficient to reduce the offset of Q_3 to below 60 μV. The timing of f_{CTRL} ensures that the positive time is seven times the negative time in one DEM period (Fig. 5.18). The quantizer Q_3 makes the decision exactly at the end of the seventh DEM period, thus it does not sample the residual ripple caused by the chopped offset in CB3. Since the ripple is filtered out by this discrete-time sampling, the second harmonic of f_{DEM} is eliminated in the digitally-assisted GERL.

5.7.2.1 10-bit ΔΣ DAC Implementation

As discussed in Sect. 5.4, the output of the DAC will toggle between two LSBs, giving rise to a limit cycle. A DAC with 10-bit resolution is required to push this limit cycle below the CFIA's noise level and also provide enough dynamic range to suppress the DEM ripple. It was decided to implement the digital logic for the digitally-assisted GERL off-chip, therefore, an over-sampling ΔΣ DAC is a good choice since it eases off-chip implementation. Furthermore, it uses over-sampling and noise shaping instead of component matching to achieve a high resolution. By employing a high OSR, the quantization noise can be shaped to a high enough frequency. Thus, a small and compact on-chip RC filter is enough to filter out the shaped quantization noise. Moreover, dithering can be employed to de-correlate the quantization noise and suppress the limit cycles, a first-order digital ΔΣ modulator was found to be good enough.

Figure 5.19 depicts the block diagram of the over-sampling ΔΣ DAC. It consists of an interpolation filter, a 1-bit first-order digital ΔΣ modulator and an analog low-pass filter (LPF). The ten-bit counter is updated at $f_{CNT} = 1$ kHz, thus the signal bandwidth at the counter output is quite low (around 1 Hz). Therefore, the interpolation filter can be implemented as a simple zero-order-hold, which is sufficient to notch out signal images.

The oversampling ratio of the 1-bit first-order digital ΔΣ modulator is chosen to be 8192 in order to push the quantization noise to a high enough frequency of 8192 kHz, which is then suppressed by the succeeding LPF. The quantizer outputs the most-significant-bit (MSB) of the register. The multiplier of 512 is realized by wiring the 1-bit modulator output to the tenth bit from the least-significant-bit (LSB) of a subtractor [9]. In this way, the modulator changes the 10-bit signal from the counter into a 1-bit digital signal which contains the gain error correction signal and the spectrally shaped quantization noise. A 2nd-order RC low-pass filter with a cut-off frequency of 2 kHz is enough to suppress the shaped quantization noise. The filtered output signal feeds to G_{m6} and generates two differential currents which compensate the mismatch of G_{m3} and G_{m4}. This dither signal is

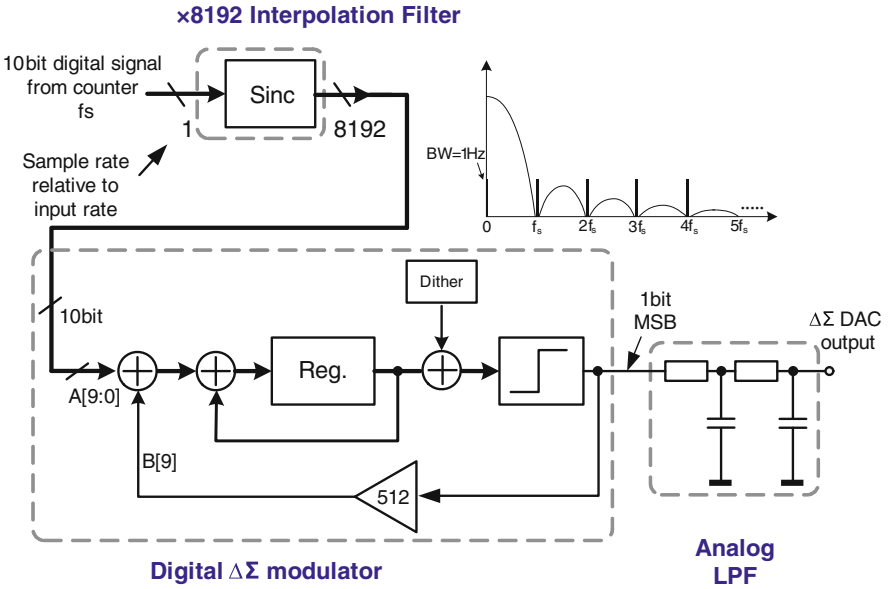

Fig. 5.19 Implementation of 1-bit first-order ΔΣ DAC

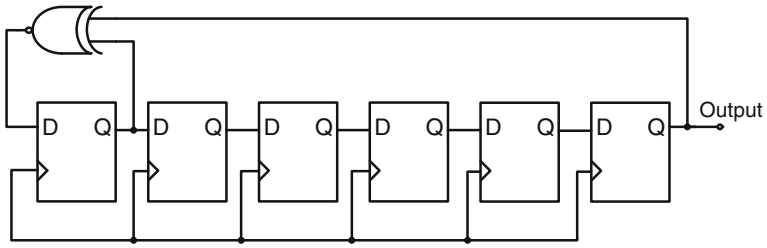

Fig. 5.20 Pseudo-random generator for the dither signal

generated by a 6-bit pseudo-random generator, as illustrated in Fig. 5.20. It consists of six D-flipflops and an XOR inverter gate.

5.7.2.2 Polarity Control Quantizer Q_2 in Digitally-Assisted GERL

Figure 5.21 shows the block diagram of the three-level quantizer. To reduce the kick-back effect and offset of the quantizer, a pre-amplifier with MOS input is implemented preceding the quantizer. Its schematic diagram is shown in Fig. 5.22. The reference voltages V_{ref+} and V_{ref-} interchange with each other once during each comparison cycle to generate two threshold levels ±200 mV, as shown in Fig. 5.22.

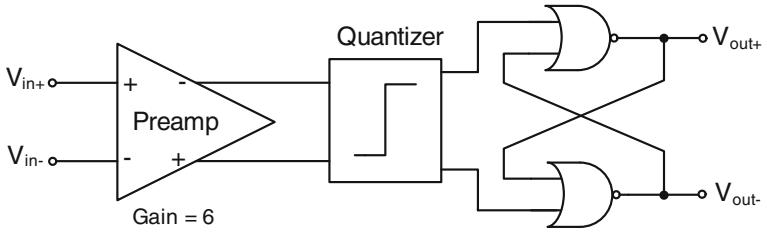

Fig. 5.21 Block diagram of the three level quantizer

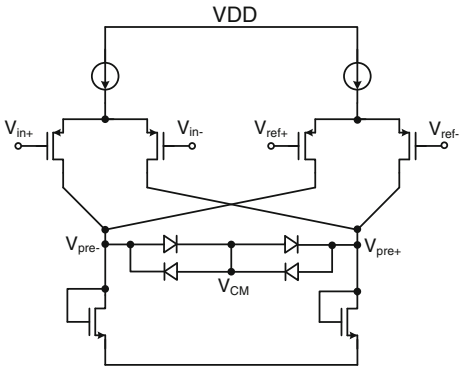

Fig. 5.22 Schematic diagram of the preamp preceding the quantizer ($\mathbf{V}_{ref+} - \mathbf{V}_{ref-} = \pm 200$ mV)

The MOS input of the preamplifier offers high input impedance and a low input bias current. The switching transitions in the quantizer thus have negligible effect on the amplifier output. To reduce the recovery time of the preamp, four clamping diodes are connected there. The resulting output swing of this preamp is limited to the V_{GS} of two diodes, which is about 1.4 V.

5.8 Measurement Results

The CFIA with the ORL and the GERL was implemented in a 0.7 μm CMOS process with low-threshold transistors, linear capacitors and high-resistivity poly resistors. The 5 mm^2 chip micrograph is shown in Fig. 5.23. Both the analog and digitally-assisted GERLs were implemented. For flexibility, the first-order ΔΣ DAC and the counter were implemented in an FPGA. The CFIA with the analog GERL only consumes a 290 μA supply current (NEF = 11.2) and the CFIA with the digitally-assisted GERL consumes a 295 μA supply current, including that which is consumed in the digital circuitry. The ORL and the GERL draw 14 % and 10 % of the total supply current, respectively. Measurements on 30 samples show that the CFIA achieves 3 μV offset and 15 nV/°C offset drift.

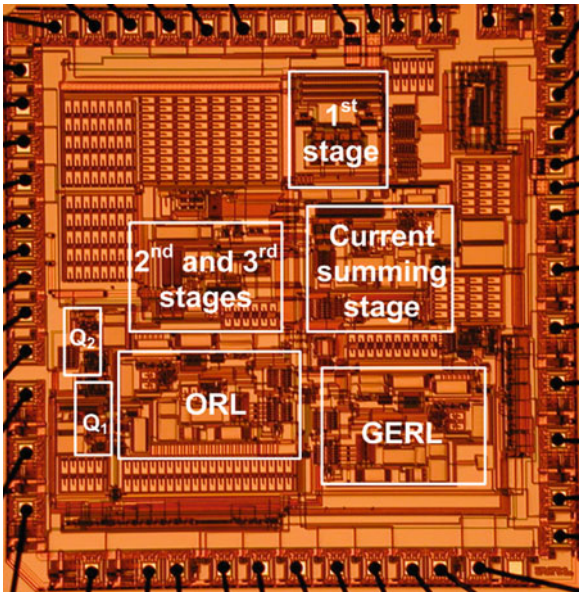

Fig. 5.23 Chip micrograph of the CFIA with GERL

5.8.1 Noise

In the digitally-assisted GERL, the quantization noise from the 1-bit ΔΣ DAC is sufficiently suppressed by the second-order RC LPF, and therefore it does not contribute to the input-referred noise PSD. Figure 5.24 depicts the measured noise PSD of the amplifier with the analog GERL and digitally-assisted GERL, respectively, showing that they achieve the same noise level of 17 nV/$\sqrt{}$Hz.

5.8.2 Output Ripple Measurement

Figure 5.25 depicts the output ripple measurement of (a) DEM only; (b) DEM + analog GERL; and (c) DEM + digital GERL. All the measurements are done with the amplifier configured at a gain of 100 and the ORL "on". As seen from the results, the ORL and the GERL indeed can work independently with each other. To verify that the digitally-assisted GERL provides sufficient dynamic range to suppress the DEM ripple, a relatively large input signal of 30 mV is fed to the amplifier. The analog GERL suppresses the DEM ripple by more than 40 dB from 4.6 mV down to 37 μV, which varies at most 0.52 μV/°C over temperature. The digitally-assisted GERL suppresses the output DEM ripple below 47 μV. Furthermore, it suppresses the second harmonic of f_{DEM} down to 18 μV, which is 2 × smaller than that in the analog GERL (35 μV). This confirms the analysis described in Sect. 5.7.2. The residual chopper ripple amplitude is 32 μV, close to the residual DEM ripple.

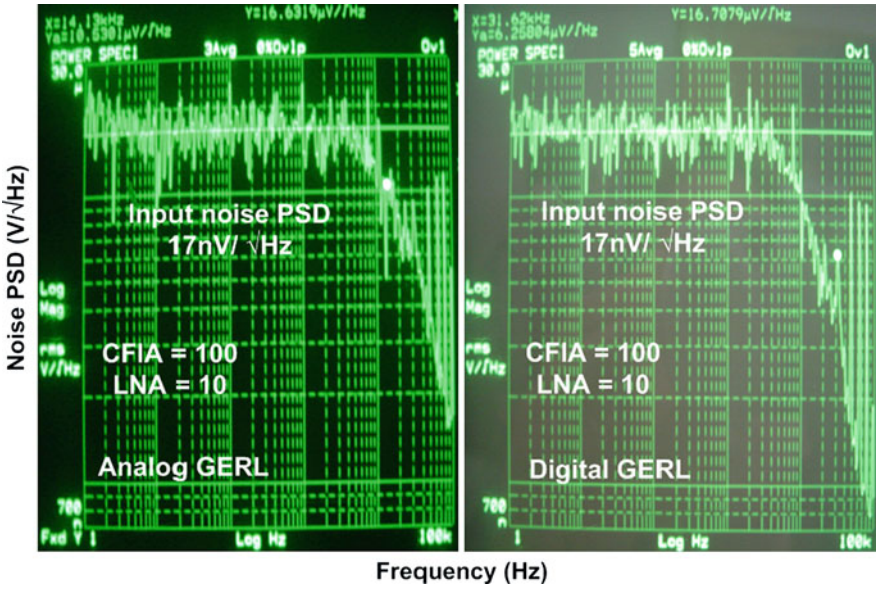

Fig. 5.24 Output noise spectrum of the CFIA with analog and digitally-assisted GERL (from 1 Hz to 100 kHz)

Figure 5.26 shows the output ripple measurement with an input CMV at 1.25 V and a feedback CMV at 2.5 V: (a) DEM only; (b) DEM + analog GERL; (c) DEM + digital GERL. Due to the different CM voltages, the residual DEM ripple at f_{DEM} increases to 60 μV, and ripple at other harmonics also increases a bit. The CM dependence of the input stages results in some interaction between the ORL and the GERL, thus the residual chopper ripple increases to about 90 μV. However, at a gain of 100, the total input-referred ripple (∼2 μV) is still low enough for most applications.

5.8.3 INL

Figure 5.27 shows the typical integrated nonlinearity INLmeasurement results in three cases: (a) without DEM; (b) with only DEM; and (c) DEM + GERL. The initial INL of the amplifier is 25 ppm. The use of DEM improves the amplifier's linearity from 25 ppm to 6 ppm (at a gain of 100). This is because that the use of DEM shifts the transfer functions of $G_{m3,avg}$ and $G_{m4,avg}$ closer to each other (Fig. 5.9c). Thus, their nonlinearity improves with DEM. Turning on the GERL further reduces the INL to 4 ppm (Fig. 5.27). This is because that the GERL nulls the mismatch to zero, after which the transfer functions of the two G_m stages become completely aligned with each other (Fig. 5.9d). As a result, the linearity improves further. The same explanation goes for the effects of DEM and the

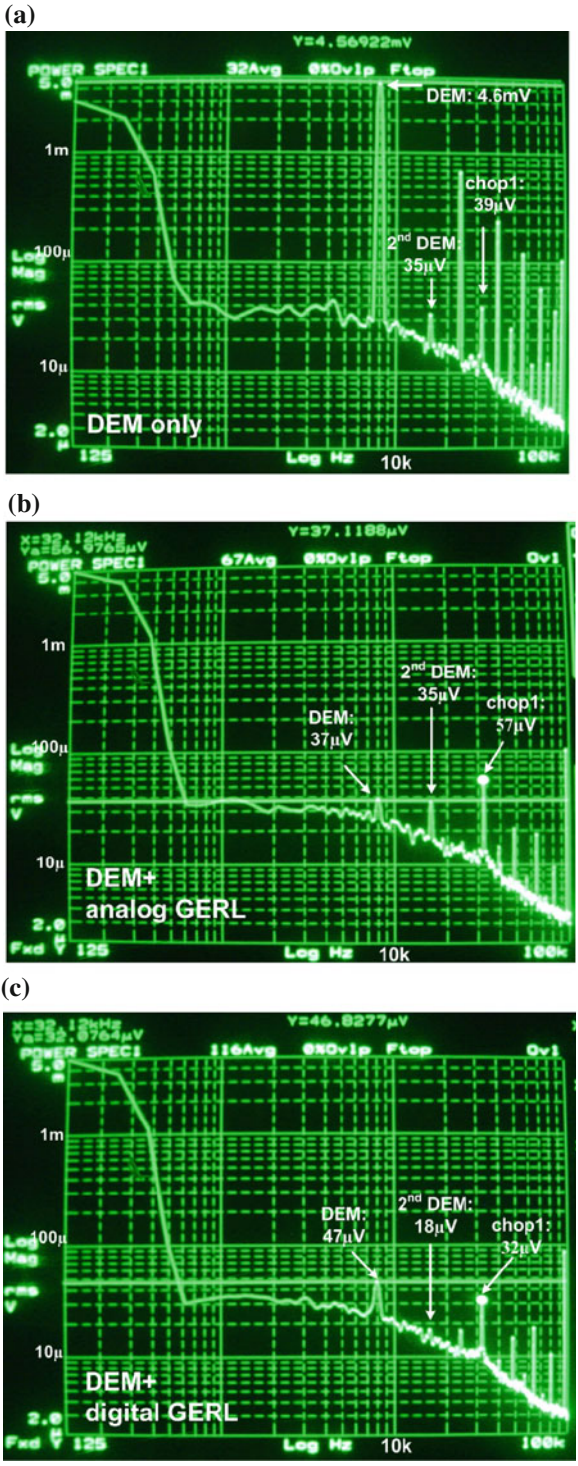

Fig. 5.25 Output ripple measurement with GERL "on" and "off" (at a gain of 100, $f_{\mathrm{DEM}} = f_{\mathrm{chop1}}/4 = 8$ kHz). **a** DEM only; **b** DEM + analog GERL; **c** DEM + digital GERL

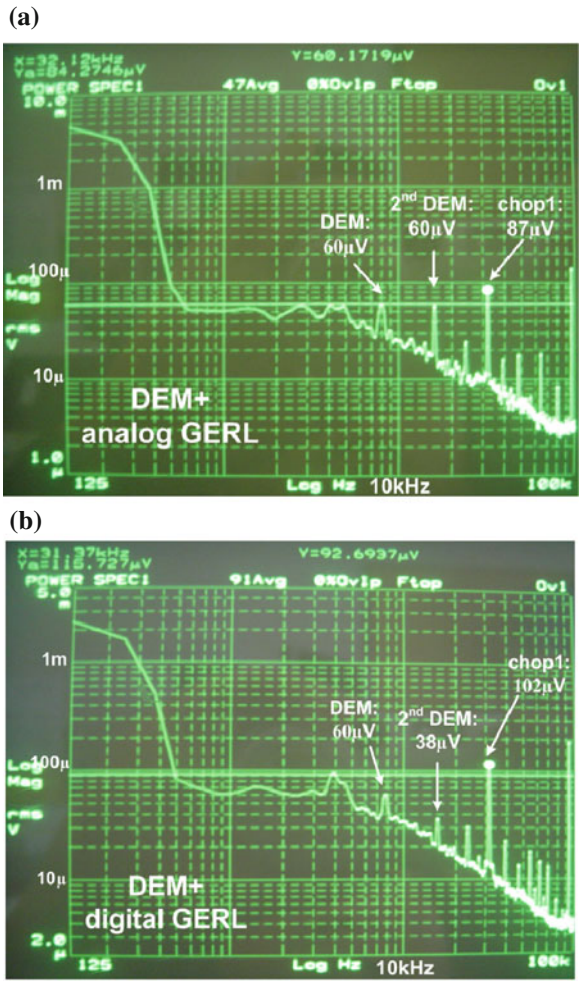

Fig. 5.26 Output ripple measurement with GERL and input CM at 1.25 V and feedback CM at 2.5 V (at a gain of 100, $f_{DEM} = f_{chop1}/4 = 8$ kHz). **a** DEM + analog GERL; **b** DEM + digital GERL

GERL on gain accuracy and gain drift. Since the use of DEM and GERL improves INL, the input range of the CFIA also increases. Without DEM, the INL is 25 ppm within ±30 mV. Turning on the DEM and GERL, the input range extends to ±120 mV with an INL of 10 ppm.

5.8.4 Gain Accuracy and Gain Drift

The use of DEM reduces the CFIA's worst case gain error from 0.6 % to 0.01 % when G_{m3} and G_{m4} are at the same CM voltage of 2.5 V. Under these conditions, the use of DEM reduces the maximum gain drift from 300 ppm/°C to 9 ppm/ °C (Fig. 5.28) (11

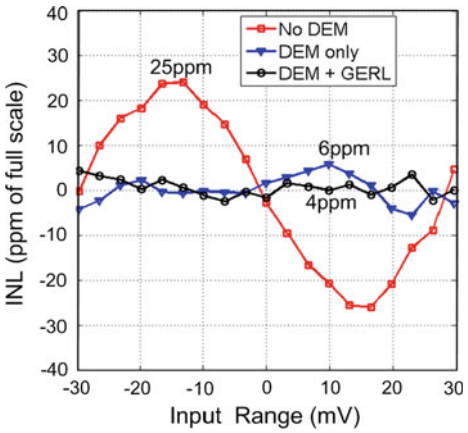

Fig. 5.27 Measured INL of the CFIA. **a** No DEM; **b** DEM only; and **c** DEM + GERL

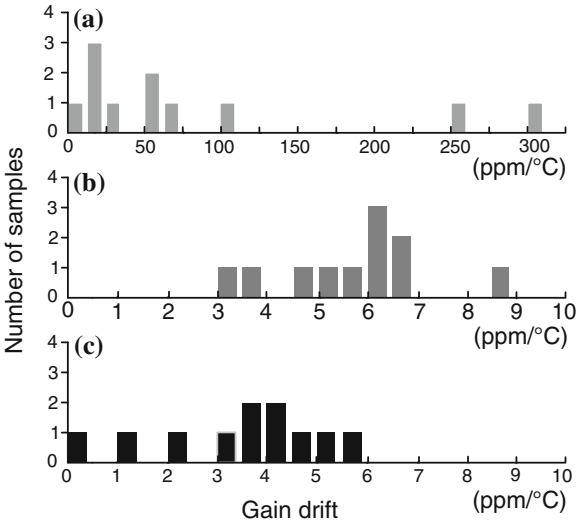

Fig. 5.28 Measured gain drift histogram of the CFIA. **a** No DEM; **b** DEM only (output ripple present); and **c** DEM + GERL)

samples). Turning on the GERL reduces it even further, to 6 ppm/°C (11 samples). Due to the limited CMRR of the input stages, the gain error increases to 0.06 % when the input of G_{m3} is at 0 V, while the input of G_{m3} is at 2.5 V. Other measurement results include a typical CMRR of 127 dB and a typical PSRR of 130 dB.

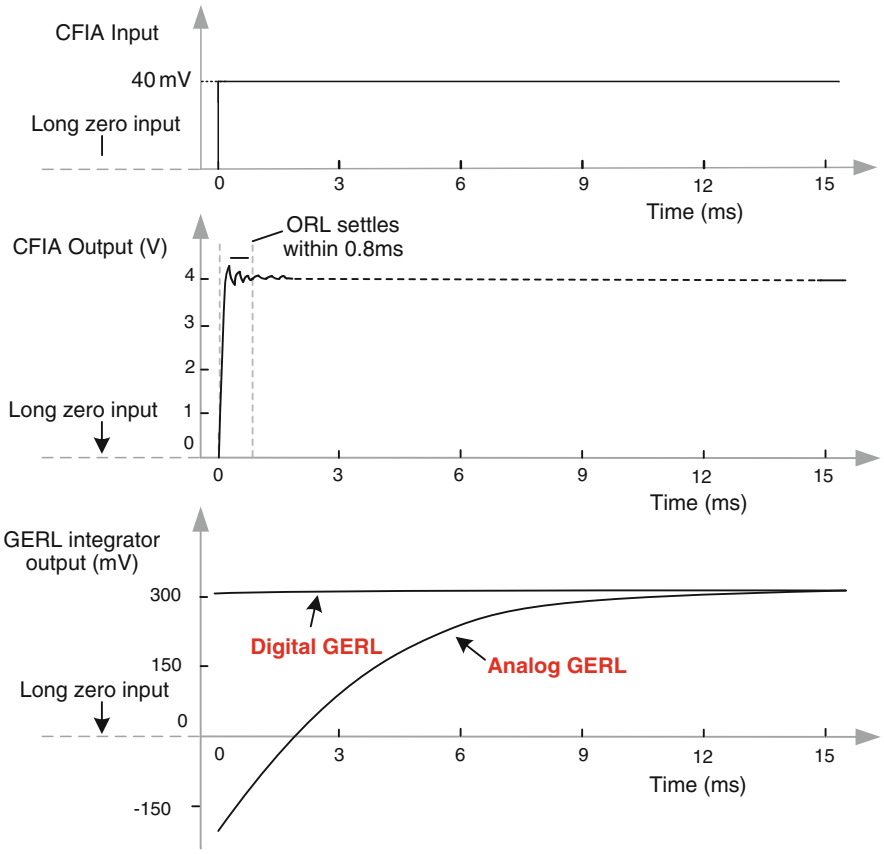

Fig. 5.29 Settling behavior of the amplifier when a step input re-appears after a long zero input

5.8.5 Settling Behavior of Analog GERL and Digitally-Assisted GERL

Figure 5.29 shows the measured settling behavior of the CFIA with a 40 mV input step appears after a long period with zero input. It can be seen that the integrator output of the analog GERL settles in an exponential manner. In contrast, the state of the digitally-assisted GERL remains stable, since after start-up, it stores the mismatch in the digital domain. Therefore, it behaves as a static mismatch compensation loop for zero input. These results confirm the analysis in Sects. 5.3.3 and 5.4.

Table 5.1 Performance summary and comparison with state-of-the-art

	This work [6]	Witte [4]	Pertijs [3]	Fan [10]	Sakunia [5]
Year	2011	2009	2010	2010	2011
Supply current (μA)	290 (analog GERL)	850	1700	143	480
Input noise PSD ($V/\sqrt{Hz}$)	17n	136n	27n	21n	28n
1/*f* noise corner (Hz)	1 m	–	–	1	–
CMRR (dB)	127	130	142	137	122
PSRR (dB)	130	114	138	120	128
Gain error (Absolute)	Dif CM: 0.06 % (Untrimmed)	0.1 % (Trimmed)	0.1 % (Untrimmed)	0.53 % (Untrimmed)	Dif CM: 0.04 % (Trimmed)
Gain drift (ppm/°C)	3 (typ) 6 (max)	–	3 (typ) 16 (max)	–	2.1 (typ)
Offset (μV)	<3	<5	<2	<2	<4 μV
Offset drift (nV/°C)	12	–	3	–	4 (typ)
GBW (kHz)	800 (stable when gain >20)	640	800	900	–
INL	4 ppm	–	–	–	–
Die area (mm^2)	5	2.5	2.5	1.8	1.48
GBW/I_{supply}	2.8	0.8	0.5	6.3	–
NEF [11]	11.2 (analog GERL)	152.9	43	9.6	24

5.9 Benchmark and Conclusions

This chapter addresses the major disadvantage of the current-feedback instrumentation amplifier (CFIA): its limited gain accuracy, which is due to the mismatch between its input and feedback transconductors. To reduce this mismatch, dynamic element matching (DEM) is applied to modulate the mismatch to the DEM frequency. Since DEM ensures good gain accuracy, the input and feedback transconductors can be implemented with simple differential pairs, thus resulting in an improved power efficiency compared to CFIAs with resistor-degenerated stages [3, 4]. To suppress the *signal-dependent* DEM ripple, a gain error reduction loop (GERL) is proposed to continuously cancel the G_m mismatch, thus eliminating the need for trimming. The residual DEM ripple then becomes *signal-independent*. This feature makes the GERL more attractive than trimming [5], because trimming can not eliminate the signal dependency in the DEM ripple. Moreover, trimming can not compensate for temperature drift. The use of DEM and the GERL ensures that the transfer functions of the input and feedback transconductances are aligned, resulting in an improved performance in terms of gain error, gain drift and linearity.

Since the loop gain of the GERL is signal-dependent and is zero for zero input, the analog GERL needs to resettle whenever an input step reappears after long zero input. To avoid resettling, a digitally-assisted GERL is implemented to store the mismatch in the digital domain and compared with the analog approach.

During the DEM transitions, the abruptly changing CM voltages cause CM current spikes in the input stages. To avoid overloading, the back-gates of the input and feedback transconductors are actively class-AB boot-strapped, so as to bypass the spikes to the supply rails.

In summary, the advantages of DEM combined with a GERL compared to other gain error reduction techniques are:

Applying DEM to two simple differential pairs ➔ good power efficiency
Dynamic cancellation loop ➔ no need for trimming
After suppression by the GERL, the DEM ripple becomes signal-independent

The measured performance of the CFIA is summarized in Table 5.1 and compared with the state-of-the-art [3, 4, 10]. Without trimming, it achieves a gain error of less than 0.06 % and a maximum gain drift of 6 ppm/°C in a power efficient manner (NEF [11] = 11.2). Compared to a CFIA with similar gain accuracy but which uses resistor-degenerated stages [3], this represents a 4 × improvement in power efficiency, which is equivalent to a 16-fold improvement in power when the same noise level is achieved [11]. However, it should be noted that the CFIA with resistor-degeneration stage has a wider input range (about ±500 mV compared to ±120 mV). Compared to a CFIA with similar power efficiency [10], this represents a 9 × improvement in gain accuracy. Compared to a ping-pong-pang CFIA, it achieves comparable gain error without

trimming and with 2 × improved power efficiency. These measurement results confirm that the combination of DEM and a GERL is a power-efficient manner to improve the gain accuracy, gain drift and linearity of a CFIA.

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Chapter 6
Read-Out Integrated Circuits

This chapter presents the design and implementation of a read-out IC that is intended for interfacing thermistor bridge, thermocouple, strain gauge and Hall sensors. The read-out IC consists of a current-feedback instrumentation amplifier (CFIA) and an analog-to-digital converter (ADC). The CFIA provides high input impedance for bridge read-out and also relaxes the ADC's noise and offset requirements. The ADC converts the amplified sensor signal into a robust digital output [1, 2].

The CFIA employs a topology that has been discussed in Chap. 4, thus this chapter will mainly focus on the design of the ADC and the system-level collaboration between the CFIA and the ADC. Firstly, the requirements and the architecture design of the ADC are discussed. This is followed by the system-level collaboration between the CFIA and the ADC. System-level chopping is employed to chop the complete read-out chain. The resulting modulated offset is then averaged out in the digital decimation filter during multiple conversions. Furthermore, the read-out IC explores the power of digital signal processing succeeding the ADC to help the CFIA to improve its gain accuracy and gain drift. Finally, the detailed circuit implementation and the measurement results are presented. Compared to previous work, our read-out IC achieves state-of-the-art performance in terms of offset and drift.

6.1 ADC Requirements

Figure 6.1 shows a simplified block diagram of a bridge read-out system with the proposed read-out IC. It is designed to meet the specifications of typical bridge sensors and thermocouples (see Sect. 1.6).

As discussed in Sect. 4.2, the CFIA consists of three gain stages, as shown in Fig. 6.2. The closed-loop gain is defined by precision external resistors. The input

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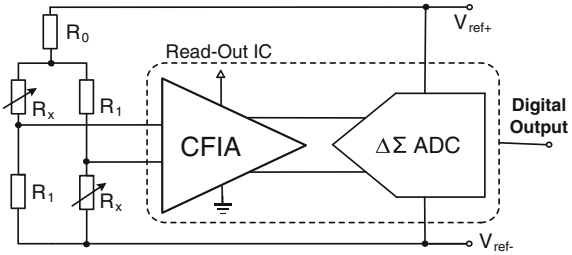


Fig. 6.1 Simplified block diagram of a bridge-readout system with the read-out IC

and intermediate stages are both chopped, thus providing sufficient gain to suppress the 1/*f* noise of the unchopped output stage down to 1 mHz [3]. The input referred noise PSD of the CFIA is 15nV/$\sqrt{}$Hz. The 1/*f* noise corner frequency of unchopped CFIA is around 10 kHz, and thus the chopping frequency is chosen to be 30 kHz, which is well above the corner frequency to remove 1/*f* noise.

To achieve a better power efficiency, the CFIA should dominate the noise, offset and gain accuracy of the overall read-out IC [4], and the ADC is designed to maintain the CFIA's performance. Based on the detailed specifications of the sensors and the read-out IC (Table 1.3), the requirements of the ADC are derived.

Bandwidth and Resolution

The output of the CFIA is digitized by an incremental ΔΣ ADC consisting of a ΔΣ modulator and a decimation filter. It is well known that ΔΣ ADCs provide high resolution with less accurate analog building blocks due to noise shaping and oversampling [5]. Here, to maintain the SNR of the CFIA, the target resolution of the ΔΣ ADC is 21-bit with a conversion time less than 0.2 s (BW = 5 Hz). The reference voltage of the ΔΣ ADC is set to be 5 V with 4 V input full scale, which corresponds to a noise density of 600nV/$\sqrt{}$Hz in 5 Hz bandwidth. Given the CFIA's gain of 100, the input referred noise density of the ΔΣ ADC is 6nV/$\sqrt{}$Hz, which is still lower than that of the CFIA (16nV/$\sqrt{}$Hz), as shown in Fig. 6.3.

Compared to the continuous-time (CT) counterpart, switched-capacitor (SC) ΔΣ ADC is chosen here because of its high accuracy [5, 6]. The CT ΔΣ ADC uses resistors or G_m stages to convert the input voltage to a current. Its gain error and nonlinearity are usually determined by the resistor- or transconductor-matching. While in the SC ΔΣ modulator, its gain error and nonlinearity are determined by capacitor-matching, with careful layout, which has superior matching over resistors or transconductors.

1/f Noise Corner

As described in Chap. 4, the CFIA already achieves a 1 mHz 1/*f* noise corner with multi-stage chopping. The ADC also aims to achieve a 1 mHz 1/*f* noise corner so that even when the closed-loop gain of the CFIA reduces in some applications, the read-out IC can still maintain the 1 mHz 1/*f* noise corner.

Gain Error

The gain accuracy of the ADC should be much better than the CFIA itself, and thus the gain accuracy of the read-out IC is not degraded by the ADC. The ADC

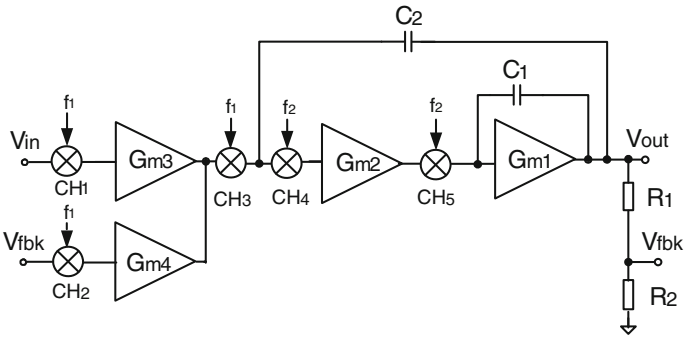


Fig. 6.2 Simplified block diagram of CFIA with the input and intermediate stages chopped

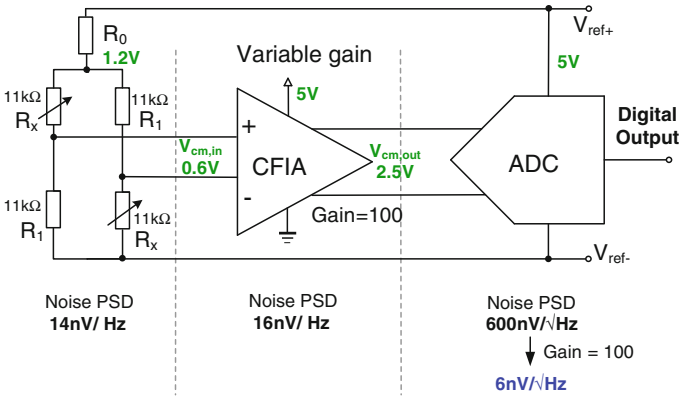


Fig. 6.3 Noise budget of the total read-out IC

aims to achieve a gain error of less than 20 ppm. The bridge and the ADC are connected in a ratio-metric structure and thus the accuracy requirement of the ADC's reference is much relaxed.

Offset

The gain of the CFIA suppresses the offset of the ADC when input-referred. To achieve a 1 μV input-referred offset with the CFIA at a gain of 100, the input-referred offset of the ADC should be less than 100 μV. Table 6.1 summarizes the specifications of the ADC.

Table 6.1 Specification summary of the 21-bit SC ΔΣ modulator

Topology	Second-order
Conversion time	<0.2 s
Output noise	1.34 μV
Noise PSD	600nV/$\sqrt{}$Hz
Input range	±4 V
Reference voltage	5 V
Thermal noise limited SNR	129 dB
Quantization noise limited SNR	129 dB
Number of bits	21bit
Offset	<100 μV
1/*f* noise corner @ 600nV/$\sqrt{}$Hz	1 mHz
Gain error	<20 ppm
Supple current	<100 μA

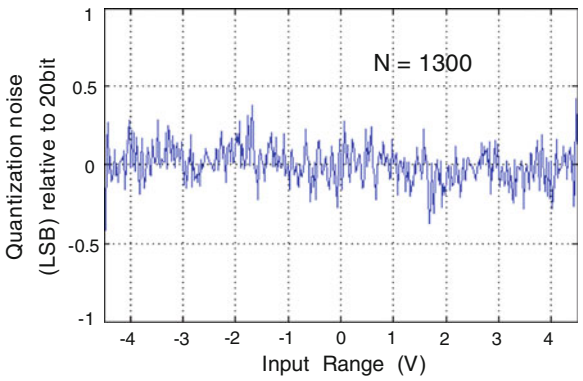


Fig. 6.4 Simulated quantization noise over the input range

6.2 Architecture Design of the ADC

6.2.1 Modulator Topology

As discussed above, the ΔΣ ADC aims to achieve a quantization noise limited resolution of 21-bit (129 dB) within a 0.2 s conversion time. A 1-bit quantizer is chosen because of its inherent linearity. As will be described in Sect. 6.3.2, the read-out IC is designed in such a way that one decimated digital output is obtained with four conversions. To achieve 21-bit resolution in the ADC, the resolution of each ADC conversion should be 20-bit. To achieve such a high resolution, a first-order incremental ΔΣ modulator requires clock cycles larger than 32768 per conversion [5], corresponding to a sampling frequency f_S of 650 kHz. Such a high sampling frequency implies undesirable high power consumption. Second, the first-order structure generates periodic sequences, so called limited cycles, for DC input signals. This issue can become even more severe due to finite DC gain of the opamp, which causes loss in the integrator and introduces dead-band that could lock into a limit cycle.

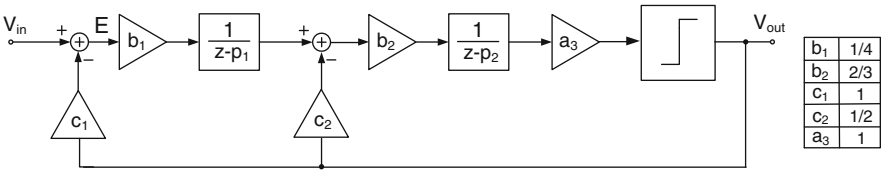


Fig. 6.5 Block diagram of a second-order ΔΣ modulator with feedback (FB) topology

To reduce the required clock frequency and errors due to dead band, a second-order ΔΣ modulator is preferable. For a second-order incremental modulator, it needs 1300 clock cycles per conversion [5]. This is confirmed by Matlab simulation result shown in Fig. 6.4, showing that the quantization noise is less than ±0.5LSB of 20 bit within the entire input range. For one decimated output, four conversions means 5200 clock cycles. To achieve a conversion time of less than 0.2 s, the minimum sampling frequency is 26 kHz. To leave some margin, a 30 kHz sampling frequency is chosen here since it is the same as the chopping frequency of the CFIA and furthermore, the ADC and CFIA can be easily synchronized to each other.

Although with a third-order modulator, a sampling frequency f_S of 3.2 kHz is sufficient to achieve a resolution of 20 bit (OSR = 160), there are some other trade-offs that need to be considered. The chopping frequency of the input stage in the CFIA has to be higher than the 1/*f* noise corner of 10 kHz to remove the 1/*f* noise. With an ADC's sampling frequency f_S of 3.2 kHz, the under-sampling of the chopper ripple (>10 kHz) is more severe than that with f_S of 30 kHz. Although a high sampling frequency f_S reduces the under-sampling errors, it would consume more power to meet the settling requirements. Moreover, the increased power in the ADC does not improve the resolution of the read-out IC, since the noise level of the CFIA dominates. In summary, a third-order modulator is not an optimum solution for our applications.

One possible topology for implementing the ΔΣ modulator is using the feedback (FB) topology shown in Fig. 6.5. In this topology, the entire output signal, consisting of both the input signal and the quantization noise is fed back to the input of each integrators. Therefore, the first integrator output must provide a strong compensation signal. This means that the error signal fed to the first integrator is also relatively large, containing a strong signal component. The opamp in the first integrator thus needs to consume large power to meet the stringent linearity requirement.

To reduce the signal swing and ensure reduced swing with an average of zero at the first integrator output, a feed-forward path a_2 can be applied [7] (Fig. 6.6). This results in a hybrid feed-forward and feedback (hybrid-FF–FB) topology.

An alternative topology is the input feed-forward (FF) topology [8] shown in Fig. 6.7. A feed-forward branch (a_2) is applied from the first integrator output to the second integrator output to ensure the stability of the modulator. The feed-forward path (a_1) is inserted to reduce latency in the feedback loop from the input through a_1,

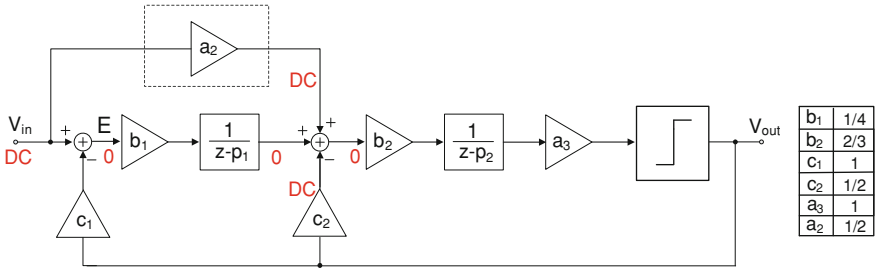


Fig. 6.6 Block diagram of a second-order ΔΣ modulator with hybrid feed-forward and feedback (hybrid-FF–FB) topology

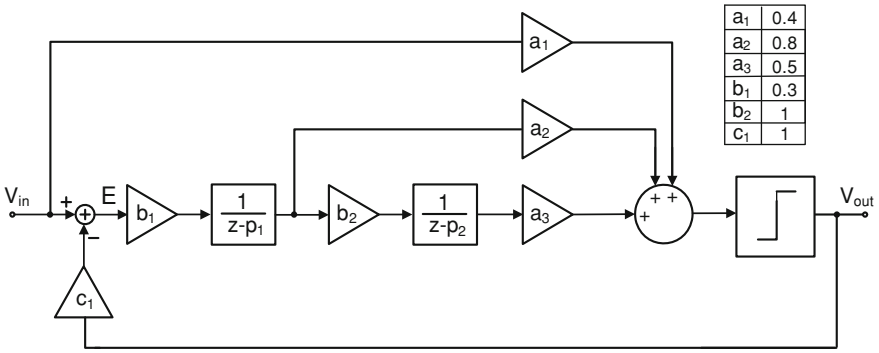


Fig. 6.7 Block diagram of a second-order ΔΣ modulator with input feed-forward (FF) topology

the quantizer and c_1. The coefficients are chosen in such a way that the input signal and the average of the bitstream feedback signal are well compensated, thus the resulting error signal *E* only contains quantization noise, relaxing the linearity and slew requirements of the opamp in the first integrator.

The output swings of the first and second integrators in the above three topologies are simulated as a function of the DC input levels (Fig. 6.8). The coefficients of these three topologies (indicated in the pictures) are chosen for the same noise transfer function (NTF) and already optimized to reduce swings at integrators' output.

It can be seen from Fig. 6.8a that the output swing of the first integrator in the feedback topology significantly increases when the input signal exceeds 0.6 V_{ref}, while those in the feed-forward and hybrid-FB–FF topologies remain below 1.1 V. As seen from Fig. 6.8b, the output swing of the second integrator in the hybrid-FB–FF topology is much larger than that in the FF topology. Since the FF

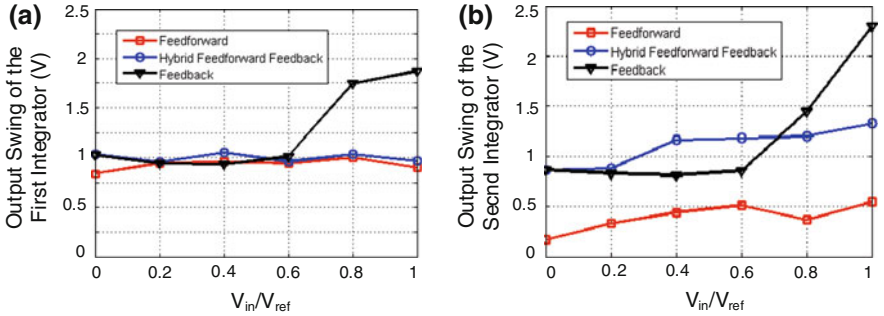


Fig. 6.8 Simulated maximum peak value of the integrator output swing as a function of the DC input levels

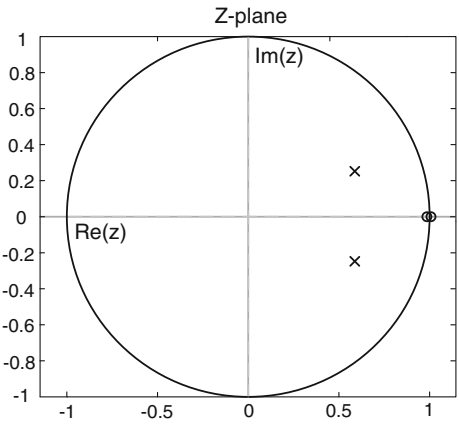


Fig. 6.9 Pole-zero plot of the NTF

topology exhibits the smallest output swings within the whole input range, it is employed in this work.

STF and NTF of the ΔΣ Modulator

From the feed-forward topology in Fig. 6.7, the signal transfer function (STF) and the noise transfer function (NTF) of the input feed-forward topology can be calculated as

$$STF = \frac{1}{c_1} \tag{6.1}$$

$$NTF = \frac{1}{1 + c_1 L(z)} = \frac{(z - p_1)(z - p_2)}{(z - p_1)(z - p_2) + a_2 b_1 c_1 (z - p_2) + a_3 b_2 b_1 c_1 (z - p_1)} \tag{6.2}$$

Table 6.2 Coefficients for the second-order ΔΣ modulator in Fig. 6.7

b_1	0.33
b_2	1
a_1	0.4
a_2	0.8
a_3	0.5
c_1	1

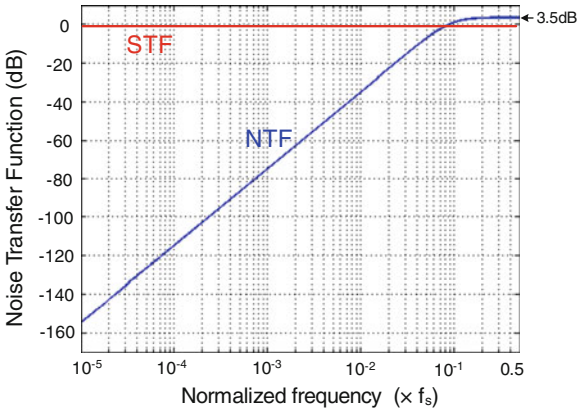


Fig. 6.10 The STF and NTF plot of the ΔΣ modulator

It can be seen from (6.2) that the two poles of p_1 and p_2 in the loop-gain of the modulator correspond to the two zeros at DC in the NTF. Since the bandwidth of the modulator is quite narrow (0–5 Hz) and close to DC, the two zeros are chosen to be at DC to sufficiently suppress the quantization noise near DC, as shown in the pole-zero plot in Fig. 6.9. Thus, assuming infinite DC gain,

$$p_1 = p_2 = 1. \tag{6.3}$$

To ensure stable second-order noise shaping and reasonable swings at the integrators' output, Matlab simulations were done to optimize the coefficients of the modulator to reduce swings at each integrator output and meanwhile obtain the targeted SNR. The results are shown in Table 6.2. Figure 6.10 depicts the ideal NTF and STF of the ΔΣ modulator with infinite DC gain. For stability purposes, the out-of-band gain of the NTF near half of the sampling frequency is chosen to be a rule of thumb value: 1.5 (3.5 dB) [5].

Figure 6.11 shows the FFT plot of the bit-stream of the modulator. It achieves an SNR of 140 dB within a 5 Hz bandwidth with a 4 V DC input referenced to 5 V (Fig. 6.11a). The FFT plot of the Matlab simulation with a sine input of 4 V at 0.2 Hz is shown in Fig. 6.11b.

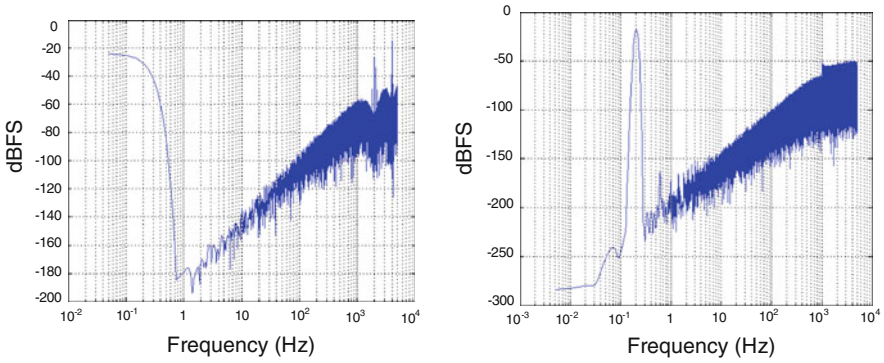


Fig. 6.11 **a** The noise spectrum of the ΔΣ modulator with 4 V DC input 4 V (reference to 5 V). **b** The noise spectrum of the ΔΣ modulator with 4 V Sine input (reference to 5 V)

6.2.2 Non-Idealities in the ΔΣ Modulator

The previous section described the order, architecture, sampling frequency and coefficients of the ΔΣ modulator, which define its quantization noise. This section discusses other non-idealities of the SC ΔΣ modulator, such as kT/C noise finite DC gain, offset, 1/*f* noise, and charge injection.

kT/C Noise

In a switched-capacitor ΔΣ ADC, its thermal noise is mainly limited by kT/C noise. The ADC's input-referred noise density was designed to be 600nV/$\sqrt{}$Hz, corresponding to a noise voltage V_n of 1.34 μV over a 5 Hz bandwidth. The full input range is ±4 V, thus the corresponding SNR due to thermal noise is 129 dB. The *OSR* is 3000 with a sampling frequency of 30 kHz. To leave some margin, the kT/C noise is designed to be 1 μV, determined by the sampling capacitor as given by

$$\frac{2kT}{C_S \times OSR} = V_n^2 = (1\mu V)^2 \tag{6.4}$$

The resulting sampling capacitor C_S is 3 pF. The factor of two accounts for the two input sampling capacitors due to the differential topology.

Leakage

In a first-order modulator, the integrator leakage p limits its effective number of bits (ENOB). Since the DC gain A_{dc} determines the leakage

$$A_{DC} = \frac{1}{1-p} \tag{6.5}$$

So,

$$p = 1 - \frac{1}{A_{DC}} \tag{6.6}$$

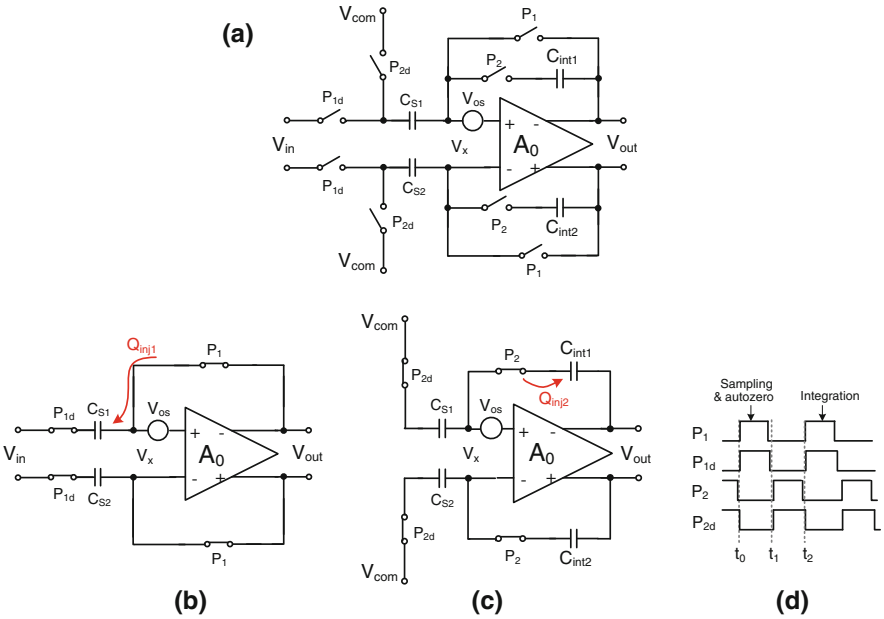


Fig. 6.12 The operation of an auto-zeroed switched-capacitor integrator in two phases. **a** Auto-zeroed Integrator, **b** auto-zero phase $P_{1,}$ **c** integration phase $P_{2,}$ **d** timing diagram

The width of the dead-band Δx in the modulator's DC characteristic normalized to its reference is given by [9]

$$\Delta x_{\max} = \frac{1-p}{1+p} \approx \frac{1-p}{2} \tag{6.7}$$

Substituting (6.6) into (6.7), the maximum width of the dead-band is given by

$$\Delta x_{\max} \sim \frac{1}{2A_{DC}} \tag{6.8}$$

It can be seen from (6.8) that in a first-order modulator, the DC gain of the first integrator limits the ENOB. A similar phenomenon occurs in a second-order modulator [5]. To obtain an ENOB of 21bits, a combined DC gain of cascaded integrators in the order of 123 dB is required, which can be easily achieved by two integrators. The first and second integrators with a DC gain of more than 90 dB and 60 dB, respectively, should be sufficient to suppress the error caused by the integrator leakage.

Offset and 1/f Noise Suppression

The ADC aims to achieve the same $1/f$ noise corner as the CFIA at 1 mHz. This is realized by auto-zeroing the first integrator [10] as shown in Fig. 6.12. In the auto-zeroing phase, the finite DC gain A_0 of the opamp in the first integrator results

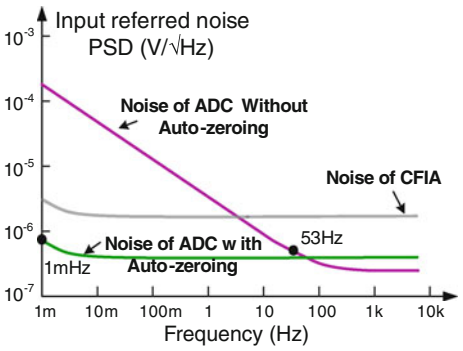


Fig. 6.13 Simulated input-referred noise spectrum of the 1st integrator with and without auto-zeroing

in a non-zero overdrive voltage at the input of the opamp, so V_x is not exactly equal to V_{os}. At the end of phase P_1, V_x equals

$$V_x(t_1) = A_0(V_{os} - V_x(t_1)) \Rightarrow V_x(t_1) = \frac{A_0}{1 + A_0} V_{os} \tag{6.9}$$

While at the end of phase P_2, it equals

$$V_x(t_2) = V_{os} - \frac{V_{\text{int}}(t_2)}{A_0} \tag{6.10}$$

Using (6.9) and (6.10), the integrated charge in every period is given by

$$Q = C_S\{V_{in}(t_1) + (V_x(t_2) - V_x(t_1))\} = C_S\left\{V_{in}(t_1) + \frac{V_{OS}}{1 + A_0} - \frac{V_{\text{int}}(t_2)}{A_0}\right\} \tag{6.11}$$

Due to the subtraction $V_x(t_2) - V_x(t_1)$ in (6.11), the auto-zeroing technique suppresses the offset and 1/*f* noise and their suppression ratio is determined by the finite DC gain A_0 of the opamp. To obtain a 1 mHz 1/*f* noise corner, simulation shows that the opamp in the first integrator must have a DC gain of 160 dB. This was achieved by using a two-stage Miller-compensated opamp with a gain-boosted first stage and a class-A second stage.

Figure 6.13 shows the input-referred noise spectrum of the first integrator with and without auto-zeroing as simulated using the Periodic Steady State (PSS) and Periodic Noise (PNOISE) tools of Spectre RF [11]. Without auto-zeroing, the first integrator exhibits a 1/*f* noise corner of 53 Hz and a noise PSD at 600nV/$\sqrt{}$Hz. With auto-zeroing, the 1/*f* noise corner is shifted down to 1 mHz with an increased noise floor of 600nV/$\sqrt{}$Hz caused by the double-sampling associated with auto-zeroing. However, the overall noise level of read-out IC is still dominated by the CFIA.

Charge Injection and Clock Feed-Through

With 160 dB DC gain in the first integrator, the integrator leakage and the residual offset due to finite DC gain, expressed by the third and second term in (6.11), becomes negligible. The residual offset is then mainly due to charge injection mismatch.

The auto-zeroed integrator uses a bottom-plate sampling scheme, as shown in Fig. 6.12. A clocking scheme with delayed falling edges [5] is used to limit the charge-injection error to that of only four switches: switches controlled by P_1, P_2. The switches driven by P_2, P_1 open first and inject some charge Q_{inj1} and Q_{inj2} into C_S and C_{int}, respectively. Note that since these switches are connected to the virtual ground of the amplifier, their charge injection can be considered as constant and signal-independent.

When the switches driven by P_{1d} and P_{2d} are open, the capacitors C_{s1} and C_{s2} are isolated if the parasitic capacitors are ignored for simplicity. The signal-dependent charges of the switches only flow to the input sources and to ground, respectively, and do not change the voltage on the capacitors of C_{s1} and C_{s2}. Using this clocking scheme, the charge injection is reduced to the charge injected by four switches that are controlled by P_1 and P_2. The common-mode voltage of the integrator is set at 2.5 V with a 5 V supply. To accommodate this common-mode voltage, the switches driven by P_1 and P_2 are implemented with the minimum size transmission gate switches composed of PMOS and NMOS switches.

Adding 10 % mismatch in switches and 10 mV offset in the opamp A_0 (Fig. 6.12), the simulated input-referred offset of the ΔΣ modulator (suppressed by the CFIA's gain of 100) is about 1 μV. This residual offset will be removed by system-level chopping which will be described in the Sect. 6.4.

Gain Accuracy and Linearity

Using the ΔΣ modulator topology shown in Fig. 6.14, the *same* sampling capacitor C_{S1} is used to sample both the input and DAC feedback signals [6]. As a result, the gain accuracy and linearity of the ΔΣ modulator is not limited by component matching. Furthermore, as shown in Fig. 6.1, the ADC's reference is connected to the reference of the bridge transducers in a ratio-metric structure and the gain accuracy of the reference is thus much relaxed. The gain error and nonlinearity of the ΔΣ modulator would be mainly determined by the non-linear DC gain of the opamp in the first integrator [12]. This nonlinear DC gain can be modeled with a third-order polynomial approximation [12], given by

$$A_{DC}(v_{out}) = A_{DC}(0) \cdot (1 - \delta_3(\frac{|v_{out}|}{d_{\max}})^3) \tag{6.12}$$

where $A_{DC}(0)$ is the DC gain at the midlevel output, δ_3 is the gain variation coefficient, v_{out} is the output swing and d_{max} is the maximum output swing.

As shown in Fig. 6.15, a DC gain of 100 dB and a $\delta_3 < 0.4$ are enough to achieve a 21 bit INL.

As mentioned before, a DC gain of 160 dB is required in the opamp in the first integrator to suppress the 1/*f* noise of the ADC down to 1 mHz. Thus, a two-stage opamp is implemented with a telescopic gain-boosting first stage and a class-A output stage to accommodate output swing. Figure 6.16 shows the DC gain characteristic of the two-stage opamp vs. the output swing. It is clear that the gain is nonlinear and a maximum gain is obtained when the output voltage is zero and it decreases as the output voltage increases ($\delta_3 = 0.2$). According to the simulation results in Fig. 6.15, it is evident that a typical INL of 1 ppm can be achieved in the ΔΣ modulator.

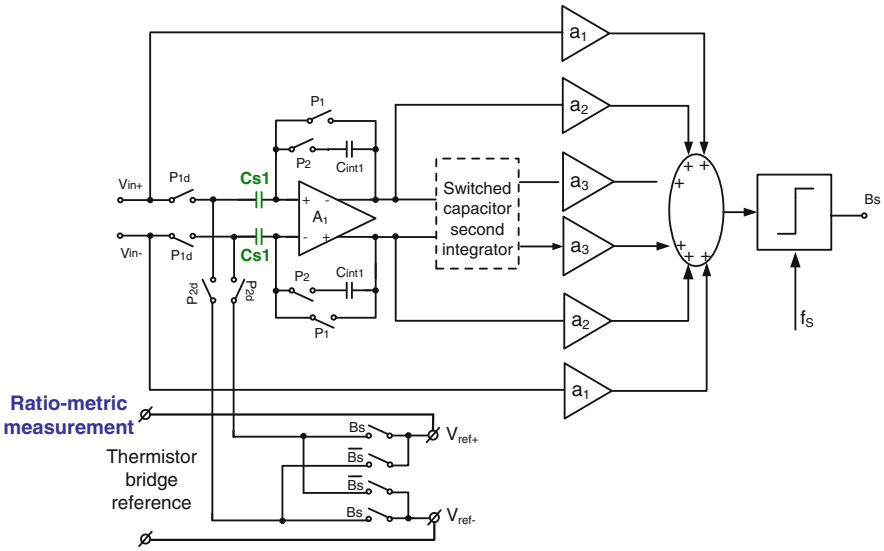


Fig. 6.14 A ΔΣ modulator topology with the *same* capacitor for input and feedback sampling

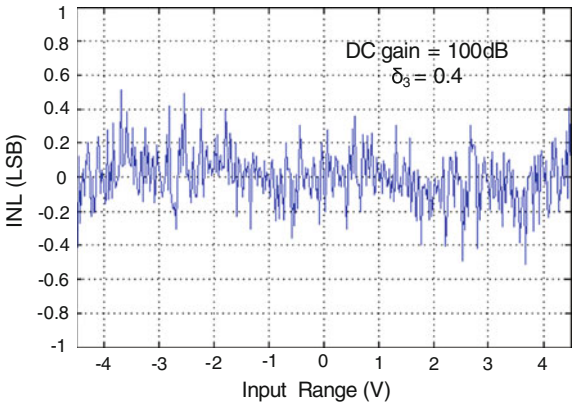


Fig. 6.15 INL simulation with DC gain of 100 dB and $\delta_3 = 0.4$

Settling

The settling at two places need to be taken into account in the design of the read-out IC: (1) at the interface between the CFIA and the ADC; (2) in the first integrator of the ADC.

The settling process is composed of two phases, slewing and linear settling thus the total settling time is given by

$$t_S = t_{slew} + t_{settling} \tag{6.13}$$

Usually, 25 % of the total settling time is allocated to slewing, as typical design practice [13], thus

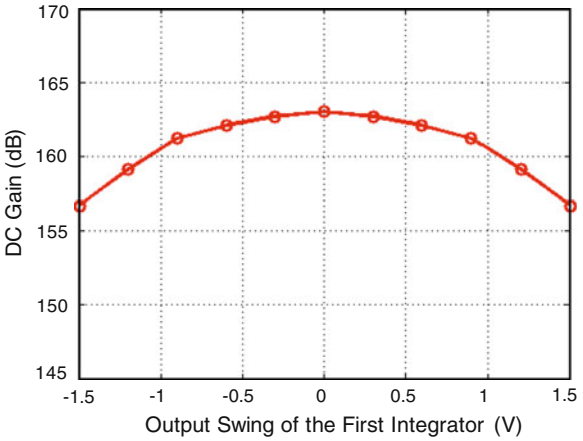


Fig. 6.16 DC gain of the first integrator versus output swing

$$t_S = 0.25t_S + 0.75t_S \tag{6.14}$$

The slew time depends on the bias current and the charging capacitor, which defines the slope of the sampled voltage; while the settling time depends on the time constant τ. With a sampling frequency of 30 kHz for auto-zeroing, the total available settling time is half of the clock period, which is 16.7 µs. The resulting slew time is 4.2 µs and the linear settling time is 12.5 µs.

To achieve a resolution of N bit (21-bit), the two settling error at the two places (at the interface between the CFIA and ADC and in the first integrator of the ADC must be both less than half an LSB. The required time constant τ for linear settling is given by [14]

$$\tau_0 > \frac{t_{settling}}{(N+1)\cdot \ln 2} \tag{6.15}$$

with $t_{settling} = 12.5$ µs, the required time constant τ_0 is 0.82 µs.

The settling requirement at the interface between the CFIA and ADC is determined by the time constant τ_{CFIA} of the CFIA, which is equal to $C_{\mathrm{load}}/G_{\mathrm{m1}} =$ 6pF/250 µA/V = 0.024 µs. Since τ_{CFIA} is much smaller than τ_0, the settling error at the interface is negligible.

The settling of the first integrator is determined by its opamp since the time constant of the switches and the sampling capacitor is negligible. For a sampling switch with a W/L ratio of 5 µm/0.7 µm, the on-resistance is about 1 kΩ. Thus the associated time constant is 0.003 µs, much smaller than the required time constant τ_0.

As discussed before, the opamp employs a two-stage topology, which offers an optimal compromise between the output swing and the noise. The class-A output stage accommodates the output swing and provides additional DC gain. The noise bandwidth of the integrator is determined by the UGB of the opamp and the feedback factor β [14]. The larger the noise bandwidth, the more noise aliasing occurs. The total noise from the opamp is determined by the Miller compensation

capacitor C_C. To make the opamp's noise negligible, C_C should be chosen larger than the input sampling capacitor C_S. In this design, C_C is chosen 11pF large than C_S of 3pF. The bias current of the first stage in the opamp is determined by the slewing requirement, given by

$$I_{bias} = \frac{C_C \cdot V}{\Delta t} = \frac{11pF \cdot 1V}{4.2\,\mu s} \approx 2.5\,\mu A \tag{6.16}$$

where the maximum output swing is 1 V and the slew time is 4.2 μs. With a 2.5 μA bias current, the transconductance g_m of one transistor in the differential pair is chosen to be 42 μA/V. The time constant of the first integrator is then given by [14]

$$\tau = \frac{1}{2\pi f_{UGB} \cdot \beta} = \frac{C_C}{g_m \beta} \tag{6.17}$$

where $\beta = 0.77$(C_S = 3pF, C_{int} = 10pF), g_m = 42 μA/V and C_C = 11pF, thus τ equals 0.34 μs, which is smaller than that required by the linear settling time of 12.5 μs. It can be seen that the settling is a bit over-designed. However, since the CFIA consumes 82 % of the power consumption of the read-out IC, further reducing the power consumption of the ADC will not lead to a significant reduction in the total power consumption.

6.3 Gain Accuracy Improvement Techniques in the Read-Out IC

In the read-out IC, the gain accuracy of a SC ΔΣ ADC, depending on capacitor matching, is typically 0.1 %. The gain error of the CFIA, determined by the mismatch of the input and feedback transconductors (in the order of 1 %), then dominates gain accuracy of the read-out IC. For some strain gauge applications [15], a gain error of 0.02 % is required. To achieve this, the same level of transconductor matching is required. Such accurate matching cannot be expected solely from precision layout technique. In addition, their gain drift should also be less than 10nV/°C and 10 ppm/°C, respectively. Such drift performances cannot be achieved with conventional one-shot trimming during production. This section will explore the system-level collaboration between the CFIA and the ADC to improve the CFIA's gain accuracy and gain drift. In this way, the CFIA and the ADC are linked or *"tuned"* to each other to improve the overall performance.

6.3.1 Dynamic Element Matching

Using precision external gain-setting resistors, the gain error of the CFIA is then mainly determined by the mismatch of the input and feedback transconductors, G_{m3} and G_{m4}. To average out this mismatch, DEM is applied to swap their inputs

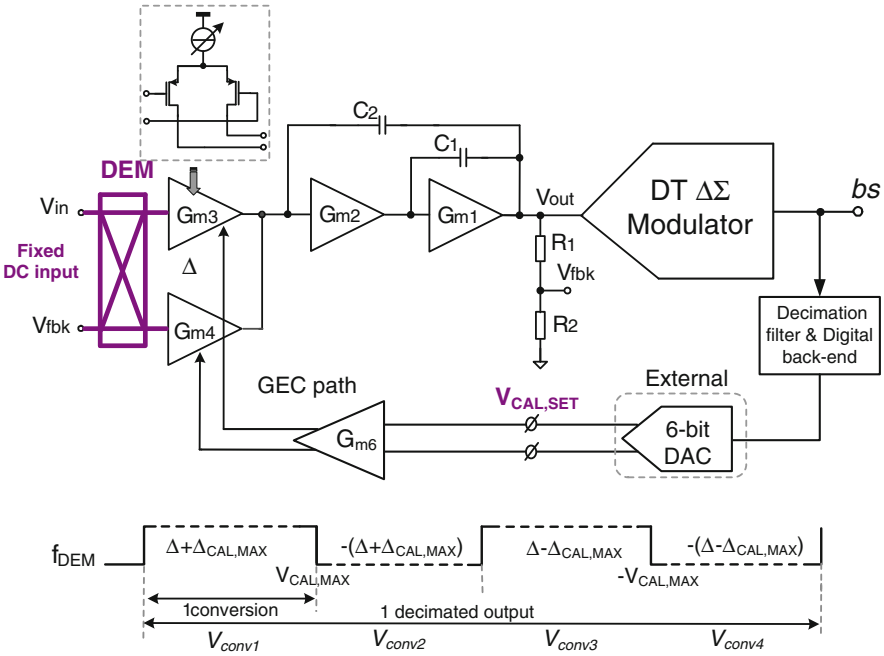


Fig. 6.17 Read-out IC employing dynamic element matching of G_{m3} and G_{m4} and the gain error correction scheme

as shown in Fig. 6.17 [17]. This is implemented by an input multiplexer which is the so called *swapper* [18]. After applying DEM, the average gain error becomes

$$|Gain\ Error| = |1 - \frac{\frac{1+\Delta}{1} + \frac{1}{1+\Delta}}{2}| \approx \frac{\Delta^2}{2} (\Delta << 1) \tag{6.18}$$

From (6.18), DEM reduces the mismatch from Δ to $\Delta^2/2$. Thus, for a typical G_m mismatch of 2 %, DEM reduces the gain error to 0.02 %.

For a CFIA, however, it typically operates with different input and feedback CM voltage. Thus the input and feedback transconductors exhibit certain CM-dependency due to finite CMRR, resulting in a CM-dependent mismatch Δ_{cm}. Unlike the mismatch Δ mentioned in (6.18), this CM-dependent mismatch Δ_{cm}, say, reference to feedback CM voltage, is always located at the G_m stage in the input path. This implies that DEM will not suppress the Δ_{cm} and the resulting gain error is given by

$$|Gain\ Error| = |1 - \frac{\frac{1+\Delta+\Delta_{cm}}{1} + \frac{1+\Delta_{cm}}{1+\Delta}}{2}| \approx \frac{\Delta^2}{2} + \frac{\Delta \times \Delta_{cm}}{2} + \Delta_{cm} \quad (for \Delta << 1) \tag{6.19}$$

From (6.19), the CM-dependent mismatch Δ_{cm} will not be suppressed by the DEM. To improve gain accuracy, the transconductances of G_{m3} and G_{m4} should be kept constant over the input CM range. As shown in [3], their CM dependency was mitigated in a power-efficient manner by cascoding the input transistors with low-threshold devices M_3-M_4 (Fig. 4.19). However, the CM-dependent mismatch Δ_{cm}, still in the order of 0.12 % [16], is the main limitation on the final gain accuracy. Circuit-level techniques will be proposed to address this problem in Sect. 6.6.1. For simplicity, this issue will be neglected in the following analysis.

Another issue with different common-mode levels is that swapping the inputs of G_{m3} and G_{m4} results in large spikes at the CFIA's output. To avoid digitizing these spikes, similar to the LF choppers, the multiplexer's state is altered during the reset period (1 ms) at the start of every ADC conversion (Fig. 6.17).

6.3.2 Digitally-Assisted Gain Error Correction Scheme

Although the use of DEM reduces the mismatch from Δ to $\Delta^2/2$, which is small enough, the mismatch may still vary over temperature, causing a gain drift around 5 ppm/°C. To reduce gain drift further, the mismatch Δ itself should be minimized, so as to achieve a better tracking between the input and feedback transconductors to counteract temperature drift. Therefore, a gain error correction (GEC) scheme is used to compensate for the static mismatch between G_{m3} and G_{m4}. It is implemented in a digitally-assisted manner with existing ADC to minimize complexity and area of analog circuitry.

The GEC path, as shown in Fig. 6.17, consists of a decimation filter, digital back-end and a 6-bit DAC which trims this mismatch by fine-tuning the tail currents of G_{m3} and G_{m4} via the transconductor G_{m6}. With a 20-bit resolution in the ADC, the output of the digital back-end is sufficiently precise. Assuming the initial gain error of the read-out IC is 1 % and it needs to be reduced to 0.02 % (a 34 dB reduction ratio), 6-bit resolution is required for the DAC. For flexibility, the DAC is implemented with a $\Delta\Sigma$ DAC consisting of an interpolation filter, a digital $\Delta\Sigma$ modulator and an RC low-pass filter (LPF).

The GEC scheme uses linear interpolation to find the calibration voltage during the start-up. Figure 6.18 shows the concept of the linear interpolation. By applying a fixed DC signal to the CFIA, the appropriate value of V_{CAL} can be determined within two DEM periods. In the first DEM period, the maximum calibration voltage $V_{CAL,MAX}$ within the DAC's output range is applied to the inputs of G_{m6}. The decimated results of two conversions within one DEM period are given by

$$V_{conv1} = V_{out,ideal}\frac{1+\Delta+\Delta_{CAL,MAX}}{1} = V_{out,ideal}(1+\Delta+\Delta_{CAL,MAX}) \tag{6.20}$$

$$V_{conv2} = V_{out,ideal}\frac{1}{1+\Delta+\Delta_{CAL,MAX}} \approx V_{out,ideal}(1-\Delta-\Delta_{CAL,MAX}) \tag{6.21}$$

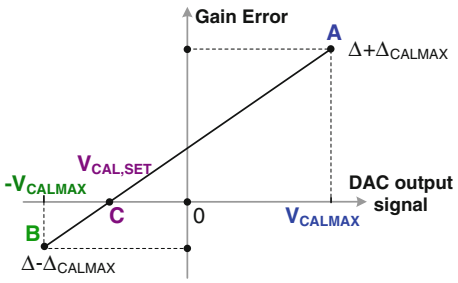


Fig. 6.18 Linear interpolation for the gain error correction scheme

where Δ is the initial mismatch of G_{m3} and G_{m4}, and $\Delta_{CAL,MAX}$ is the extra mismatch caused by $V_{CAL,MAX}$. The output-referred mismatch error due to $(\Delta + \Delta_{CAL,MAX})$ can be determined from the difference of these two conversion results (6.20) and (6.21), as written by

$$V_{out,error,A} = 2V_{out,ideal}(\Delta + \Delta_{CAL,MAX}) \tag{6.22}$$

which is noted as point A in Fig. 6.18.

In the second DEM period, the minimum signal $-V_{CAL,MAX}$ within the DAC's output range is applied to G_{m6}. The decimated result of one conversion in half of the DEM period is expressed as

$$V_{conv3} = V_{out,ideal}\frac{1 + \Delta - \Delta_{CAL,MAX}}{1} = V_{out,ideal}(1 + \Delta - \Delta_{CAL,MAX}) \tag{6.23}$$

The decimated result of one conversion in the other half of the DEM period is given by

$$V_{conv4} = V_{out,ideal}\frac{1}{1 + \Delta - \Delta_{CAL,MAX}} \approx V_{out,ideal}(1 - (\Delta - \Delta_{CAL,MAX})) \tag{6.24}$$

The output-referred mismatch error due to $(\Delta - \Delta_{CAL,MAX})$ can also be determined by the difference of (6.23) and (6.24), as expressed by

$$V_{out,error,B} = 2V_{out,ideal}(\Delta - \Delta_{CAL,MAX}) \tag{6.25}$$

which is noted as point B in Fig. 6.18. Under the condition that the DAC output range is linear to the induced mismatch and furthermore the DAC output range is larger than the worst-case static mismatch of G_{m3} and G_{m4}, the value of $V_{CAL,SET}$ that minimizes the mismatch error (point C) then can be found by linear interpolation (Fig. 6.18). Since the calibration voltage is found within two DEM periods, one decimated output is also chosen to be the average result of two DEM periods, i.e. four conversions.

Since G_{m3} and G_{m4} are biased in weak inversion for maximum power efficiency, and so their mismatch can be tuned by adjusting their tail currents with a transconductor G_{m6}. To attenuate the noise contribution of the GEC path, the transconductor G_{m6} is implemented with resistor-degeneration stage to attenuate

the noise from the GEC path ($G_{m3}/G_{m6} = 480$) and thus, the voltage across the input of G_{m6} are linear to the induced mismatch. Since the calibration voltage $V_{CAL,SET}$ is determined by the ratio of gain errors at points A and B, the value of the fixed DC input during calibration does not need to be known. After finding the calibration voltage $V_{CAL,SET}$ in the start-up, the digital word of the DAC freezes and the read-out IC enters the normal operation.

6.4 Offset and 1/*f* Noise Suppression Techniques in the Read-Out IC

For sensor application, the bandwidth of interest is usually several Hz. At low frequencies, offset and 1/*f* noise are the dominant error sources. To mitigate these errors, nested-chopping techniques can be applied in various ways. Two different possibilities will be described in this Section.

6.4.1 Previous Approach (Multi-Stage Chopping and System-Level Chopping)

Figure 6.19 shows a simplified block diagram of the read-out IC consisting of a three-stage CFIA and a SC ΔΣ ADC. In previous work, the input and intermediate stages of the CFIA were both chopped, so as to suppress their own 1/*f* noise while providing enough gain to suppress the input-referred 1/*f* noise of the un-chopped output stage. However, the resulting up-modulated offset and 1/*f* noise would give rise to a few hundred mV of chopper ripple at CFIA output [3].

In principle, the ADC's clock scheme could be designed such that the ripple would only be sampled at zero-crossings. However, this is not a robust solution since the exact location of the zero-crossings will be a function of the CFIA's closed-loop frequency response, which, in turn, is a function of its user-selectable closed-loop gain (Fig. 6.19). As a result, the ripple will not be sampled exactly at zero-crossings, resulting in residual offset and noise. Moreover, any clock jitter will also be translated into excess noise. To avoid such issues, chopper ripple must be suppressed.

In [16], the input stages were chopped at 30 kHz, which was chosen to be slightly above their 1/*f* corner frequency and equal to the sampling frequency of ΔΣ ADC. The resulting ripple was removed by a continuous-time offset reduction loop (ORL) (Fig. 6.20), which synchronously demodulated the CFIA's output chopper ripple and used the information to null the offset, and hence the ripple. The intermediate stage is chopped at a higher frequency (600 kHz), to ensure that its resulting chopper ripple is sufficiently suppressed by the LPF formed by the CFIA's compensation network. However, the associated charge injection and

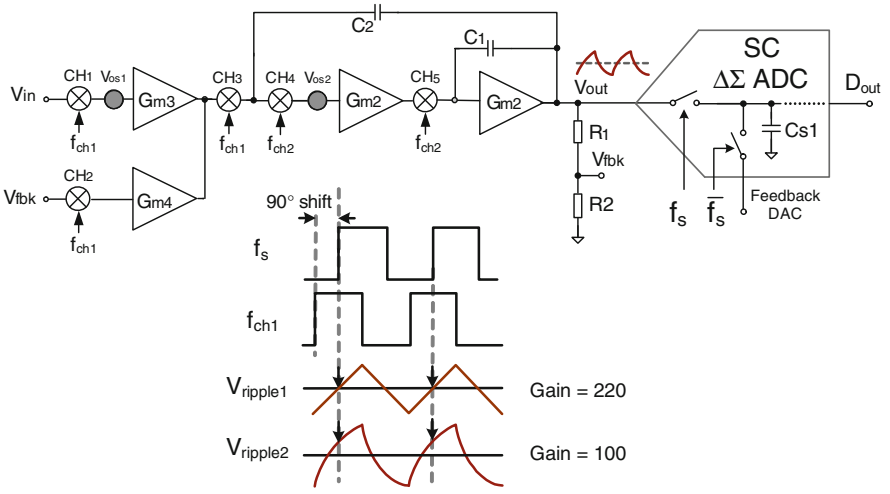


Fig. 6.19 Simplified block diagram of the read-out IC

clock spikes are observed to increase the CFIA's residual offset from 1μV to 5μV. Furthermore, interaction between the high frequency ripple and the shaped quantization noise of ΔΣ modulator is observed to increase low-frequency noise. In [16], this excess noise is suppressed by chopping the intermediate stage in a bitstream-controlled (BSC) manner [19], so as to eliminate the correlation between the chopper ripple and the quantization noise. Since the BSC chopping frequency f_{BSC} is never higher than $f_S/2 = 15$ kHz, the residual offset is only reduced to 3μV. The entire read-out IC is then chopped after every two conversions (Fig. 6.21) and the low-frequency ripple is averaged in the digital decimation filter, resulting in a worst-case offset of 200 nV.

6.4.2 *Proposed Approach (Input-Stage Chopping Combined with System-Level Chopping)*

In this approach, a nested-chopping scheme that simply combines input stage chopping (in the CFIA) with system-level chopping (of the whole read-out IC) is shown to achieve tens of nV-level offset and a sub-mHz $1/f$ noise corner. In this scheme, the intermediate stage is not chopped, thus avoiding a potential source of residual offset and ripple. As in [16], a ORL is applied to reduce the ripple associated with the chopped input and feedback transconductors.

Applying DEM could cause some offset drift due to different input and feedback CM voltage. To average out this drift, the frequency of the system-level chopping is chosen to be half of the DEM frequency (Fig. 6.21) and one decimated

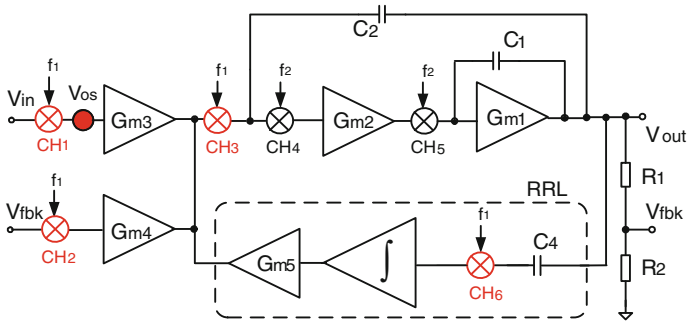


Fig. 6.20 Simplied block diagram of the CFIA with ripple reduction loop

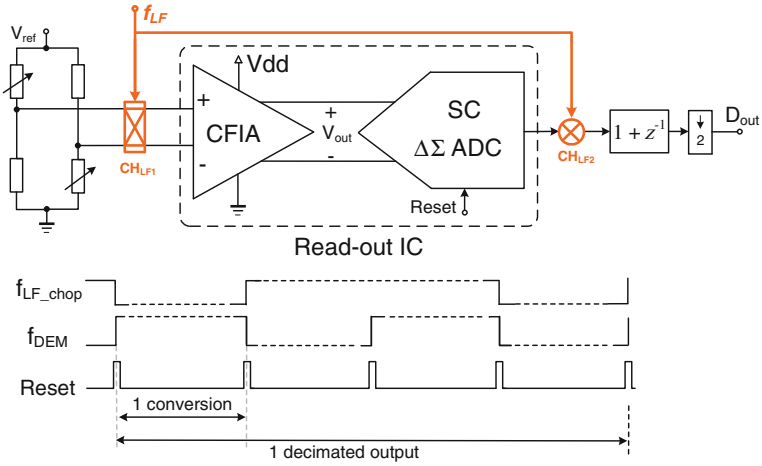


Fig. 6.21 Read-out IC with system-level chopping and the associated timing diagram

digital output is the average result of four ADC conversions. Instead of using a "0011" pattern for the system-level chopping in four conversions, a "0110" pattern is chosen in this work. Assuming that X is the DC input signal, V_n is the read-out IC's low-frequency errors, i.e. offset, drift, and 1/*f* noise, and Y is the digital output of one system-level chopping period. When applying system-level chopping with "0011" pattern, the output Y can be expressed as

$$\begin{aligned} Y &= \frac{(X+V_n)+(X+V_n)\cdot z^{-1}+(X-V_n)\cdot z^{-2}+(X-V_n)\cdot z^{-3}}{4} \\ &= X+\frac{V_n}{4}(1+z^{-1})^2(1-z^{-1}) \end{aligned} \tag{6.26}$$

However, after applying "0110" pattern, the output Y is expressed as

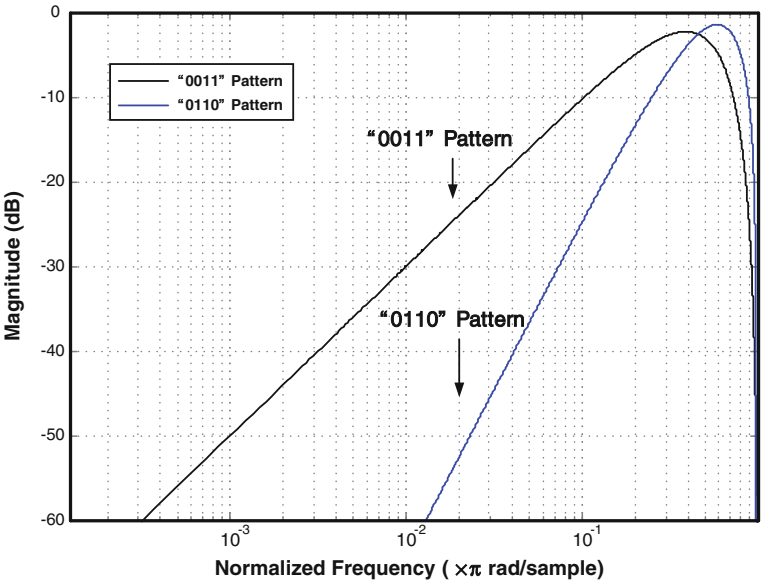


Fig. 6.22 High-pass filtering effect of system-level chopping on the low-frequency noise with "0011" or "0110" chopping pattern

$$Y = \frac{(X + V_n) + (X - V_n) \cdot z^{-1} + (X - V_n) \cdot z^{-2} + (X + V_n) \cdot z^{-3}}{4}$$
$$= X + \frac{V_n}{4}(1 + z^{-1})(1 - z^{-1})^2 \tag{6.27}$$

Figure 6.22 shows the transfer functions of these two chopping patterns on the 1ow-frequency errors. It can be seen that the "0011" pattern exhibits a first-order high-pass filtering (HPF), while the "0110" pattern exhibits a second-order HPF, which imposes better rejection over low-frequency errors. More intuitively, it can be seen that, unlike the "0011" pattern, the "0110" pattern can exactly compensate for any offset drift that is a linear function of time.

Chopping just the input stage of the CFIA reduces its 1/*f* noise corner from 10 kHz to 0.3 Hz, Therefore, when the system-level chopping frequency is chosen to be higher than 0.3 Hz, the CFIA's *1/f* noise will be effectively suppressed. For one decimated output, it takes 5200 clock cycles (four conversions) with a sampling frequency of 30 kHz, the system-level chopping frequency f_{sys} equals 30 kHz/5200 = 5.8 Hz. Therefore, the low-frequency noise lower than this frequency will be removed by system-level chopping.

Simulations in periodic steady-state (PSS) and periodic noise analysis (PNOISE) tools of Spectre RF [11] are made to confirm the validity of above analysis. Figure 6.23 shows the simulated input-referred noise spectrum of the read-out IC with various 1/*f* noise suppression techniques. The input-stage chopping combined with system-level chopping achieves a 1/*f* noise corner frequency

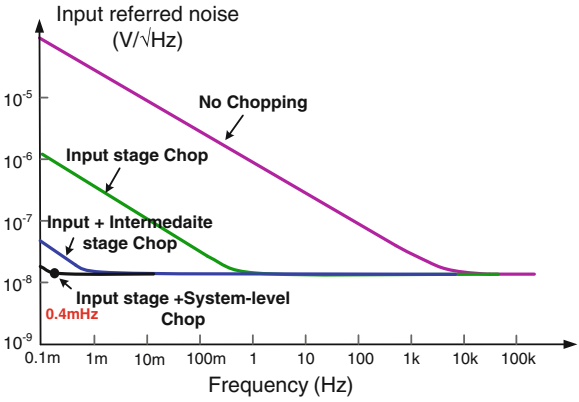


Fig. 6.23 Simulated input referred noise spectrum of read-out IC with various 1/*f* noise suppression techniques

of 0.4 mHz, which is comparable to the result achieved by the multi-stage chopping combined with system-level chopping (1/*f* noise corner less than 1 mHz).

6.5 Error Correction Techniques Summary

Figure 6.24 shows a bridge-readout system based on the proposed read-out IC with associated timing diagram. Table 6.3 summaries the errors and the associated error correction techniques applied in the proposed read-out IC. The gain error and gain drift are reduced by using DEM and the digitally-assisted gain error correction scheme. The offset and 1/*f* noise are suppressed by the combination of input stage chopping in the CFIA and system-level chopping (The second pair of choppers can be turned off, thus they are displayed grey in the Fig. 6.24). The chopper ripple of the input stage is removed by the ripple reduction loop.

6.6 Circuit Implementations

6.6.1 CFIA Implementation

The Input and Feedback G_m Stages with Enhanced CM Immunity

As discussed in Sect. 6.3.1, with the same CM, DEM reduces gain error of the CFIA from Δ to $\Delta^2/2$. However, with different CM, the CM dependency between G_{m3} and G_{m4} limits the gain accuracy even with DEM applied. To improve gain accuracy, the transconductances of G_{m3} and G_{m4} should be kept constant over the input CM range. Figure 6.25 shows the conventional input and feedback G_m stages [3, 16]. Their CM dependency was mitigated in a power-efficient manner by

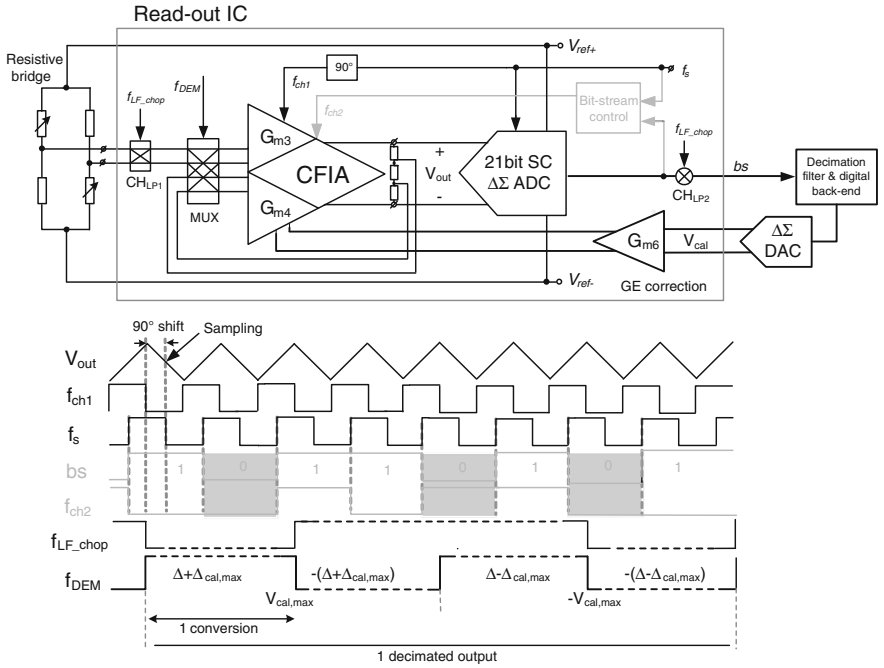


Fig. 6.24 Block and timing diagrams of a bridge-readout system based on the proposed read-out IC

Table 6.3 Errors and the associated error-correction techniques employed in the read-out IC

Error	Error correction techniques
Gain error and gain drift	Dynamic element matching and digital-backend gain error correction (Sect. 6.3)
Offset and 1/*f* noise in CFIA	Input stage chopping + system-level chopping or multi-stage chopping + system-level chopping (Sect. 6.4)
Offset and 1/*f* noise in ADC	Auto-zeroing in the first integrator (Sect. 6.2.2)
Chopper ripple from the input stage	Offset reduction loop and zero-crossing sampling (Sect. 6.4)

cascoding the input transistors with low-threshold devices M_3–M_4. Transistors M_1–M_4 operate in weak inversion at a large G_m/I_b ratio. The resulting drain-source voltage V_{DS} of M_1 equals the threshold difference of M_1 and M_3, which is about 0.18 V. This small V_{DS} limits the output impedance of the input differential pair.

Two opposing effects influence the G_m of the input (or feedback) stage in Fig. 6.25. When the CM level increases, the V_{DS} of M_1 also increases due to channel length modulation, leading to an increased G_m, as shown in curve-2 in Figs. 6.26a and b. On the other hand, the increased CM level reduces the head-room of the tail

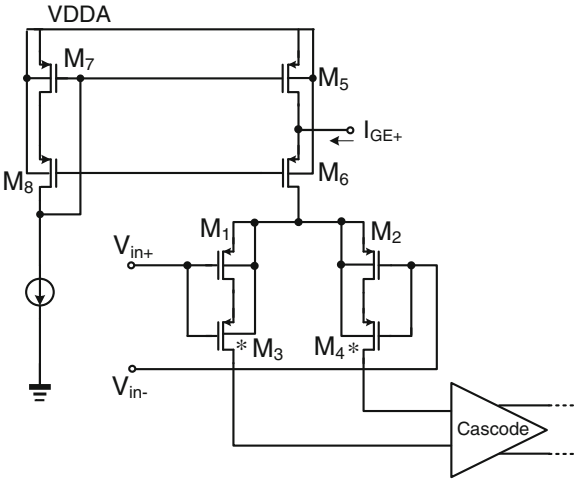


Fig. 6.25 Conventional input (or feedback) G_m stage implemented with PMOS differential pair and low-threshold cascoding [3]

current source M_5, hence reducing a tail current and the G_m of the input differential pair, as depicted by curve 1 in Fig. 6.26a and b. These two opposing effects might provide an improved CM immunity. However, due to the limited V_{DS} of M_1, the channel-length modulation effect is much larger than the reduced bias-current effect. The G_m of the input differential pair, therefore, exhibits a limited CM immunity. Increasing the output impedance of the input pair will reduce the channel length modulation effect and thus flatten the slope.

Figure 6.29 shows the simulated G_m variation of the input or (feedback) stage for an input CM range of −0.1 V to 2.8 V (typical process corner). If the current source in Fig. 6.25 is ideal, the G_m variation is 0.6 % over the CM range, as depicted by curve 1 in Fig. 6.29. If the cascode current source shown in Fig. 6.25 is used, the two opposing effects partially compensate each other. This is because the input pair and the current source are cascoded differently (note that the gate terminals of the input and cascode transistors are connected together in Fig. 6.25). The CM sensitivities of these two circuits thus differ, resulting in a residual G_m variation of 0.07 %, as shown in curve 2 in Fig. 6.29. It is observed that G_m increases with input CM voltage, implying that the CM dependency is limited by the finite output impedance of the input pair.

To boost the output impedance of the input pair, the threshold difference between M_1 and M_3 need to be increased. This can be done in two manners: reducing the threshold of M_3 or increasing the threshold of M_1. To reduce the threshold of M_3, a resistor R_1 can be added between the source of M_1 and the bulk of M_3, as shown in Fig. 6.27a. The voltage drop across R_1 introduces a V_{SB} of 0.3 V, so as to reduce M_3's threshold by 0.1 V. However, this approach needs an extra bias current of I_1, leading to an increase in power consumption. A better alternative is to increase the threshold of M_1. As shown in Figure. 6.27b, resistor R_3 is added between the common sources of M_1 and M_2, and the common bulk of M_1 and M_2. The voltage drop across R_3 introduces a V_{BS} of 0.29 V to M_1,

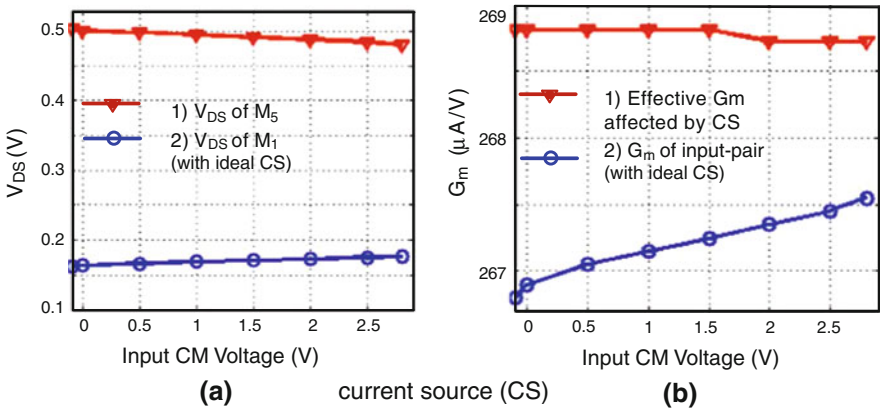


Fig. 6.26 **a** Simulated V_{DS} versus input CM (Fig. 6.25). **b** Simulated G_m versus input CM (Fig. 6.25)

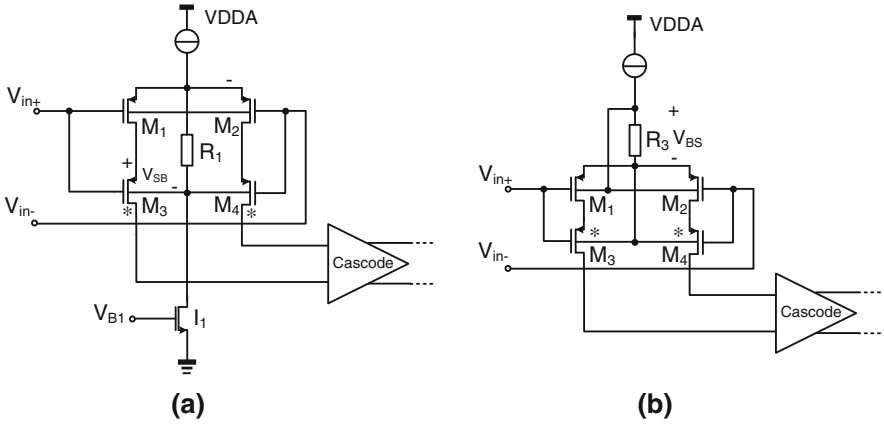


Fig. 6.27 Input (or feedback) G_m stage. **a** The threshold of M_3 is reduced by body effect, **b** the threshold of M_1 is increased by body effect

increasing the threshold of M_1 from about 0.9 to 1 V due to body effect. As a result, the V_{DS} of M_1 increases, boosting the output impedance of the input pair from 200 MΩ to 500 MΩ. The advantage of this solution is that input and cascode transistors all share the same bias current, resulting in better power efficiency.

To improve the CM immunity further, the same cascode configuration is applied in both the input pair and the tail current source (Fig. 6.28), so as to balance their impedance. This ensures that the two opposing effects have nominally the same absolute CM sensitivity and so will completely cancel each other.

The combination of the threshold boosting and impedance balancing techniques reduces the G_m variation from 0.07 to 0.02 % (typical corner) over the input CM range, as shown in curve 3 of Fig. 6.29. Simulations over all process corners show

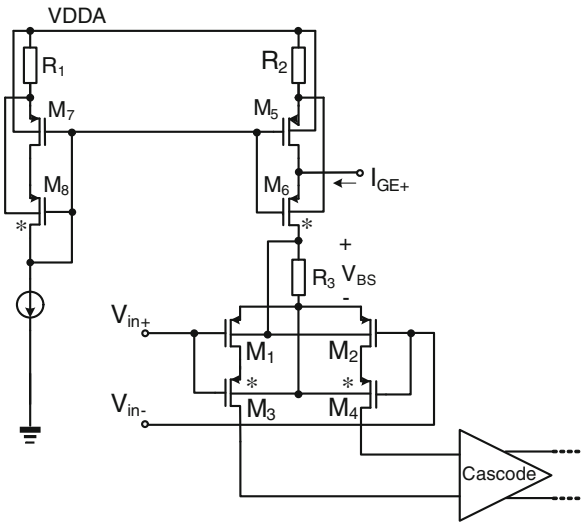


Fig. 6.28 Proposed input (or feedback) G_m stages with enhanced CM immunity

that this reduction is robust to process variation: the maximum G_m variation is reduced from 0.089 % (with Fig. 6.25) to 0.033 % (with Fig. 6.28). The only disadvantage of this approach is that the voltage drops across R_2 and R_3 reduce the input CM range from 0–3.7 V to 0–2.8 V.

Compensation G_{m6} Stage

Transconductance G_{m6} is added to compensate the mismatch of G_{m3} and G_{m4} by fine-tuning their tail currents. The noise contribution from the gain error correction path is negligible because it is attenuated by the ratio of $G_{m3}/G_{m6} = 480$ and suppressed by the finite CMRR of the input stages. G_{m6} is implemented as a resistor-degenerated stage. Its bias current is chosen just large enough to cover the maximum expected mismatch (2 %) between G_{m3} and G_{m4}. the implementation of the intermediate stage G_{m2}, the output stage G_{m1}, the cascode buffer 2 (CB2) and the cascode buffer 1 (CB1) (Fig. 4.15) is similar to that with the ORL [3].

6.6.2 ADC Implementation

This section discusses the implementation of the ADC in the ROIC. The ADC is implemented as a second-order SC ΔΣ modulator followed by a decimation filter. Figure 6.30 shows the block diagram of the modulator with its associated timing diagram. It is implemented using two fully differential switched-capacitor integrators and a clocked comparator. The modulator uses non-overlapping clocks to control the timing for switches. Clocks with delayed falling edges (P_{1d} and P_{1d}) are used to prevent signal-dependent charge injection [5].

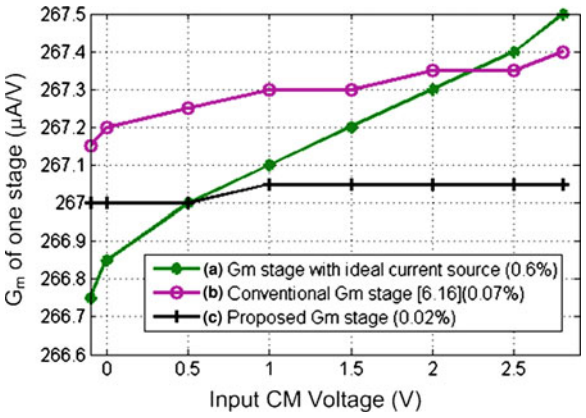


Fig. 6.29 Simulated G_m variations versus input CM **a** with ideal current source, **b** using Fig. 6.25, **c** using Fig. 6.28

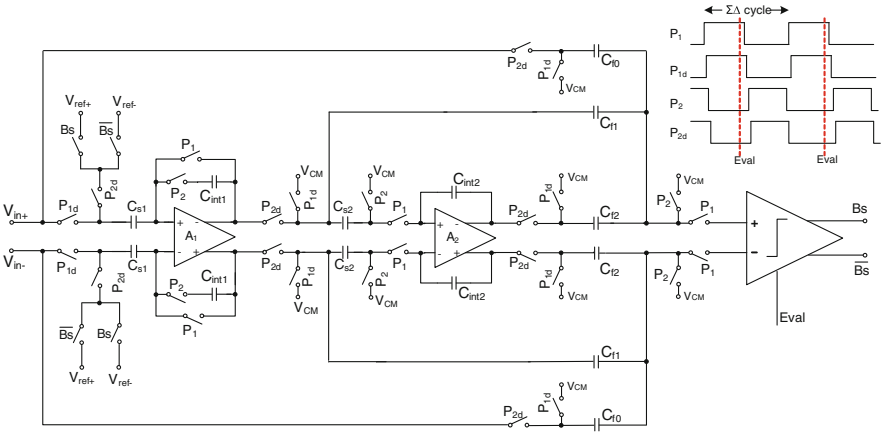


Fig. 6.30 Block diagram of the second order ΔΣ modulator

Topology and Clock Timing

In one ΔΣ cycle, when the first integrator is in the sampling and auto-zeroing phase, as shown Fig. 6.31 (clock P_1 and P_{1d} is high), the input signal and the offset of opamp A_1 are sampled on the sampling capacitors C_{S1}. When the clock P_2 and P_{2d} are high, the charge of the feedback voltage controlled by the bit-stream is subtracted from the charge of the input signal stored on C_{S1}, as shown in Fig. 6.32. The subtraction result is scaled by the ratio of $C_{S1}/C_{int1} = 3/10$, appearing at the integrator output.

When the 1st integrator is auto-zeroed, the signal is not available during this period. Thus the 2nd integrator can only sample the 1st integrator output to the sampling capacitor C_{S2} during the integration phase when P_2 and P_{2d} are high, as shown in Fig. 6.32. In the next half clock period (when P_1 and P_{1d} are high), the charge stored on C_{S2} is transferred to the integration capacitor C_{int2}.

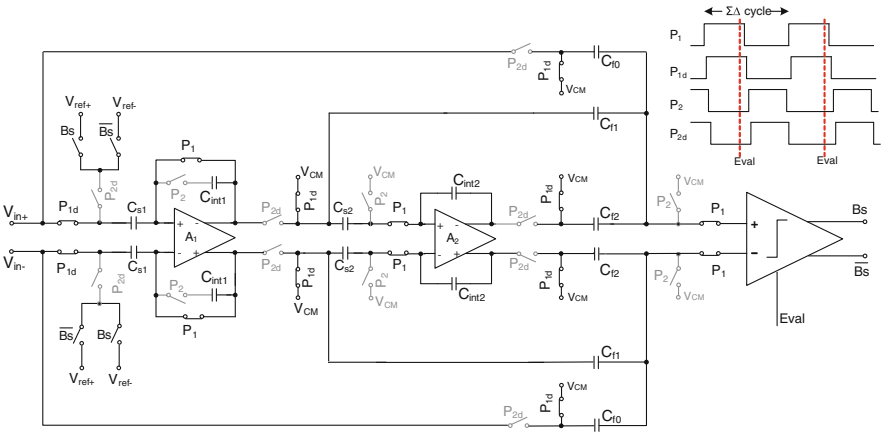


Fig. 6.31 The second-order ΔΣ modulator when P_1 and P_{1d} are "high"

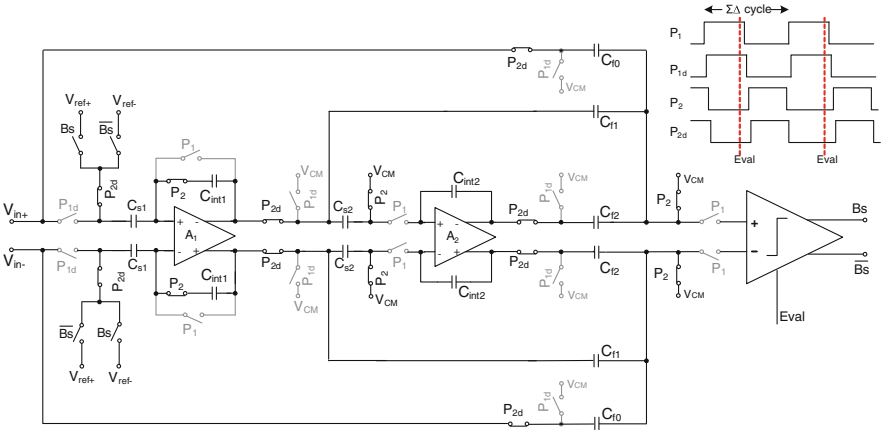


Fig. 6.32 The second-order ΔΣ modulator when P_2 and P_{2d} are "high"

In the feed-forward topology, two feed-forward paths from the input and from the 1st integrator output are introduced. Therefore, an analog adder is required to sum up the signal at the quantizer input. In this design, this adder is implemented in a passive structure in two phases, as shown in Fig. 6.33. It is controlled by the non-overlapping clocks P_1, P_{1d} and P_2, P_{2d}. The feed-forward coefficients are set by the capacitor ratios. The quantizer decides near the end of the clock phase P_1 when the passive adder has fully settled (Fig. 6.30).

The feed-forward coefficients are determined by the ratio between the feed-forward capacitors and the total capacitor summation. When the adder is in the sampling phase (clock P_2 and P_{2d} are high), it samples the input signal (V_{in} +), the first integrator output (V_{int1+}) and the second integrator output (V_{int2+}). Therefore the amount of charge stored on each capacitor is given by:

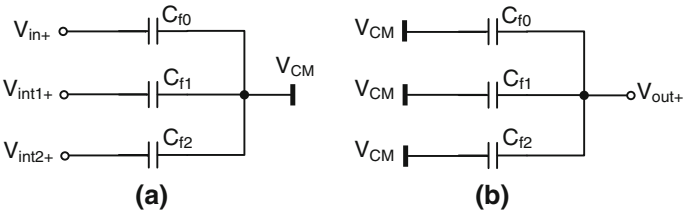


Fig. 6.33 Passive adder on the positive side **a** sampling phase, **b** summing phase

$$Q_{ff0} = C_{f0} \cdot (V_{in+} - V_{CM}) \tag{6.28}$$

$$Q_{ff1} = C_{f1} \cdot (V_{\text{int1}+} - V_{CM}) \tag{6.29}$$

$$Q_{ff2} = C_{f2} \cdot (V_{\text{int2}+} - V_{CM}) \tag{6.30}$$

When clocks P_1 and P_{1d} are high, the adder is in the summing phase with all the sampling capacitors connected in parallel. The charge redistributes itself among them and the output voltage of the adder is derived as

$$V_{out+} - V_{CM} = \frac{C_{f0} \cdot (V_{in+} - V_{CM}) + C_{f1} \cdot (V_{\text{int1}+} - V_{CM}) + C_{f2} \cdot (V_{\text{int2}+} - V_{CM})}{C_{f0} + C_{f1} + C_{f2}}$$
$$= \frac{C_{f0}}{C_{f0} + C_{f1} + C_{f2}} \cdot V_{in+} + \frac{C_{f1}}{C_{f0} + C_{f1} + C_{f2}} V_{\text{int1}+} + \frac{C_{f2}}{C_{f0} + C_{f1} + C_{f2}} V_{\text{int2}+} - V_{CM} \tag{6.31}$$

Equation (6.28) shows that all the feed-forward coefficients are smaller than one, the values of which are listed in Table 6.2 (a_1, a_2, a_3).

Implementation Details

The settling behavior and DC gain of the opamp in the first integrator are important for the overall performance of the modulator. The circuit was therefore designed for complete settling (i.e. the equivalent settling error is less than 130 dB). To achieve a 160 dB DC gain in A_1 for $1/f$ noise suppression, it is implemented with a two-stage Miller-compensated amplifier consisting of a gain-boosted telescopic topology in the first stage and a class-A structure in the second stage (Fig. 6.34). Overall, this opamp has a UGB of 250 kHz with 5pF load capacitor and draws only 38 μA.

Since errors introduced by the second integrator are attenuated by the gain of the first integrator, no offset cancellation or gain boosting are needed here. Thus the opamp A_2 in the second integrator is implemented as a fully-differential two-stage amplifier consisting of a telescopic first stage and a class-A output stage, as shown in Fig. 6.35. This amplifier achieves a DC gain large than 100 dB and a UGB of 60 kHz with 6pF load capacitor while consuming only 8 μA.

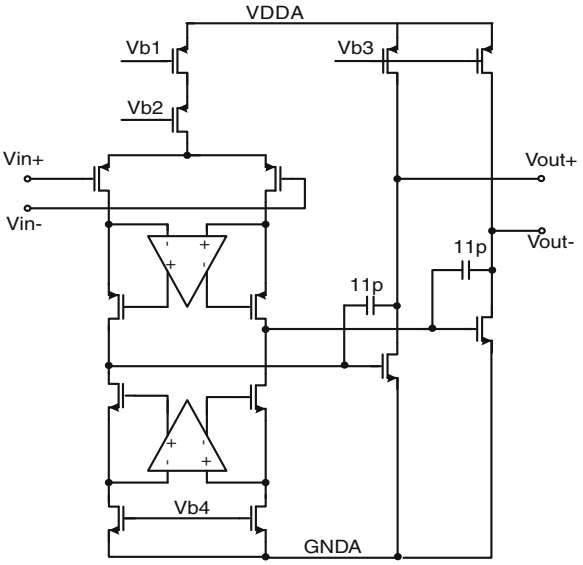


Fig. 6.34 The schematic diagram of the opamp A_1 in the 1st integrator of the $\Delta\Sigma$ modulator shown in Fig. 6.30

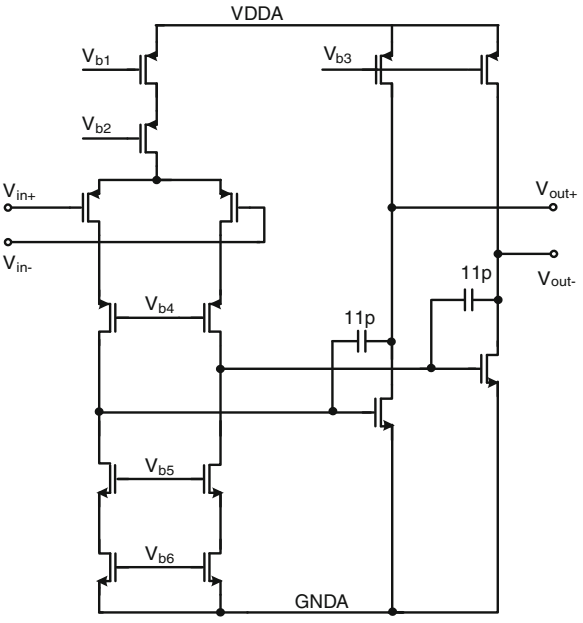


Fig. 6.35 Schematic diagram of the opamp A_2 in the 2nd integrator of the $\Delta\Sigma$ modulator shown in Fig. 6.30

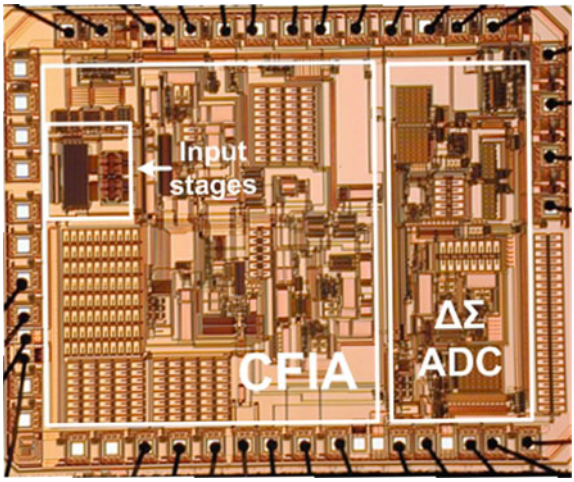


Fig. 6.36 Chip micrograph of the ROIC

6.7 Measurement Results

The read-out IC was fabricated in a standard 0.7 μm CMOS process with low-threshold transistors, linear capacitors and high-resistivity poly-resistors. The chip has an active area of 6 mm^2, as shown in Fig. 6.36. All the measurement results are based on the measurements of ten samples.

Noise Spectrum of the ROIC

Figure 6.37a shows the measured output PSD of the read-out IC, which is set with multi-stage chopping while system-level chopping and DEM are "off". The noise level is flat from 1 mHz with a noise density of 16.2nV/$\sqrt{\text{Hz}}$, corresponding to a resolution of 20-bits with respect to a full-scale range of ±40 mV in 5 Hz bandwidth. To eliminate the low-frequency lobe that would occur due to the interaction between the read-out IC's residual offset and the Hann window used, the read-out IC's offset was subtracted before the FFT was computed. The ADC's sampling frequency f_S and input stage chopping frequency f_{ch1} is lowered to 10 kHz to display higher frequency resolution (10 kHz/2^{24} = 0.596 mHz). As seen from the zero-input FFT plot (b) in Fig. 6.37a, the noise level of the read-out IC is mainly limited by the thermal noise.

Figure 6.37b shows the output noise spectrum of the read-out IC with ORL "on" and "off". It is clearly seen that with "ORL" off, some aliased noise appears at the signal band below 10 Hz, since the chopper ripple at 10 kHz is being sampled by a sampling frequency fs of 10 kHz. Furthermore, the uncertainty of the sampling moment of the chopper ripple due to clock jitter could also induce low frequency noise. Figure 6.37b shows that the ORL is necessary to avoid any aliasing error near DC, so as to achieve a flat noise spectrum down to 1 mHz.

To test the effectiveness of system-level chopping on suppressing the 1/f noise, the choppers in the intermediate stage are turned off, while DEM and system-level

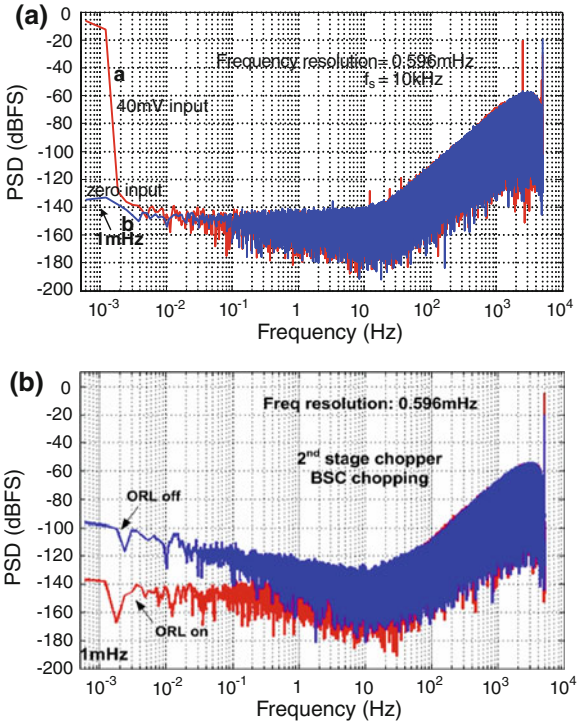


Fig. 6.37 **a** Measured output spectrum of the read-out IC with DEM and system-level chopping off (ORL "on"). **b** Measured output spectrum of the read-out IC with DEM and system-level chopping off (ORL "off" and "on")

chopping are both on. Figure 6.38 shows the measured noise spectrum with decimated output. It is evident that the 1/*f* noise corner is suppressed below 0.1 mHz, showing that input stage chopping combined with system-level chopping can be used as a better alternative to suppress the 1/*f* noise.

Noise Spectrum of the ADC

The measured output spectrum of the ADC alone also achieves a flat noise spectrum from 1 mHz to 10 Hz, as seen from the curve b in Fig. 6.39. This corresponds to a resolution of 21-bit with a full-scale range of ±4 V (reference to 5 V). This result confirms that the DC gain in the auto-zeroing phase of the first integrator is sufficient for 1/*f* noise suppression. The FOM of the ADC (evaluated by FOM = Power/($2^{\mathrm{ENOB}} \times 2f_{\mathrm{B}}$)) is 10 pJ/Conv.

Gain Error

As discussed before, the gain accuracy of the ROIC is mainly determined by the mismatch between the input and feedback G_m stages in the current-feedback instrumentation amplifier. Applying DEM to them reduces the gain error from 0.6 % to ±0.0035 % if G_{m3} and G_{m4} are at the same CM voltage (2.5 V). Including the GEC path further reduces the gain error to ±0.00165 %, as shown in Fig. 6.40. However, due to CM dependency between the G_{m3} and G_{m4}, the gain error rises to 0.12 % in the worst-case when one of the G_m's is at 0 V [16]. Using

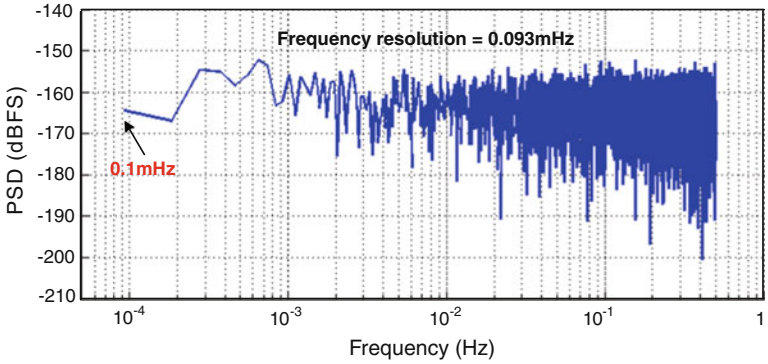
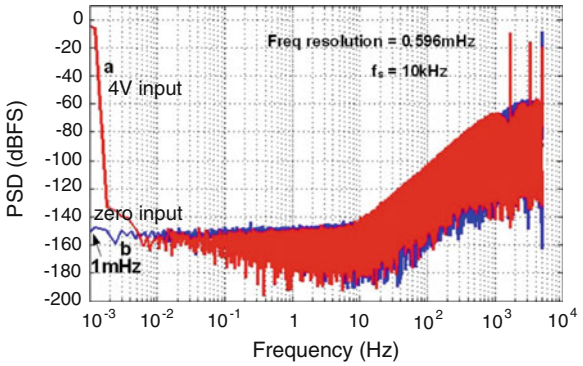


Fig. 6.38 Decimated output spectrum of the read-out IC with Input stage chopping and system-level chopping "on" (Choppers in the intermediate stage are "off")

Fig. 6.39 Measured output spectrum of the ADC alone without CFIA



the bulk-biasing and impedance-balancing techniques (shown in Fig. 6.28), the typical CMRR of the ROIC is increased from 130 to 140 dB, close to that obtained with resistor-degenerated stages [20]. Figure 6.41 shows the measured CMRR histogram of the ROIC compared to [16]. Figure 6.42 shows that the ROIC achieves a gain error of 0.037 % over a CM range of 0–2.5 V, which is a 3.2X improvement compared to [16].

Offset

Figure 6.43 shows the measured offset histograms with different chopping strategies. By employing multi-stage chopping in the CFIA, the ROIC achieves a maximum offset of 4.6 μV (Fig. 6.43a). Turning on the system-level chopping reduces offset to less than 200 nV (Fig. 6.43b) [16]. Tuning off the choppers in the intermediate stage, using the combination of the input stage chopping and system-level chopping achieves a lower offset of 48 nV (Fig. 6.43c), which confirms the analysis discussed in Sect. 6.4.2. The measured worst case offset drift is less than 6 nV/°C.

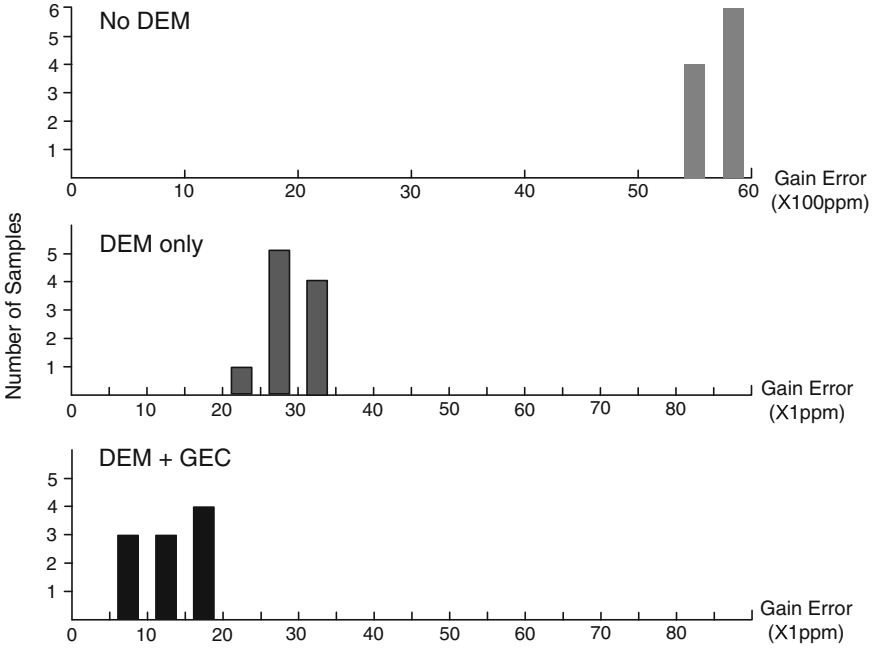


Fig. 6.40 Measured gain error histograms with the same input and feedback CM

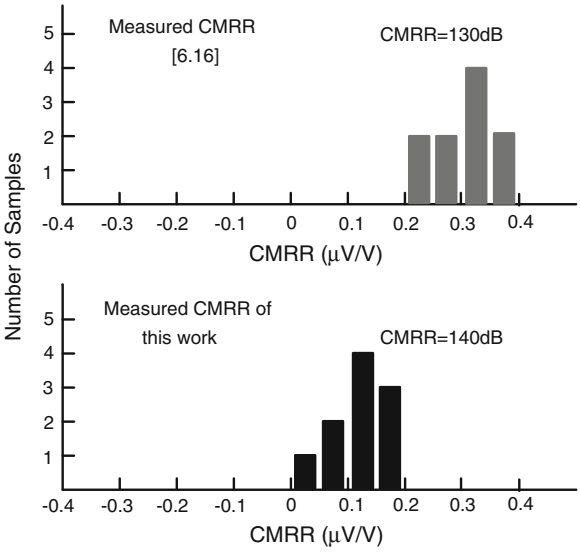


Fig. 6.41 Measured CMRR and comparison to [16] showing the effect of bulk biasing the impedance balancing in improving CM immunity

INL

The current-feedback instrumentation amplifier is the main source of INL, since the measured INL of the ADC is around ±1 ppm, as shown in Fig. 6.44. The use

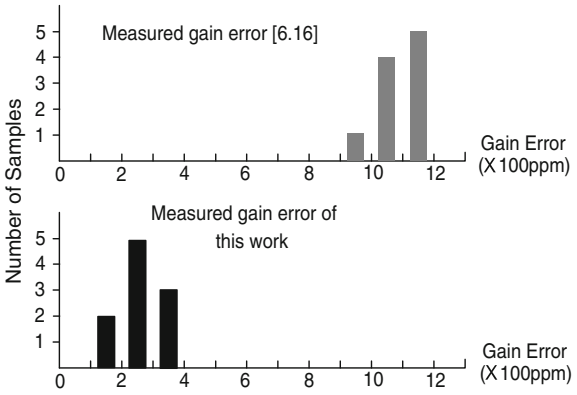


Fig. 6.42 Measured gain error histograms and comparison to [16] showing the effect of bulk biasing the impedance balancing

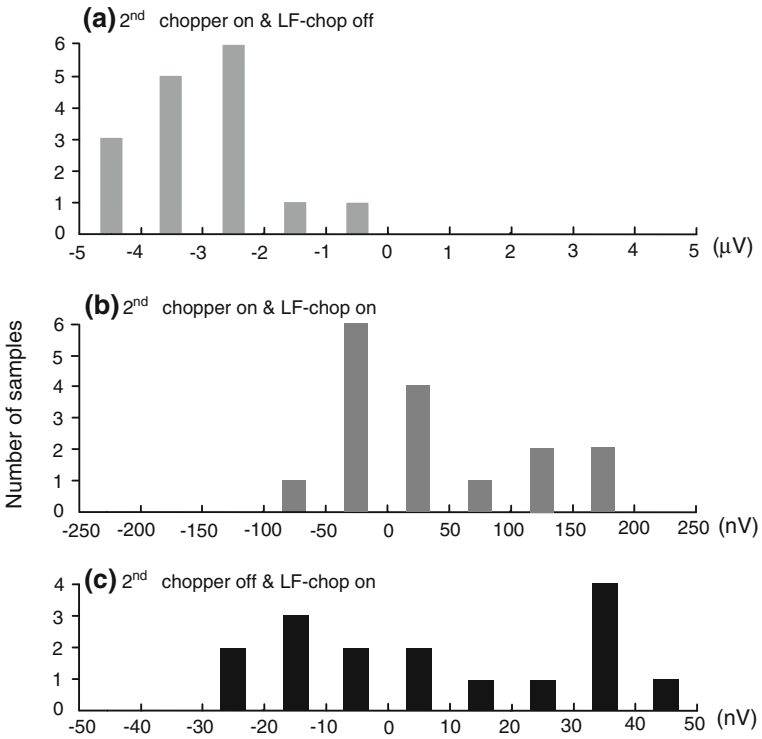


Fig. 6.43 Measured offset histograms

of DEM improves the INL of ROIC from 35 to 5 ppm. When the gain error correction path is turned on, the INL is improved slightly, as shown in Fig 6.45. At low gain settings, saturation of the amplifier's input stages eventually limits its linear input range (INL $<$ 10 ppm) to $\pm$120 mV (with DEM and GEC on), as depicted in Fig. 6.46.

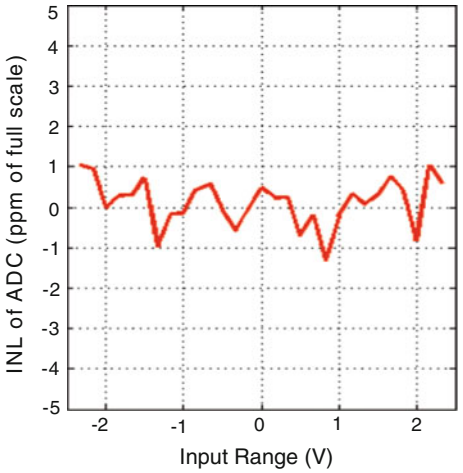


Fig. 6.44 Measured INL of the ADC without CFIA

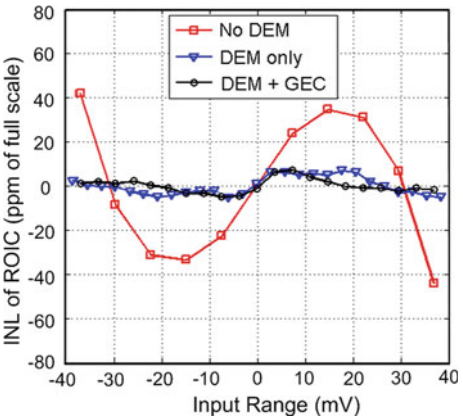


Fig. 6.45 Measured INL of the ROIC. **a** No DEM, **b** DEM only, **c** DEM + GEC

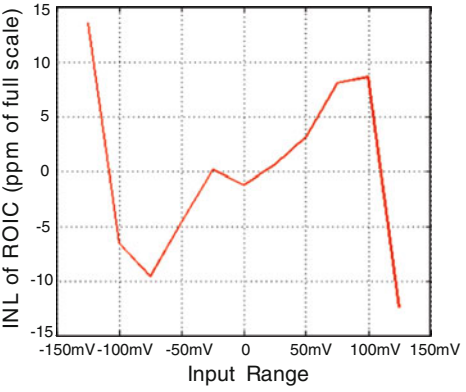


Fig. 6.46 Measured INL of the ROIC with an input range of ± 120 mV

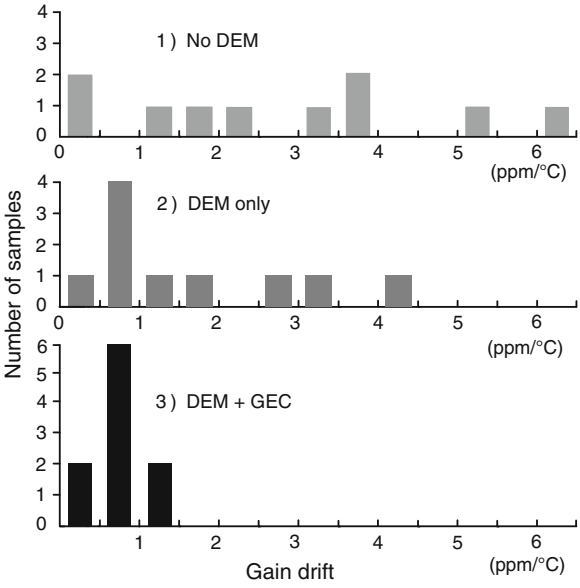


Fig. 6.47 Measured gain drift histograms of the ROIC. **a** No DEM, **b** DEM only, **c** DEM + GEC

Gain Drift

For thermistor and thermalcouple read-out, gain drift of the interface electronics is essential. The use of DEM improves the gain drift from 6.1 ppm/°C to 4.3 ppm/°C. Further applying GEC improves the gain drift to 1.2 ppm/°C, as shown in Fig. 6.47.

Thermistor Measurements with the ROIC

To test and compare the performance of the ROIC with other precision instrument, three measurement set-ups (Fig. 6.48) were used to simultaneously measure the temperature drift in a large (96 cm^3) oven-stabilized aluminum block. The first one used the ROIC to read out a thermistor bridge, the second one used a Keithley 2002 7-1/2 digit multimeter to read-out the same thermistor bridge, the third one used the same Keithley 2002 multimeter to read-out a Pt-100 reference sensor.

The three measurement systems were set-up for a conversion time of 0.25 s, which for the ROIC meant that 5000 samples (@ $f_s = 20$ kHz) were decimated by a $sinc^3$ filter. The measurement results are shown in Fig. 6.49. Due to its lower sensitivity, the resolution of the Pt-100 is much lower than that of the thermistor bridge. The 0.7 μK (rms) temperature-sensing resolution achieved by the thermistors and the ROIC is roughly 2X better than that achieved by the thermistors and the Keithley, despite the fact that the ROIC only draws 270 μA and is much more compact.

The performance of the read-out IC is summarized in Table 6.4 and compared with other state-of-the-art. The read-out IC achieves a typical gain drift of 0.7 ppm/°C and a 5 ppm INL at a gain of 100. Furthermore, the combination of the input stage chopping and system-level chopping enable the read-out IC to achieve

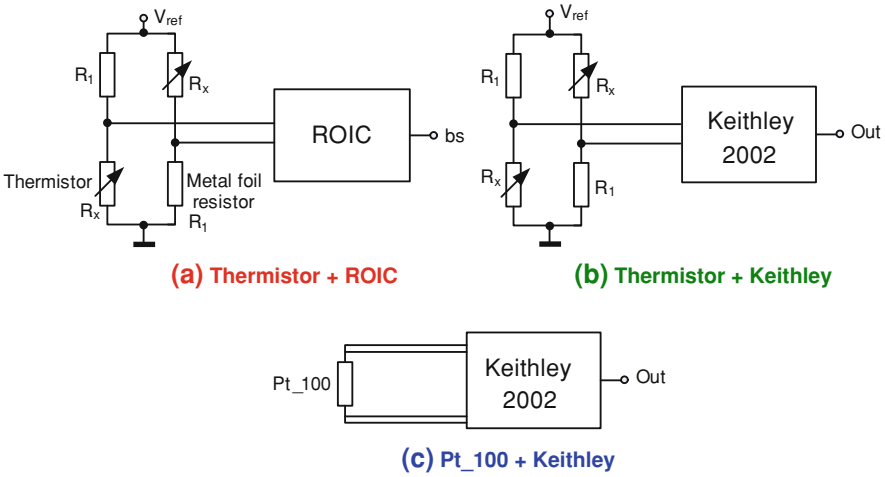


Fig. 6.48 Three comparison measurement set-ups with thermistors and Pt_100. **a** Thermistor + ROIC, **b** Thermistor + Keithley, **c** Pt_100 +Keithley

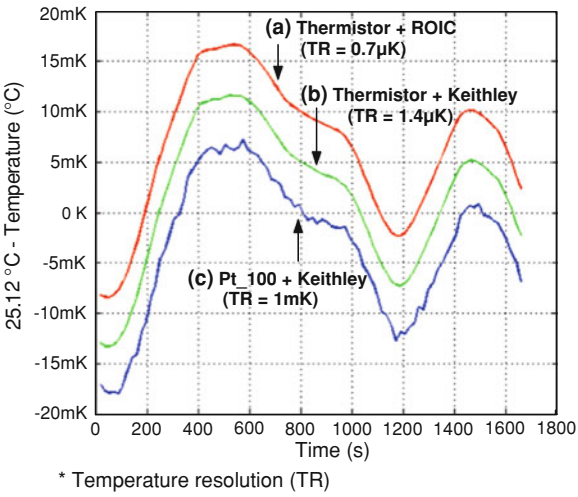


Fig. 6.49 Temperature drift as measured by a **a** thermistor bridge + ROIC, **b** thermistor bridge + Keithley, **c** Pt-100 + Keithley (for clarity, the curves are offset by 5 mK)

0.1 mHz 1/*f* noise corner, a maximum offset of 48nV and an offset drift of 6nV/°C. Compared to other work, our work achieves the best gain error of 0.037 %, 20X better offset and 1.5X better gain drift than [21]. Moreover, it only consumes a 270 µA supply current from a 5 V supply (CFIA 220 µA, ADC 50 µA).

Table 6.4 Performance of the ROIC versus the state-of-the-art

	This work	AD7193 [21]	CS5530 [22]	ADS1282 [23]	Thomsen [24]
Year	2011	2011	2009	2007	2000
Supply current	270 μA	4.3 mA	7 mA	4.5 mA	8.2 mA[a]
Supply voltage	5 V	5 V	5 V	5 V	5 V
1/*f* noise corner	0.1 mHz	–	25 mHz	–	10 mHz
Input range	±40 mV	±39 mV	±78 mV	±263 mV	±28 mV
CMRR	140 dB[b]	110 dB[b]	120 dB[b]	110 dB[b]	–
Input referred noise density	16.2 nV/$\sqrt{Hz}$	5nV/$\sqrt{Hz}$	12 nV/$\sqrt{Hz}$	5 nV/$\sqrt{Hz}$	6.2 nV/$\sqrt{Hz}$
Gain drift	DEM + GEC: 0.7 ppm/°C[b] DEM: 3 ppm/°C[b]	1 ppm/°C (typ)	2 ppm/°C (typ)	9 ppm/°C (typ)	15 ppm/°C (typ)
Gain error (uncalibrated)	0.037 %[a]	0.39 %[b]	1 %	1 %	–
Offset drift	6 nV/°C[a]	5nV/°Cb[b]	10nV/°C[b]	20 nV/°C[b]	70 nV/°C[a]
Offset (uncalibrated)	48 nV[a]	1 μV[a]	9.5 μV[a]	200 μV[a]	–
Nonlinearity	5 ppm[b]	–	30 ppm[b]	4 ppm[b]	–
Conversion time	0.173 s	0.2 s	0.13 s	0.004 s	0.0083 s
FOM(pJ/Conv) [25]	111	135	9000	172	160

[a] Worst case
[b] Typical case

6.8 Conclusions

This chapter described the system-level design and implementation of the read-out IC that consists of a current-feedback instrumentation amplifier (CFIA) and a switched-capacitor ΔΣ ADC. The CFIA provides high input impedance for bridge read-out and relaxes the noise and offset requirements of the ADC.

To achieve 1 mHz 1/*f* noise corner, both the input and intermediate stages of the CFIA are chopped, so as to provide sufficient gain to suppress the 1/*f* noise corner of the unchopped output stage down to mHz range. Chopping gives rise to a chopper ripple at the amplifier output and this ripple will be sampled by the sampling front-end of the succeeding ADC. To avoid noise aliasing, a continuous-time offset reduction loop is employed to suppress the ripple from the input stage, while the ripple from the intermediate stage is chopped in a bit-stream controlled manner, so as to reduce the correlation between the chopper ripple and quantization noise.

To reduce offset further to the nV-level, system-level chopping is employed to chop the entire read-out chain during multiple conversions. The modulated offset is then averaged out in the decimation filter. It has been found that to suppress 1/*f* noise and offset, input stage chopping combined with system-level chopping can be used as a better alternative to the multi-stage chopping with system-level

chopping. Measurement results show that the former achieves a 0.1 mHz 1/*f* noise corner and 48 nV worst-case offset.

The ADC employs a topology whose gain accuracy does not depend on component matching. Furthermore, with ratio-metric topology, the gain accuracy of the ADC's reference is much relaxed. These two solutions enable the ADC to achieve a gain error of less than 2 ppm. Thus, the gain error of the read-out IC is mainly determined by the mismatch between the input and feedback transconductors.

To eliminate the transconductor mismatch, dynamic element matching (DEM) is applied to the input and feedback transconductors to average out the mismatch. However, their CM dependency limits the achievable gain accuracy with DEM applied. To enhance their CM immunity, bulk-biasing and impedance-balancing techniques are applied. To reduce gain error and gain drift further, a digitally-assisted gain error correction scheme is proposed, which explores the power of digital signal processing succeeding the ADC to improve the gain accuracy and gain drift of the CFIA. This gain error correction scheme uses a linear interpolation algorithm to find the correct calibration voltage during start-up. Due to its ratio-metric property, the input calibration signal does not need to be known. Overall, GEC path serves as a coarse-trimming to the G_m mismatch, while the DEM acts as a fine-tuning to compensate for temperature drift.

Measurement results show that the offset and drift of the read-out IC exceeds the-state-of-art. These qualities make the proposed read-out IC very suitable for demanding bridge transducer applications, which require low thermal and 1/*f* noise, high accuracy, low drift, and simultaneously, low power consumption.

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Chapter 7
Conclusions

This final chapter summarizes the work described in Chaps. 1–6 and provides an overview of the original contributions and the most important findings presented in this thesis. It also shows how some of the techniques developed for bridge sensor readout can also be useful in other applications, and provides an outlook on future work.

7.1 Original Contributions

The following list provides an overview of the most important original contributions presented in this thesis. References to the thesis and the appropriate publications have also been included.

7.2 Chapter 4

- A multi-stage chopping strategy is proposed for a current-feedback instrumentation amplifier (CFIA), in which the input and intermediate stages are chopped and their gain is made high enough to suppress the 1/*f* noise of the output stage down to 1 mHz [1] (Sect. 4.2).
- To suppress the chopper ripple in a CFIA, a continuous-time offset reduction loop (ORL) is proposed [2, 3]. Due to its continuous-time nature, the ORL does not cause noise folding, thus reducing the noise power around the chopping frequency (Sect. 4.3).
- Compared to ripple reduction techniques using continuous-time [4] or discrete-time [5] notch filters or an auto-correction feedback loop [6], the key advantage of the ORL is that it is inherently stable. Thus, a low chopping frequency can be

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chosen to achieve low offset without the stability problems caused by excessive phase shift in the notch-filter (Sects. 2.4.5 and 4.3.2).
- Detailed analysis of the loop gain transfer function of the ORL in a CFIA [3] (Sect. 4.3.2).

7.3 Chapter 5

- The gain accuracy of a CFIA is mainly determined by the mismatch between its input and feedback transconductances. To improve this, dynamic element matching (DEM) can be applied. To suppress the resulting signal-dependent DEM ripple, a continuous-time gain error reduction loop (GERL) is proposed. The GERL continuously nulls the mismatch of the input and feedback transconductances, thus eliminating the need for trimming [7, 8] (Sect. 5.3).
- Detailed analysis of the loop gain transfer function of the GERL in a CFIA [8] (Sect. 5.3.3).
- Since the loop gain of the analog GERL is signal dependent and is zero for zero input. In this state, leakage causes the integrator output to drift away, thus it needs to re-settle when a finite input signal reappears. To avoid the need of re-settling, a digitally-assisted GERL that stores the gain mismatch information in the digital domain is proposed [8] (Sects. 5.4 and 5.7.2).

7.4 Chapter 6

- To suppress the 1/*f* noise in a read-out IC that consists of a CFIA and an ADC, the combination of input stage chopping (in the CFIA) and system-level chopping (that chops the complete read-out chain) is shown to be a better alternative to the combination of multi-stage chopping and system-level chopping. Lower offset and comparable 1/*f* noise corner frequency are achieved in the former approach (Sect. 6.4).
- To improve the gain accuracy, gain drift and linearity of the read-out IC, DEM is applied to the input and feedback transconductors of the CFIA. Furthermore, a gain error correction scheme is proposed in a digital backend to compensate the G_m mismatch of the CFIA by applying a compensation voltage to an auxiliary G_m stage. A linear interpolation algorithm, implemented in the digital backend, is used to determine the appropriate compensation voltage [9, 10] (Sect. 6.3).
- The common-mode (CM) dependency of the input and feedback transconductors limits the gain accuracy even with DEM applied. To improve CM immunity, threshold boosting and impedance balancing techniques are proposed, resulting in a 3.2 × improved gain accuracy without increasing the power consumption [11] (Sect. 6.6.1).

7.5 Main Findings

The following list summarizes the main findings of this thesis:

- To improve the gain accuracy of a CFIA, DEM can be applied to the input and feedback transconductors. This reduces the gain error from Δ to $\Delta^2/2$ and thus significantly reduces their mismatch. Turning on the GERL improves matters further, since it drives the mismatch Δ to zero. As a result, the transfer functions of these two transconductances become even more closely aligned, which, in turn, results in a further improvement in gain error, gain drift and linearity (Sect. 5.6).
- After applying DEM, the residual gain error of a CFIA is not limited by $\Delta^2/2$, but mainly by the CM dependency of its input and feedback transconductors (Sects. 3.3.3 and 5.2).
- A power efficient way to increase the output impedance of a PMOS differential pair is to use a low-threshold cascode transistor to fix the drain-source voltage of the input transistors. However, the maximum output impedance is limited by the threshold difference between the normal and low-threshold transistors, which is determined by the CMOS process used (Sect. 6.6.1).

7.6 Other Applications of this Work

It has been shown in Sect. 4.5 that the ORL can be applied to general purpose chopper CFIAs [12], chopper operational amplifiers [12] and capacitively-coupled chopper instrumentation amplifiers [13]. Due to its continuous-time nature, it does not cause noise folding. The same goes for the GERL. It can be applied in the high-gain/low-frequency path of a multi-path amplifier, e.g. the one in [12] to improve its low frequency gain accuracy.

7.7 Future Work

- The offset of the integrator of an ORL gives rise to extra ripple, which can not be suppressed by the ORL (See Sect. 4.4.1). This offset can be eliminated by a chopped and gain-boosted current buffer to isolate the demodulation chopper from the sensing capacitors (Fig. 4.14). It also can be mitigated by autozero-stabilizing the opamp in the integrator of the ORL (Fig. 4.13). Since chopping is avoided in this approach, there is no chopper ripple at the integrator output, which should eliminate the 2nd harmonic of the chopping frequency at the CFIA output.

- In the read-out IC, an offset reduction loop is used to reduce the CFIA's chopper ripple. This loop also can be implemented in a digitally-assisted manner, i.e. by using a DAC to generate an offset-compensating current.
- The CM dependency of the input and feedback transconductors limits the gain accuracy even with DEM applied. To improve CM immunity, bulk-biasing and impedance-balancing techniques have been applied to two transconductors made with simple PMOS differential pairs (Sect. 6.6.1). These techniques could also be applied to the improved CFIA with better gain accuracy, which has been described in Chap. 5.

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Summary

This thesis describes the theory, design and realization of precision interface electronics for bridge transducers and thermocouples that require high accuracy, low noise, low drift and simultaneously, low power consumption. This thesis is dedicated to two aspects: (1) the design of precision stand-alone instrumentation amplifiers (IAs) that can be used to drive an external Analog-to-Digital Converter (ADC); (2) the design of a read-out IC that combines an instrumentation amplifier and an ADC. Several new concepts and techniques have been proposed and verified in CMOS technology.

Chapter 1

An introduction and motivation of the work described in this thesis is given in this chapter. Precision bridge transducers and thermocouples typically output low-frequency (LF) signals of a few Hz with millivolt levels. Therefore, they require instrumentation amplifiers (IAs) with input-referred errors at the microvolt- or nanovolt- level to boost such signals to levels compatible with the typical input ranges of subsequent analog-to-digital converters (ADCs). Since sensor output signals are often either ground-referenced or accompanied by a large common-mode (CM) voltage, such IAs require ground-sensing capability and a high common-mode rejection ratio (CMRR) (>120 dB).

Current-feedback Instrumentation amplifiers (CFIAs) are well-suited for bridge read-out because of their high CMRR, ability to handle different input and output CM voltages and power efficiency. However, their main disadvantages are limited gain accuracy due to the mismatch of the input and feedback transconductors and limited input range due to the non-linearity of these transconductors. This thesis focuses on the design of improved CFIAs.

Furthermore, the CFIA can be used as a preamplifier and combined with an ADC to comprise a read-out IC. For instrumentation applications, the incremental

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ΔΣ ADCs are very suitable. The IAs in previous read-out ICs generally employed switched-capacitor (SC) or two-opamp IA topologies. Neither of these topologies is particularly power efficient. Since CFIAs are more power efficient, this thesis presents the design of a read-out IC that combines a CFIA and an ADC, both of which collaborate to achieve an optimum performance.

As a test-case, the challenging task of developing interface electronics for a precision thermistor bridge is described. This is intended for use in wafer steppers where μK-level temperature resolution is required. The resulting interface electronics is also applicable to other sensors, e.g. strain gauges, thermocouples and Hall sensors.

Chapter 2

Chapter 2 gives an overview of dynamic offset cancellation techniques such as chopping, auto-zeroing and offset-stabilization. It also shows how to apply these techniques to operational amplifiers. It is shown that since chopping is a continuous-time modulation technique that does not cause noise folding and is thus superior than auto-zeroing. However, in stand-alone amplifiers, the modulated $1/f$ noise and offset need to be suppressed to ensure a ripple free output.

There are numerous ways to eliminate chopper ripple, such as auto-zeroing, switched-capacitor (SC) or continuous-time (CT) notch filters or the use of an auto-correction feedback loop. The SC sampling techniques incur a certain noise folding penalty. The CT notch filter requires a good matching between the period of the chopping clock and the notch position in the CT filter. Furthermore, all the above-mentioned techniques suffer from the excess phase shift introduced by the notch filter. Therefore, a high chopping frequency (or a low unity-gain-bandwidth of the amplifier) is required to maintain stability. A new ripple reduction technique is proposed in Chap. 4 that avoids all these issues.

Chapter 3

The use of dynamic offset compensation techniques is extended to precision CFIAs, since they are well suited for bridge read-out. However, the gain accuracy of a CFIA is rather limited due to the mismatch between its input and feedback transconductors. Several techniques can be applied to improve its gain accuracy, such as resistor-degeneration, auto-gain calibration and dynamic element matching (DEM). However, resistor-degeneration requires significantly more power and auto-gain calibration can not maintain a continuous output signal. DEM improves gain accuracy by modulating the G_m mismatch to the DEM frequency, thus giving rise to a signal dependent ripple. To eliminate the DEM ripple, trimming can be used. However, it increases production costs and will not compensate for temperature drift. A new technique is proposed in Chap. 5 that eliminates the need of trimming.

Chapter 4

The architectural design and implementation of a stand-alone chopper CFIA are described. It consists of three gain stages, in which the input and intermediate stages are both chopped at 30 kHz to suppress their 1/*f* noise and also to provide sufficient gain to suppress the 1/*f* noise of the unchopped output stage. To suppress the chopper ripple due to the offset of the input stage, a continuous-time offset reduction loop (ORL) is proposed, while the chopper ripple associated with the intermediate stage was suppressed by chopping it at a much higher frequency (510 kHz).

The ORL uses a synchronous detection technique to demodulate the ripple, and then drives the ripple to zero by continuously compensating for the offset. Due to its continuous-time nature, the ORL does not cause noise folding. Furthermore, the ORL is inherently stable, which is the key advantage compared to other ripple reduction techniques using notch filters or auto-correction feedback loop. A low chopping frequency can thus be chosen for low offset. Other authors have shown that the ORL can also be applied to general-purpose chopper CFIAs and operational amplifiers.

Measurement results show that the ORL reduces the amplitude of the chopper ripple by a factor of 1100, to levels below the amplifier's own input-referred noise level. The CFIA achieves 1 mHz 1/*f* noise corner at a noise PSD of 15 nV/$\sqrt{\text{Hz}}$ while consuming only 230 μA supply current (NEF = 8.8), which is quite respectable compared to previous work. To the authors' knowledge, this represents the best LF noise performance ever reported for a stand-alone CMOS instrumentation amplifier.

Chapter 5

The chopper CFIA described in the previous chapter achieves microvolt-level offset and a high CMRR (>120 dB). However, its gain error, mainly determined by the mismatch of the input and feedback transconductors (noted as "Δ"), is about 0.5 %, which becomes the dominant source of residual error. Thus, the design and implementation of a CFIA with improved gain accuracy are discussed in this chapter.

To improve gain accuracy, dynamic element matching (DEM) is applied to the input and feedback transconductors of the CFIA, so as to average out their mismatch. DEM modulates the G_m mismatch to the DEM frequency, thus giving rise to a signal-dependent ripple at CFIA output. To suppress this ripple, a gain error reduction loop (GERL) is proposed to continuously null the mismatch of the input and feedback transconductances, thus eliminating the need for trimming.

Unlike the ORL, which feeds back an additive offset-compensating signal, the GERL feeds back a *multiplicative* gain-compensating signal, which adjusts the

ratio of the input and feedback transconductances. The output DEM ripple is then the product of the mismatch and the output signal, and so the gain of the GERL will be signal dependent. To guarantee negative feedback, a polarity reversing switch is used to link the polarity of the GERL to that of the output signal.

The loop gain of the GERL is proportional to the input signal and so is zero for zero input. In this case, leakage causes the integrator output $V_{\text{int,GE}}$ to drift with a time constant of several seconds and eventually clip. The GERL will then need to resettle whenever a finite input signal re-appears. To avoid the need for resettling, a digitally-assisted GERL is implemented to store the mismatch information in the digital domain in this circumstance. For comparison, the analog implementation of the GERL is also implemented.

DEM reduces the gain error from Δ to $\Delta^2/2$, moving the average input and feedback transconductances closer to each other. This results in a CFIA with improved gain error, gain drift and linearity. The GERL improves matters further, since it drives the mismatch to zero. As a result, the average input and feedback transconductors become even more closely *aligned*. Finally, the use of DEM and the GERL also increases the linear input range of the CFIA by a factor of three.

Measurement results show that without trimming, the CFIA achieves a gain error of less than 0.06 % and a maximum gain drift of 6 ppm/°C in a power efficient manner (NEF = 11.2). Compared to a CFIA with similar gain accuracy, but using resistor-degenerated input stages, this represents a 4× improvement in power efficiency, which is equivalent to a 16× less power when achieving the same noise level. These measurement results confirm that the combination of DEM and the GERL is a power-efficient manner of improving the gain accuracy, gain drift and linearity of a CFIA.

Chapter 6

The CFIA described in Chap. 4 is then combined with a switched-capacitor sigma–delta ($\Delta\Sigma$) ADC to realize a read-out IC. The system-level design and implementation of the read-out IC are described. The CFIA provides high input impedance for bridge read-out and relaxes the noise and offset requirements of the ADC. The ADC employs a topology whose gain accuracy does not depend on component matching. Furthermore, the use of a ratio-metric topology means that the accuracy of the ADC's reference is much relaxed. These two solutions enable the ADC to achieve a gain error of less than 2 ppm. Thus, the gain error of the read-out IC is mainly determined by the mismatch between the input and feedback transconductors of the CFIA.

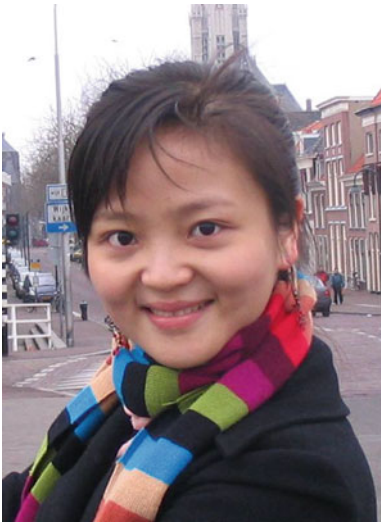
To eliminate this mismatch, DEM is applied to the two transconductors to average out their mismatch. However, the CM dependency of these transconductors limits the achievable gain accuracy even with DEM applied. To enhance their CM immunity, bulk-biasing and impedance-balancing techniques are employed. To reduce gain error and gain drift further, a digitally-assisted gain

error correction (GEC) scheme is applied, which digitally processes the output of the ADC and feeds back a gain error correcting signal. This improves the gain accuracy and gain drift of the CFIA. Overall, the GEC path serves as a coarse-trim of G_m mismatch, while the DEM acts as a fine-trim that compensates for temperature drift.

To reduce offset to the nV-level, system-level chopping is employed to chop the entire read-out chain during multiple conversions. The modulated offset is then averaged out in the decimation filter. It has been found that the combination of input stage chopping in the CFIA and system-level chopping is a better way to suppress 1/*f* noise and offset, compared to the use of multi-stage chopping. Measurement results show that the former achieves 0.1 mHz 1/*f* noise corner, while the latter achieves 1 mHz 1/*f* noise corner. Furthermore, in the former approach, the choppers in the intermediate stage of the CFIA are off, thus avoiding extra offset due to the coupling of charge injection and clock spikes through the Miller-compensation capacitor. The ultimate residual offset of the read-out IC is then determined by its resolution and is about 48 nV.

Measurement results show that the read-out IC achieves state-of-art 1/*f* noise corner (0.1 mHz), offset (48 nV), gain drift (1.2 ppm/°C), offset drift (6 nV/°C) and power efficiency (FOM = 111 pJ/Conv). These qualities make the proposed read-out IC very suitable for demanding bridge transducer applications, which require low thermal and 1/*f* noise, high accuracy, low drift, and simultaneously, low power consumption.

About the Author



Rong Wu was born on November 4, 1981. She received the B.Eng. degree in microelectronics from Fudan University, Shanghai, China, in 2003. After one year graduation study in Fudan, she started the M.Sc. study in electrical engineering at Delft University of Technology, Delft, The Netherlands, in September, 2004. She received her M.Sc. degree of TU Delft in February, 2006 and her M.Sc. degree of Fudan University in July, 2006, both on electrical engineering.

In October 2006, she joined the Electronic Instrumentation Laboratory of the TU Delft, pursuing her Ph.D degree on the subject of precision amplifier and sigma–delta ADCs for sensor read-out. In December 2011, she received her Ph.D degree. Currently, she is with precision ADC group of Analog Devices in Wilmington, MA. Her research interests include sensors, precision analog and mixed-signal interface electronics.

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